C9801

Low EMI Clock Generator for Pentium™ II CPU Systems with Power Management

Product Features

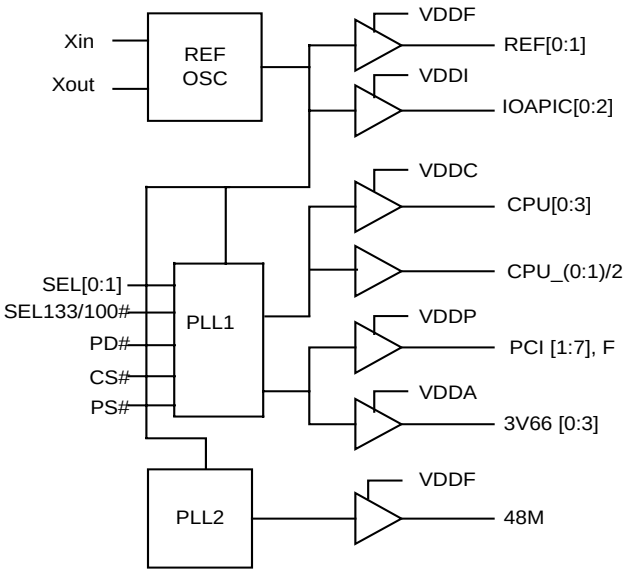
- Supports Intel Pentium™ II CPU designs.
- 133 and 100 Mhz CPU clock support
- Designed to meet Intel chipset specification
- 4 CPU clocks with isolated power supply
- 2 CPU/2 clock with isolated power supply
- 8 PCI clocks with isolated power supply
- 3 IOAPIC clocks with isolated power supply
- One 48 MHz fixed clock for USB/Super IO with isolated power supply
- 4 3V66 clocks with isolated power supply
- 2 reference clocks with isolated power supply
- <175 pS Max. skew among CPU clocks
- <500 pS Max. skew among PCI clocks
- Power management control of CPU and PCI clocks
- 56-pin SSOP package
- Spread Spectrum EMI reduction mode

Frequency Table

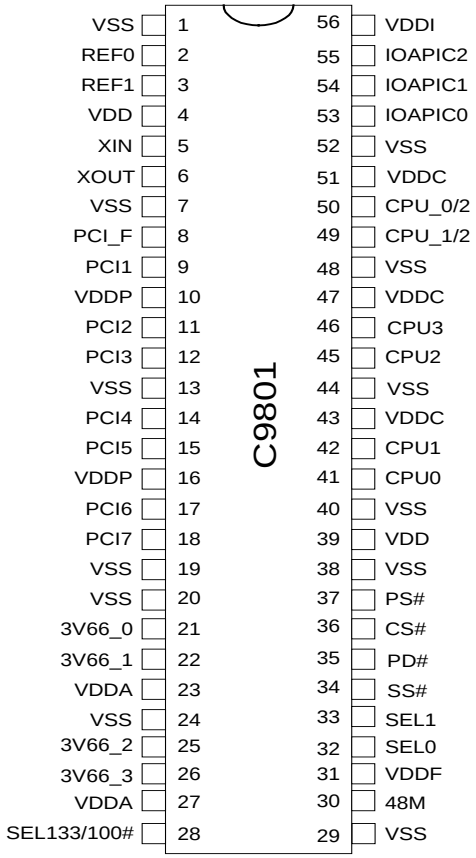
SEL133/100#	CPU	PCI
0	100*	33.3*
1	133*	33.3*

*See complete table on page 3.

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
5	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
6	**Xout**	VDD	O	OSC1	On-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
41,42, 45,46	**CPU(0:3)**	VDDC	0	BUF1	Clock outputs. CPU frequency table specified on page 1.
49, 50	**CPU/2 [0,1]**	VDDC	O	BUF4	CPU Synchronous clocks. Its frequency is half CPU clocks.
8	**PCI_F**	VDDP	O	BUF4	Free running PCI clock. Does not stop when PS# is brought to a logic 0 (low) level.
9, 11, 12, 14, 15, 17, 18	**PCI (1:7)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
1, 7,13, 19,20, 24,29, 38, 40, 44, 48,52	**VSS**	-	P	-	Ground pins for the device.
10, 16	**VDDP**	-	P	-	3.3 Volt power supply pins for PCI and PCI_F clock output buffers.
31	**VDDF**	-	P	-	3.3 Volt power supply pins for 48 MHz clock output buffers.
56	**VDDI**	-	P	-	2.5 Volt power supply pins for IOAPIC clock buffers.
43, 47	**VDDC**	-	P	-	3.3 or 2.5 Volt power supply pins for CPU clock output buffers.
4, 39	**VDD**				Power supply pins for analog circuits and core logic.
23, 27	**VDDA**	-	P	-	3.3 Volt power supply pins for 3V66 clock output buffers.
21, 22, 25, 26	**3V66 (0:3)**	VDDA	O	BUF	Fixed 66.6 Mhz Advanced Graphics Processor Clock. This clock is rising edgy synchronous with the CPU clock.
2,3	**REF (0:1)**	VDDR	O	BUF#	Buffered outputs of on-chip reference oscillator.
30	**48M**	VDDF	O	BUF3	Fixed 48 MHz frequency clock output.
28	**SEL133/ 100#**	-	I	PAD	CPU frequency select pin. **By design this input does not contain any internal pull-up or pulldown resistor.**
35	**PD#**			PU	Device power down signal. Removes power from all internal logic when at a logic low level. See page 4.
37	**PS#**			PU	PCI clock stop signal. Stops all PCI clocks when at a logic low level, except for the PCI_F clock. See page 4.
36	**CS#**			PU	CPU clock stop signal. Stop all CPU clocks when at a logic low level. See page 4.
32, 33	**SEL (0:1)**	-	I	PAD PU	Function selector pins. See description on page 3.
34	**SS#**	-	I	PAD PU	When driven to a logic low level, this pin enables the device's EMI reducing Spread Spectrum mode (affects only CPU, PCI, 3V66, and IOAPIC clocks).
53,54, 55	**IOAPIC(0:2)**	VDDI	0	PAD	2.5 volt copies of a 16.67 Mhz clock that is synchronized with the CPU clock. See note on page 3

SEL 133/100#	SEL1	SEL0	CPU	CPU/2	3V66	PCI	48M	REF	IOAPIC
0	0	0	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
0	0	1	105 MHz	52.5 MHz	70.0 MHz	35.0 MHz	48 MHz	14.5 MHz	17.50 MHz
0	1	0	100 MHz*	50 MHz*	66.6 MHz*	33.3 MHz*	High-Z	14.3 MHz	16.67MHz*
0	1	1	100 MHz*	50 MHz*	66.6 MHz*	33.3 MHz*	48 MHz	14.3 MHz	16.67MHz*
1	0	0	REF/2	REF/4	REF/4	REF/8	REF/2	REF	REF/16
1	0	1	139.7 MHz	69.8 MHz	69.8 MHz	34.9 MHz	48 MHz	14.3 MHz	17.40 MHz
1	1	0	133 MHz	66.6 MHz	66.6 MHz	33.3 MHz	High-Z	14.3 MHz	16.67MHz
1	1	1	133 MHz	66.6 MHz	66.6 MHz	33.3 MHz	48 MHz	14.3 MHz	16.67MHz

IOAPIC Clock Synchronization

This device incorporates IOAPIC clock synchronization. With this feature, the IOAPIC clocks are derived from the CPU clock and represent a divided by 8 (133 MHz CPU clock mode) or divided by 6 (100 MHz CPU clock mode) clock. The IOAPIC clock lags the CPU clock by the specified 1.5 to 4.0 nSEC.

Power Management Functions

All PCI (excluding PCI_F) and CPU clocks can be enabled or stopped via the PSTOP and CSTOP input pins. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, (after bring PD from a low to high state) the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CS#	PS#	PD#	CPU	CPU/2	3V66	PCI	PCIF	IOAPIC	48M	REF	XTAL & VCOs
X	X	0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF
0	0	1	LOW	ON	LOW	LOW	ON	ON	ON	ON	ON
0	1	1	LOW	ON	LOW	ON	ON	ON	ON	ON	ON
1	0	1	ON	ON	ON	LOW	ON	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON	ON

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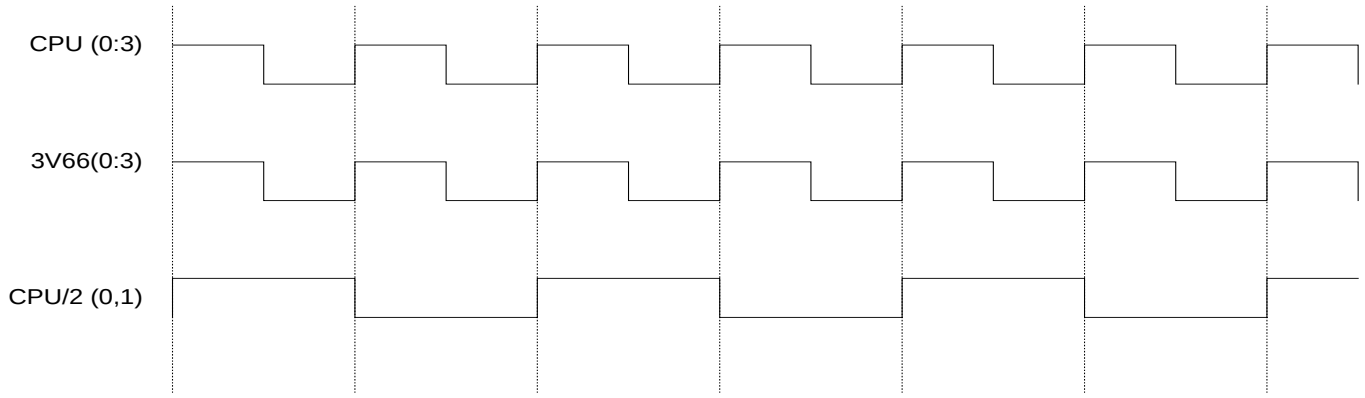
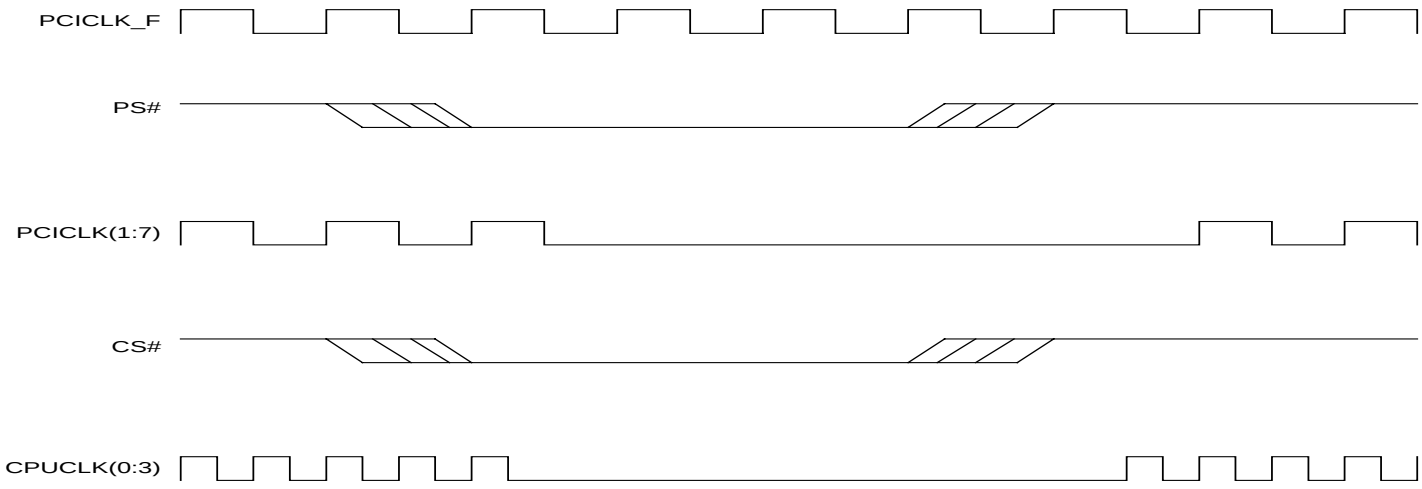
Power Management Functions (Cont.)

CPU, 3V66, and CPU/2 Clock Phase Alignment



Power Management Timing

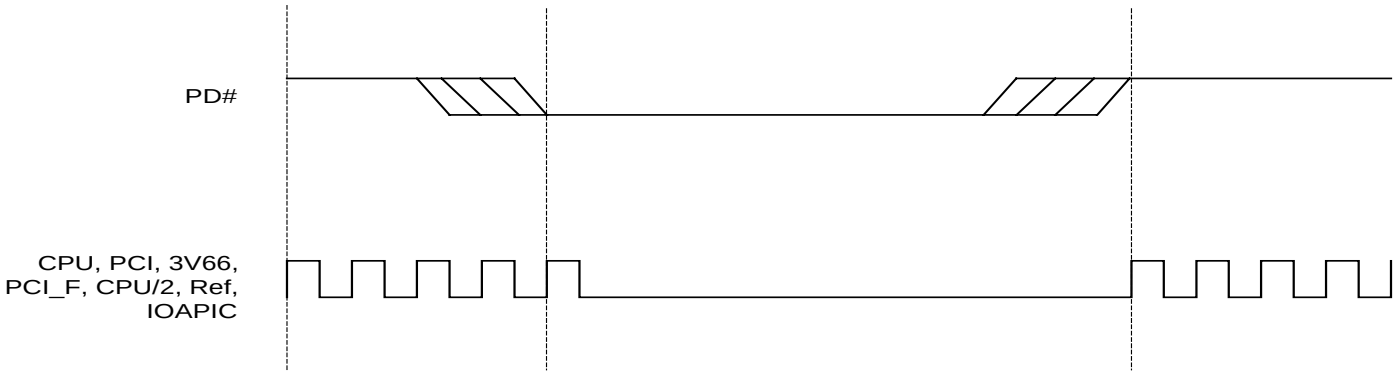


Power Management Timing

		Latency
Signal	**Signal State**	**No. of rising edges of free running PCICLK (PCIF)**
CS#	0 (disabled)	1
	1 (enabled)	1
PS#	0 (disabled)	1
	1 (enabled)	1
PD#	1 (normal operation)	3 mS
	0 (power down)	2 mS max.

Notes:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PD# goes inactive (high) to when the first valid clocks are driven from the device.

Power Management Timing



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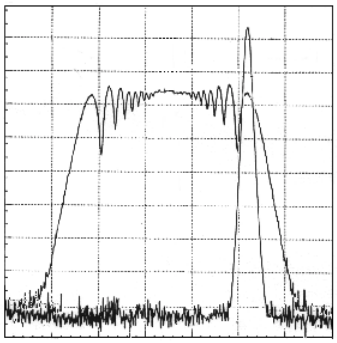
Spectrum Spread Clocking



Spectrum Analysis

Spectrum Spreading Selection Table

Min(MHz)	Center(MHz)	Max(MHz)	CPU Frequency	% OF Frequency Spreading	Mode
99.5	99.75	100	100	0.5% (-0.5%% + 0%)	Down Spread
126.4	129.7	133	133.3	0.5% (-0.5% + 0%)	Down Spread

Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range: VSS<(Vin or Vout)<VDD

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL2	-	-	0.8	Vdc	SDATA, SCLK
Input High Voltage	VIH2	2.0	-	-	Vdc	SDATA, SCLK
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	Pull up
Input High Current (@VIL = VDD)	IIH			5	µA	Pull up
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd_{max}	-	-	175	mA	Note 1
Static Supply Current	Isdd	-	-	0.3	mA	PD# pin at logic low level
VDD = VDDS = 3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note1: CPU frequency = 133 MHz, all outputs loaded to datasheet maximum capacitive loading values and Vdd = 3.465V

AC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V for 3.3 Volt VDD clocks and 1.25V for 2.5V VDD clocks
SKEW PERFORMANCE						
CPU to CPU Skew	$tSKEW_{cc}$	0	-	175	pS	CPU load = 20 pF, measured at 1.25V
CPU/2 to CPU/2 Skew	$tSKEW_{cc2}$	0	-	175	pS	CPU/2 load 20 pF, measured at 1.25V
IOAPIC to IOAPIC Skew	$tSKEW_{II}$	0	-	250	pS	IOAPIC load = 20 pF, measured at 1.25V
3V66 to 3V66 Skew	$tSKEW_{AA}$	0	-	250	pS	3V66 load = 30 pF, measured at 1.5V
PCI to PCI Skew	$tSKEW_{PP}$	0	-	500	pS	PCI load = 30 pF measured at 1.5V
CLOCK OFFSETS						
CPU to 3V66 Offset	$tOFF_{CA}$	0	-	1.5	nS	CPU load = 20 pF, 3V66 load = 30 pF measured at 1.25V, 3V66 = 1.5V (CPU leads)
3V66 to PCI Offset	$tOFF_{CP}$	1.5	-	4.0	nS	3V66 load = 30 pF, PCI load = 30 pF measured at 1.5V
CPU to IOAPIC Offset	$tOFF_{CL}$	1.5	-	4.0	nS	CPU load = 20 pF, IOAPIC load = 20 pF measured at 1.25V (CPU leads)
JITTER PERFORMANCE						
ΔPeriod Adjacent Cycles CPU, CPU/2 and IOAPIC	ΔP	-	-	±250	pS	Measured at 1.25 volts, 20 pF load
ΔPeriod Adjacent Cycles 48M, 3V66, PCI and REF	ΔP	-	-	± 500	pS	Measured at 1.50 volts, 3V66 at 30 pF load, all others at 20 pF load
VDD = VDDP = VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%, TA = 0°C to +70°C						

Buffer Characteristics for IOAPIC (0:2), and CPU/2 (0,1)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = VDD/2
Pull-Up Current Max	IOH_{max}	-	-	-13.6	mA	Vout = VDD – 0.5V
Pull-Down Current Min	IOL_{min}	27.7	-	-	mA	Vout = VDD/2
Pull-Down Current Max	IOL_{max}	-	-	11.8	mA	Vout = 0.4 V
Rise Time Min Between 0.4 V and 2.0 V	TR_{min}	0.4	-	1.6	nS	20 pF Load
Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	0.4	-	1.6	nS	20 pF Load
Dynamic Output Impedance	Z_O		-		Ohms	
VDD = VDDP = VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%, TA = 0°C to +70°C						

Buffer Characteristics for CPU(0:3)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-32.2	-	-	mA	Vout = VDD/2V
Pull-Up Current Max	IOH_{max}	-	-	-15.8	mA	Vout = VDD – 0.5V
Pull-Down Current Min	IOL_{min}	35.3	-	-	mA	Vout = VDD/2
Pull-Down Current Max	IOL_{max}	-	-	14.4	mA	Vout = 0.4 V
Rise Time Min Between 0.4 V and 2.0 V	TR_{min}	0.4	-	1.6	nS	20 pF Load
Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	0.4	-	1.6	nS	20 pF Load
Dynamic Output Impedance	Z_O		-		Ohms	
VDD = VDDP = VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%, TA = 0°C to +70°C						

Buffer Characteristics for REF(1:3) and 48(1:2) MHz

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-17.7	-	-	mA	Vout = VDD/2V
Pull-Up Current Max	IOH_{max}	-	-	-6.1	mA	Vout = VDD – 0.5V
Pull-Down Current Min	IOL_{min}	21.3	-	-	mA	Vout = VDD/2V
Pull-Down Current Max	IOL_{max}	-	-	5.9	mA	Vout = 0.4 V
Rise Time Min Between 0.4 V and 2.4 V	TR_{min}	1.0	-	4.0	nS	20 pF Load
Fall Time Max Between 0.4 V and 2.4 V	TF_{max}	1.0	-	4.0	nS	20 pF Load
Dynamic Output Impedance	Z_O		-		Ohms	
VDD = VDDP = VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0°C to +70°C						

Buffer Characteristics for PCICLK(0:7), 3V66 (0,7)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-41.6	-	-	mA	Vout = VDD/2V
Pull-Up Current Max	IOH_{max}	-	-	-15.5	mA	Vout = VDD – 0.5V
Pull-Down Current Min	IOL_{min}	44.1	-	-	mA	Vout = VDD/2V
Pull-Down Current Max	IOL_{max}	-	-	13.7	mA	Vout = 0.4 V
Rise Time Min Between 0.4 V and 2.4 V	TR_{min}	0.5	-	2.0	nS	30 pF Load
Fall Time Max Between 0.4 V and 2.4 V	TF_{max}	0.5	-	2.0	nS	30 pF Load
Dynamic Output Impedance	Z_O		-		Ohms	
VDD = VDDP = VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC						

Crystal and Reference Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	Note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	Note 1
X1 and X2 Load	CL		36		pF	Internal crystal loading capacitors on each pin (to ground). Provided by C9801.

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0 pF.(matching CL)

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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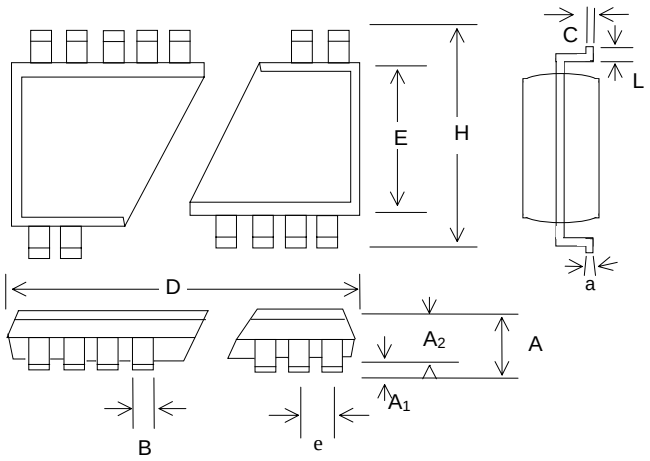
Package Drawing and Dimensions



56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.720	0.725	0.730	18.29	18.42	18.54
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9801CY	56 Pin SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example:

Cypress
C9801CY
Date Code, Lot #

C9801CY

- Package: Y = SSOP
- Revision
- Device Number

Notice

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Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107057	06/12/01	IKA	Convert from IMI to Cypress