C9641

133 MHz Clock Generator for ALI 1641 Chipset Systems

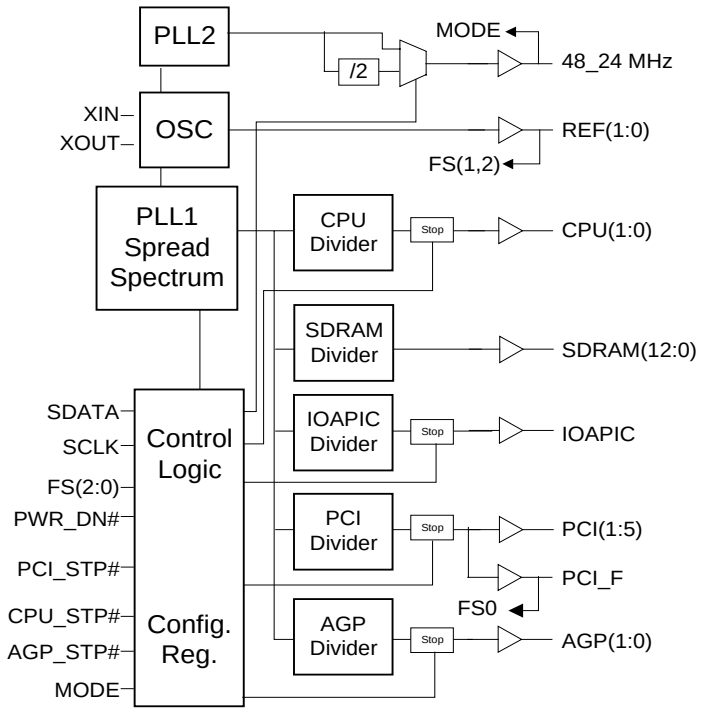
Product Features

- Supports ALI 1641 chipsets
- 2 CPUs at 2.5V, up to 146.2 MHz
- 2 -AGP Clocks at 3.3V
- 13 SDRAM's at 3.3V, up to 146.2 MHz
- 6 - PCI's Clocks at 3.3V,
- 1 IOAPIC at 2.5V at 14.318 MHz
- 1 - 48 MHz or 24 MHz programmable via SMBus
- 2 REF at 3.3V, 14.318 MHz
- Power management capability
- SMBus programming interface
- CYPRESS Spread Spectrum for EMI control
- CPU to PCI offset 1.0nS to 4.0 nS (CPU early)
- Available in 48 SSOP and TSSOP package

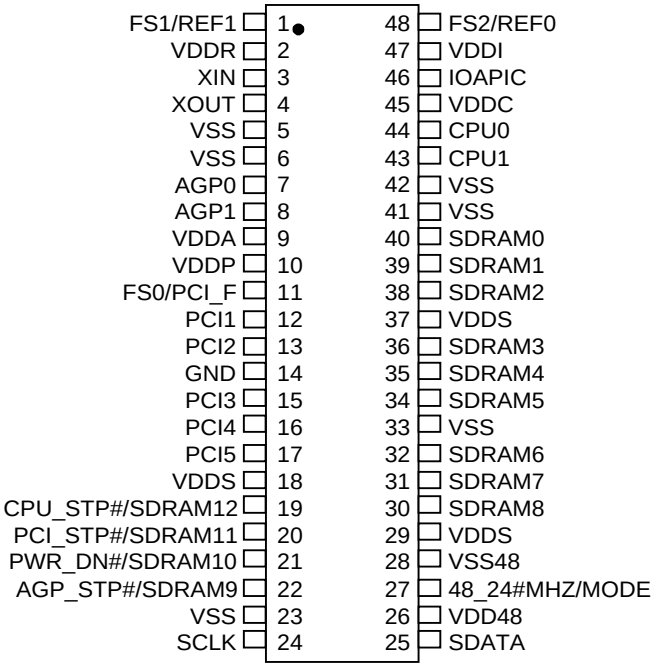
Frequency Table

								48_24# MHz SMBus Byte 0 Bit 0	
FS2	FS1	FS0	CPU	SDRAM	AGP	PCI	REF	0	1
0	0	0	66.82	100.23	66.8	33.40	14.318	24M	48M
0	0	1	100.23	100.23	66.8	33.40	14.318	24M	48M
0	1	0	66.82	66.82	66.8	33.40	14.318	24M	48M
0	1	1	133.64	100.23	66.8	33.40	14.318	24M	48M
1	0	0	66.82	133.64	66.8	33.40	14.318	24M	48M
1	0	1	100.23	133.64	66.8	33.34	14.318	24M	48M
1	1	0	100.23	66.82	66.8	33.40	14.318	24M	48M
1	1	1	133.64	133.64	66.8	33.40	14.318	24M	48M

Block Diagram



Pin Configuration



Cypress Semiconductor Corporation
525 Los Coches St.
Milpitas, CA 95035. Tel: 408-263-6300, Fax: 408-263-6571
http://www.cypress.com

Pin Description

PIN No.	Pin Name	TYPE	Description
1	**FS1/ REF1**	IN / OUT	This is a power on bi-directional pin with an internal pull-up. During power up, this pin is an input “FS1” for setting the CPU frequency (see table1, page 1) (see app note, page 4). When the power reaches the rail, this pin becomes a buffered output of the signal applied at Xin (typically 14.318 MHz).
3	**XIN**	IN	Input pin to the crystal oscillator. This pin connects to the crystal lead. It also may serve as the input to an externally generated clock.
4	**XOUT**	OUT	Output pin of the crystal oscillator. This pin connects the crystal lead. When an externally generated signal is applied to XIN, this pin remains unconnected.
8, 7	**AGP (1:0)**	OUT	AGP clock outputs. They are synchronous to CPU clocks
11	**FS0/ PCI_F**	IN / OUT	This is a power on bi-directional pin with an internal pull-up. During power up, this pin is an input “FS0” for setting the CPU frequency (see table1, page 1) (see app note, page 4). When the power reaches the rail, this pin becomes a PCI clock output. This clock does not stop when PCI_STP# is asserted low.
17, 16, 15, 13, 12	**PCI (1:5)**	OUT	PCI clock outputs. They are synchronous to CPU clocks.
19	**CPU_STP# / SDRAM12**	IN / OUT	This is a bi-directional pin with an internal pull-up. Its direction is controlled by the state of “Mode” (pin27). If Mode = 1, this pin is an SDRAM12 clock output. If Mode = 0, this pin is a CPU_STP# input pin. When CPU_STP# is asserted low CPU(0:1) clocks are synchronously stopped in a low state. (See Power Management Description, page 5.)
20	**PCI_STP# / SDRAM11**	IN / OUT	This is a bi-directional pin with an internal pull-up. Its direction is controlled by the state of “Mode” (pin27). If Mode = 1, this pin is an SDRAM11 clock output. If Mode = 0, this pin is a PCI_STP# input pin. When PCI_STP# is asserted low PCI(1:5) clocks are synchronously stopped in a low state. (See Power Management Description, page 5.)
21	**PD# / SDRAM10**	IN / OUT	This is a bi-directional pin with an internal pull-up. Its direction is controlled by the state of “Mode” (pin27). If Mode = 1, this pin is an SDRAM10 clock output. If Mode = 0, this pin is a PD# input pin. When PD# is asserted low, all clocks are stopped in a low state. (See Power Management Description, page 5.)
22	**AGP_STP# / SDRAM9**	IN / OUT	This is a bi-directional pin with an internal pull-up. Its direction is controlled by the state of “Mode” (pin27). If Mode = 1, this pin is an SDRAM9 clock output. If Mode = 0, this pin is a AGP_STP# input pin. When AGP_STP# is asserted low, AGP(0:1) clocks are synchronously stopped in a low state (See Power Management Description, page 5.)
24	**SCLK**	IN	SMBus compatible SDATA input. Has an internal pull-up (>100KΩ)
25	**SDATA**	IN	SMBus compatible SCLK input. Has an internal pull-up (>100KΩ)
27	**MODE / 48_24# MHz**	IN / OUT	This is a power on bi-directional pin with an internal pull-up. During power up, this pin is an input “Mode”. (see app not, page 4). If “Mode” is strapped high, then pins 19-22 are SDRAM (9:12) outputs. If “Mode” is strapped low, the pins 19-22 are inputs and the power management feature is enabled. When the power reaches the rail, this pin becomes a 48_24#Mhz programmable output clock. The frequency of this output defaults to 48MHz. It may be programmed to 24MHz via the SMBus bus, Byte 0, Bit0.
30, 31, 32, 34, 35, 36, 38, 39, 40	**SDRAM(0:8)**	OUT	SDRAM clock outputs. They are synchronous to CPU clocks.

Pin Description (Cont.)

PIN No.	Pin Name	TYPE	Description
46	**IOAPIC**	OUT	14.31818 MHz, 2.5V clock output. This output is used to clock the CPU communication bus in multi processor systems.
48	**FS2 / REF0**	IN / OUT	This is a power on bi-directional pin with an internal pull-up. During power up, this pin is an input “FS1” for setting the CPU frequency (see table1, page 1) (see app not, page 4). When the power reaches the rail, this pin becomes a buffered output of the signal applied at Xin (typically 14.318 MHz).
44, 43	**CPU (1:0)**	OUT	2.5V host bus (CPU) clock outputs. See Table 1 Page 1 for frequency programming.
2	**VDDR**	PWR	3.3V power supply for reference output clocks and crystal circuitry.
9	**VDDA**	PWR	3.3 Volt Power supply for AGP clock.
10	**VDDP**	PWR	3.3V power supply for PCI clocks.
18, 29, 37	**VDDS**	PWR	3.3 Volt Power supply pins for SDRAM's.
45	**VDDC**	PWR	2.5 Volt Power supply pin for CPU (1:0) output buffers.
47	**VDDI**	PWR	2.5 Volt Power supply pin for IOAPIC output.
5, 6, 14, 28, 33, 41, 42, 23	**VSS**	PWR	Power supply Ground return pins for the device.
26	**VDD48**	PWR	Power supply pin for the 48 MHz output.

Internal pull-ups are typically 250KΩ. They may vary between 200KΩ and 500KΩ.

Power on Bi-Directional Pins

Power Up Condition:

Pins 1, 11, 27, and 48 are Power up bi-directional pins and are used for programming initial power up frequency and desktop/mobil mode functions in this device (see Pin description, Page 2). During power-up, these pins are in input mode (see Fig 2, below), therefore, they are considered input select pins internal to the IC. After a settling time, the Selection data is latched into internal control registers and these pins then become toggling clock outputs.

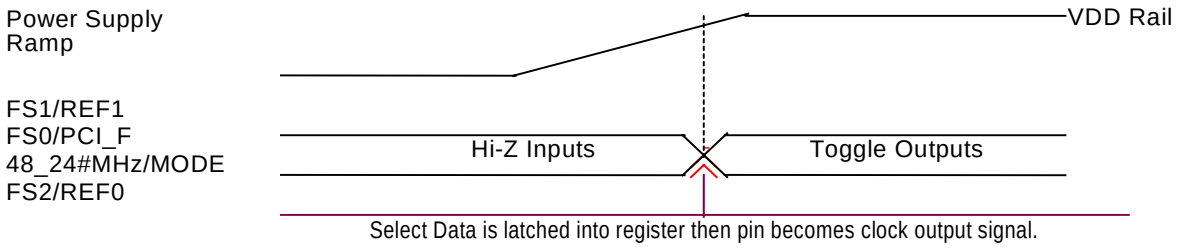


Fig. 2

Strapping Resistor Options:

The power up bidirectional pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 3mS settling time), then **it is recommended** to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig. 3A and Fig. 3B.

Fig. 3A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.4A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 3B represent a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

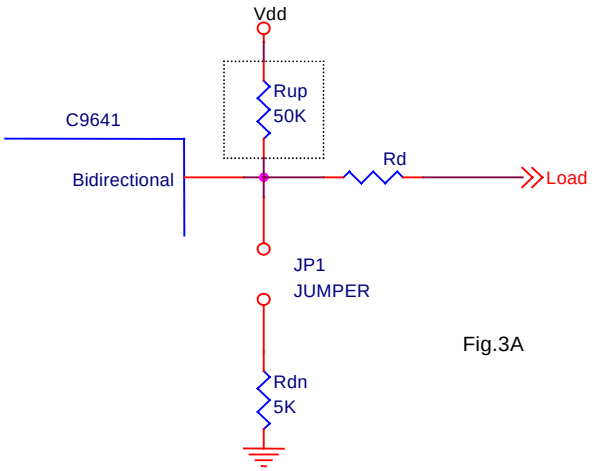


Fig.3A

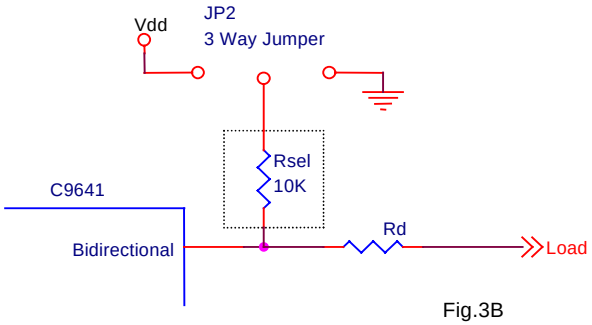


Fig.3B

Power Management Functions

If the "Mode" pin (pin 27) is strapped to a logic 0 at power up, the power management pins will be enabled. Power Management on this device is controlled by CPU_STP# (pin19), PCI_STP# (pin20), PWR_DN# (pin21), and AGP_STP# (pin22).

When CPU_STP# is forced low, all CPU signals are synchronously (no glitch) disabled in a low state. The CPU clocks do not modulate stop, they will toggle one to three complete cycles before stopping on the falling edge, regardless of the number of cycles it completes, it will stop before the next PCI_F rising edge occurs. This is to ensure synchronous stopping after a full cycle without any glitches. When CPU_STP# is released to high, the CPU clocks are synchronously re-enabled. The clocks will wait the equivalent of one to three cycles after CPU_STP# is asserted high then will start toggling on the rising edge. Regardless of the number of cycles it completes, it will start before the next PCI_F rising edge occurs. This also is to ensure a synchronous start of a full clock cycle.

When PCI_STP# is forced low, only PCI(1:5) signals are synchronously disabled in a low state. These signals will complete one full cycle before stopping on the following falling edge. PCI_F is still running. When PCI_STP# is released to high, PCI(1:5) are synchronously re-enabled after one full PCI_F cycle latency.

Power Management Functions (Cont.)

When AGP_STP# is forced low, both AGP clocks are synchronously disabled in a low state. These signals will complete one full cycle before stopping one the following falling edge When AGP_STP# is released to high, AGP clocks are synchronously re-enabled after one full PCI_F cycle latency.

When PWR_DN# is forced low, CPU(0:1), PCI(F,1:5), IOAPIC, SDRAM(0:12), 48_24#MHz, and REF(0:1) signals are synchronously disabled, all internal circuitry (including the crystal buffer) is shutdown and the device is then placed in Low Power (or in power down) Mode. After PWR_DN# is forced low, all power supplies (3.3V and 2.5V) may be removed. All power supplies must be re-applied 200mS before releasing PWR_DN# (to high), consequently, the device must be allowed 1mS before the clock outputs settle to their preset frequencies. (see Fig.4, and table 2 below)

Power Management Timing

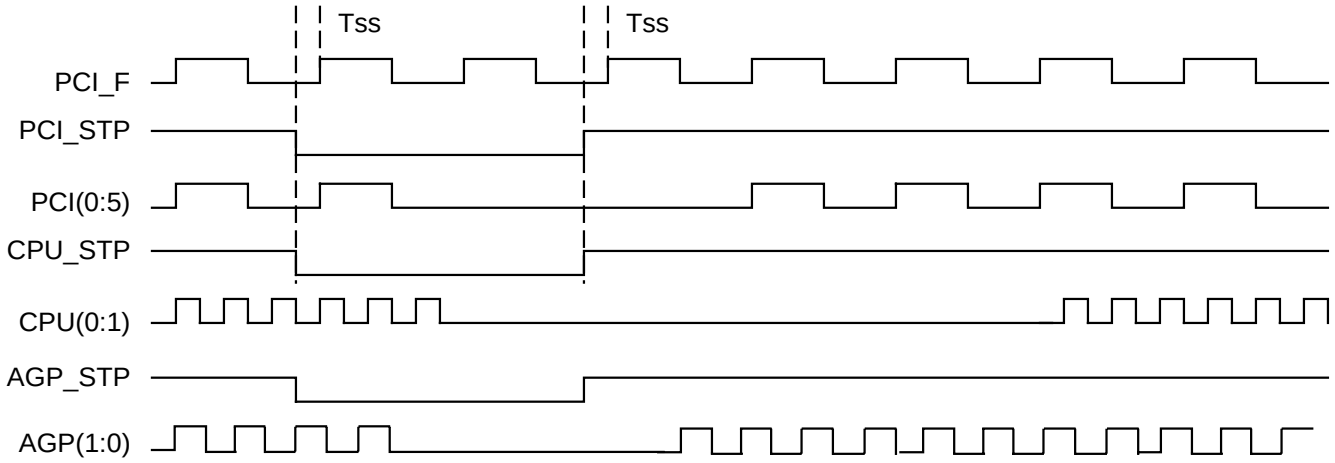


Fig. 4

Tss is the stop clock setup time. All functionality is referenced to the rising edge of PCI_F. If the tss timing is met, with respect to the next occurring PCI_F low to high transition, then the CPU or PCI clocks that are controlled are guaranteed to stay low (stopped) or to rise (run) at the next rising edge of PCI_F. See the AC parameters for tss time.

Power Management Function Table

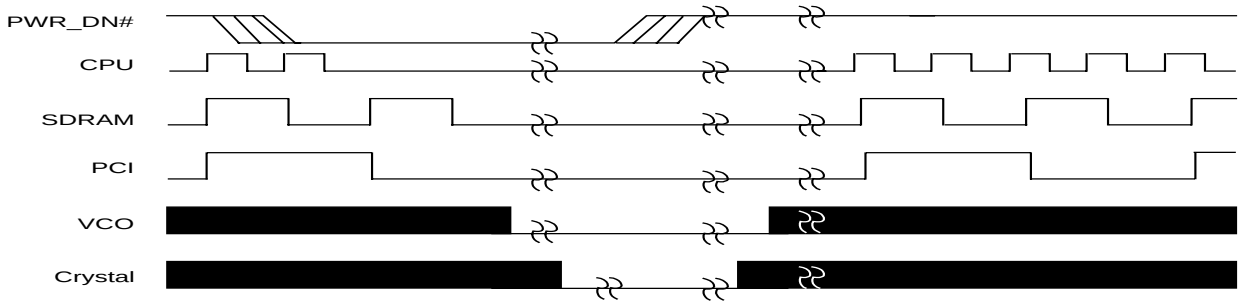
AGP_ STP#	CPU_ STP#	PWR_ DN#	PCI_ STP#	SDRAM (0:12)	CPU (0:1)	REF (0:1)	PCI (1:5)	PCI_F	48_24M	IOAPIC	PLL1	PLL2	AGP (0:1)
X	X	0	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF	LOW
1	0	1	0	RUN	LOW	RUN	LOW	RUN	RUN	RUN	RUN	RUN	RUN
1	0	1	1	RUN	LOW	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
1	1	1	0	RUN	RUN	RUN	LOW	RUN	RUN	RUN	RUN	RUN	RUN
1	1	1	1	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
0	1	1	1	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	OFF
0	0	1	1	RUN	LOW	RUN	RUN	RUN	RUN	RUN	RUN	RUN	OFF
0	1	1	0	RUN	RUN	RUN	LOW	RUN	RUN	RUN	RUN	RUN	OFF
0	0	1	0	RUN	LOW	RUN	LOW	RUN	RUN	RUN	RUN	RUN	OFF

Table 2

PWR_DN# Timing Diagram

The power down selection is used to put the part into a low power state without turning off control power to the part. PWR-DN# is an asynchronous active low input. This signal needs to be synchronized to affected system functions powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PWR_DN# is active low, all clocks are driven to a low value and held there prior to turning off the VCOs and crystal oscillator. The power up latency is less than 3 mS. The power down latency conforms to the sequence requirements shown below. PCI_STP#, AGP_STP#, and CPU_STP# are considered to be don't cares during the power down operations. The REF and 48_24#MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPU clock (defined as inside the device).
2. As shown, the outputs Stop Low on the next falling edge after PWR_DN# goes low.
3. PWR_DN# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the device.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133 MHz operation. Similar operation will occur when the CPU clock is operating at 100 MHz.

Spectrum Spread Clocking

Down Spread Description

Spread Spectrum is a modulation technique for distributing clock period over a certain bandwidth (called Spread Bandwidth). This technique allows the distribution of the energy (EMI) over a range of frequencies therefore reducing the radiation generated from clocks. As the spread is a percentage of the rested (non-spread) frequency, it is effective at the fundamental and all its harmonics.

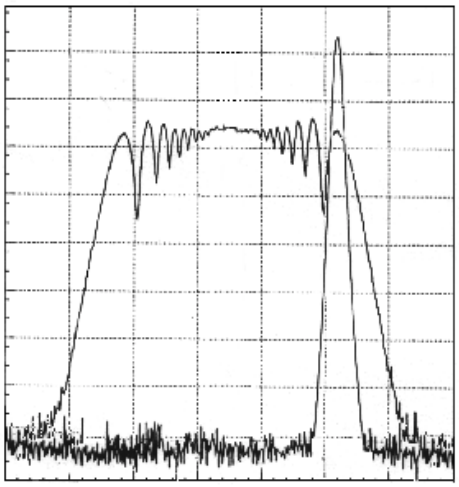


Fig.5A

In this device Spread Spectrum is controlled through SMBus register Byte0, Bit1 and 2. The SMBus register table describes the functionality of these bits.

Two modes of spread spectrum modulation may be chosen. One provides a total frequency deviation from the selected frequency by –0.5% or –0.7% of the selected frequency (downspread). The other selection provides a +/- 0.25% or a +/- 0.35% spread centered at the selected frequency.

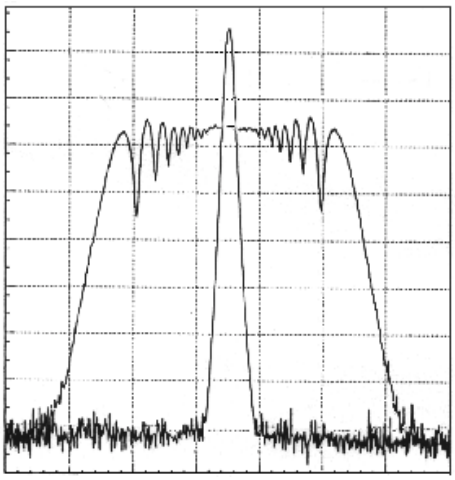


Fig.5B

SMBus Byte0		Byte 5	
Bit2	**Bit1**	**Bit7 (WMBW)**	**Spread**
0	0	0	+/- 0.35
0	0	1	+/- 0.5 (default)
0	1	0	- 0.7
0	1	1	- 0.5
1	0	0	+/- 0.25
1	0	1	Spread off, normal
1	1	0	N/A
1	1	1	Tristate all outputs

2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (see fig6) The device can be read back by using standard SMBus command bytes. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an "acknowledge" is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode. R/W# = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the "acknowledge" (low) signal on the SDATA wire following reception of each byte. If the device should be read then an address **D3** must be sent. Data is transferred MSB first at a max rate of 100kbits/S.
The device will not respond to any other control interface conditions, and previously set control registers are retained.

Serial Control Registers

NOTE: The Pin # column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte , two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2,…) will be valid and acknowledged.

Byte 0: Functionality & Frequency Select Register (default = 0)

Bit	Description								@Pup
	Bit				CPU	SDRAM	AGP	PCI	
	7 (FS3)	6 (FS2)	5 (FS1)	4 (FS0)					
(4:7)	0	0	0	0	66.82	100.23	66.8	33.40	Note 1, 3
	0	0	0	1	100.23	100.23	66.8	33.40	
	0	0	1	0	66.82	66.82	66.8	33.40	
	0	0	1	1	133.64	100.23	66.8	33.40	
	0	1	0	0	66.82	133.64	66.8	33.40	
	0	1	0	1	100.23	133.64	66.8	33.34	
	0	1	1	0	100.23	66.82	66.8	33.40	
	0	1	1	1	133.64	133.64	66.8	33.40	
	1	0	0	0	90.03	90.03	60.0	30.01	
	1	0	0	1	95.02	126.35	63.4	31.67	
	1	0	1	0	105.00	139.71	70.0	35.00	
	1	0	1	1	109.99	109.99	82.4	41.2	
	1	1	0	0	119.75	119.75	59.8	29.94	
	1	1	0	1	126.35	95.02	63.2	31.59	
	1	1	1	0	139.71	105.00	69.8	34.93	
	1	1	1	1	146.22	146.22	73.1	36.56	
Bit3	0 = Frequency is selected by hardware select, latched inputs (pins 1, 11 and 48) 1 = Frequency is selected by Bit 4:7								0
Bit2	00 = +/- 0.5% Center Spread Spectrum 01 = Down Spread Spectrum 0 to –0.5%								00
Bit1	10 = Spread Spectrum modulator off 11 = Tristate all outputs								
Bit0	1 = 48_24#MHz = 48 MHz 0 = 48_24#MHz = 24 MHz								1

Notes:

1. Default at Power-up will be determined by the logic levels present at the bi-directional FS pins, FS3 powers up in a 0 state.
2. @Pup = Power-Up Default.
3. When in test mode, the ratio of TCLK output depends on FS3 to FS0 bit selection. Test mode is enabled when Byte0 bit2 = 1, bit1 = 0, Byte2 bit6 = 0, bit5 = 0, Byte4 bit7 = 0, bit6 = 0, bit5 = 0, Byte5 bit6 = 0, and bit5 = 0.

Byte 1: CPU, 48M Register (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Pin Description
7	1	**27**	48_24#MHz
6	1	11*	FS0
5	1	1*	FS1
4	1	48*	FS2
3	1	-	FS3
2	1	27*	MODE
1	1	43	CPU1
0	1	44	CPU0

Byte 2: PCI Clock Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin#	Pin Description
7	1	11	PCI_F
6	1	-	Reserved
5	1	-	Reserved
4	1	17	PCI5
3	1	16	PCI4
2	1	15	PCI3
1	1	13	PCI2
0	1	12	PCI1

* This pin selection is latched at power up

Byte 3: SDRAM Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin #	Pin Description
7	1	31	SDRAM7
6	1	32	SDRAM6
5	1	34	SDRAM5
4	1	35	SDRAM4
3	1	36	SDRAM3
2	1	38	SDRAM2
1	1	39	SDRAM1
0	1	40	SDRAM0

Byte 4: SDRAM Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin #	Pin Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	19	SDRAM12
3	1	20	SDRAM11
2	1	21	SDRAM10
1	1	22	SDRAM9
0	1	30	SDRAM8

Byte 5: Peripheral, Active/Inactive Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin #	Pin Description
7	1	-	WMBW
6	1	-	Reserved
5	1	-	Reserved
4	1	48	REF0
3	1	1	REF1
2	1	7	AGP0
1	1	8	AGP1
0	1	46	IOAPIC

Byte 6: Reserved Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin #	Pin Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	0	-	Reserved

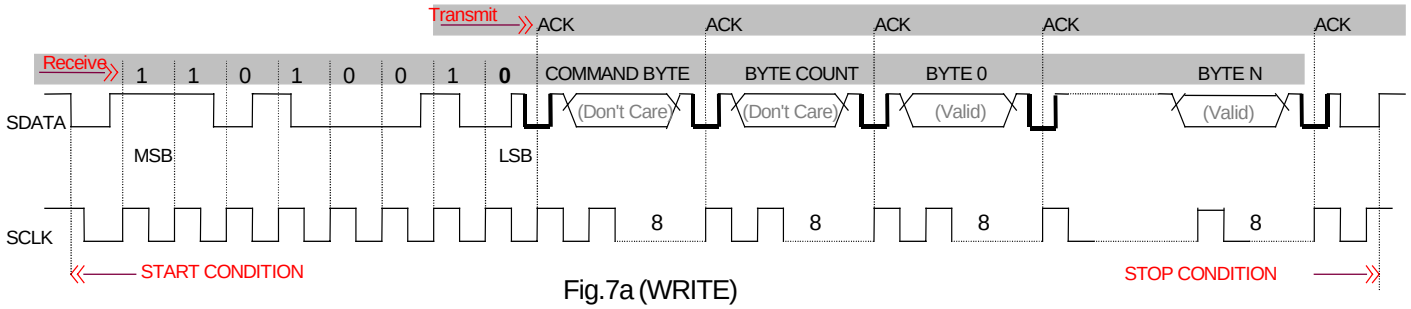


Fig.7a (WRITE)

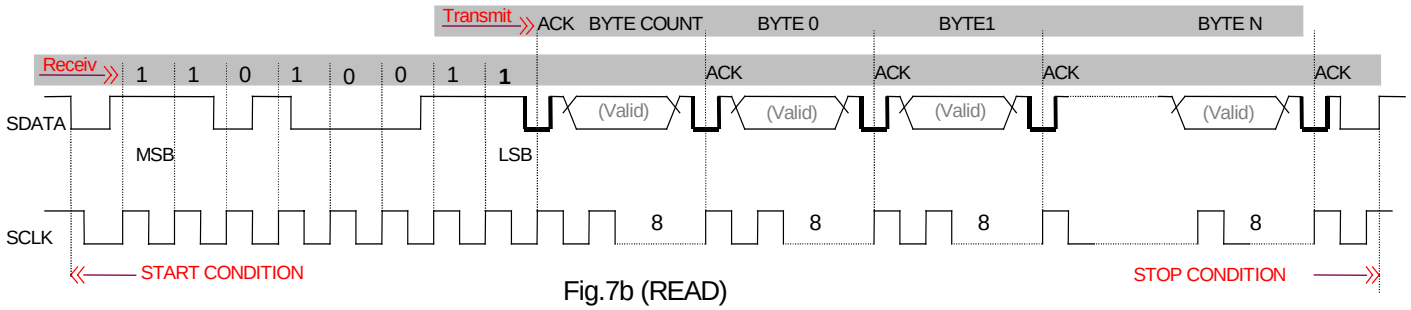


Fig.7b (READ)

Figure 6
SMBus Communications Waveforms

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +70ºC
Maximum ESD protection 2000V
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (VDD = VDDR = VDDL = VDDM = VDDC = 3.3V ±5%, TA = 0ºC to +85ºC)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Current (@Vin = VSS)	IIL	-16		-4	µA	For internal pull up resistors
Input High Current (@Vin = VDD)	IIH	0		5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	300	mA	Note 1
Static Supply Current	Isdd	-	-	400	µA	PWR_DN# = 0, Note 1
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin Inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	32	34	38	pF	Measured from Pin to Ground. Note 2
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
Internal Pull-up and Pull-down resistor value	Rpi	200	250	500	KΩ	

Note1: All outputs loaded as per the maximum capacitive table in this data sheet.
Note2: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.

AC Parameters (VDD = VDDR = VDDP = VDD48 = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +85ºC)

Symbol	Parameter	133.64 MHz CPU		100.23 MHz CPU		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU(0:1) period	7.48	8.0	9.97	10.5	nS	5, 6, 8
THIGH	CPU(0:1) high time	1.87	-	3.0	-	nS	6,10
TLOW	CPU(0:1) low time	1.67	-	2.8	-	nS	6, 11
Tr / Tf	CPU(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	CPU0 to CPU1 Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	CPU(0:1) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	SDRAM(0:12) period	7.48	8.0	9.97	10.5	nS	5, 6, 8
THIGH	SDRAM(0:12) high time	1.87	-	3.0	-	nS	6,10
TLOW	SDRAM(0:12) low time	1.67	-	2.8	-	nS	6, 11
Tr / Tf	SDRAM(0:12) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	Any SDRAM to any SDRAM Skew time	-	250	-	250	pS	
TCCJ	SDRAM(0:12) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	AGP(0:1) period	14.4	15.4	14.4	15.4	nS	5, 6, 8
THIGH	AGP(0:1) high time	5.25	-	5.25	-	nS	6,10
TLOW	AGP(0:1) low time	5.05	-	5.05		nS	6, 11
Tr / Tf	AGP(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	AGP0 to AGP1 Skew time	-	250	-	250	pS	6, 8, 9
TCCJ	AGP(0:1) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	PCI(_F,1:5) period	29.4	-	29.4	-	nS	5, 6, 8
THIGH	PCI(_F,1:5) high time	12.0	-	12.0	-	nS	6,10
TLOW	PCI(_F,1:5) low time	12.0	-	12.0	-	nS	6, 11
Tr / Tf	PCI(_F,1:5) rise and fall times	0.5	2.0	0.5	2.0	nS	6, 7
TSKEW	(Any PCI) to (Any PCI) Skew time	-	500	-	500	pS	6, 8, 9
TCCJ	PCI(_F,1:5) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	48_24MHz period (conforms to +167ppm max)	20.8299	20.8333	20.8299	20.8333	nS	5, 6, 8
Tr / Tf	48_24MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	48_24MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	IOAPIC period	69.841	71.0	69.841	71.0	nS	5, 6, 8
Tr / Tf	IOAPIC rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	IOAPIC Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8, 9
TPeriod	REF(0,1) period	69.841	71.0	69.841	71.0	nS	5, 6, 8
Tr / Tf	REF(0,1) rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	REF(0,1) Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tpLZ, tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tstable	All clock Stabilization from power-up		3		3	mS	12
tss	Stopclock Set Up Time	10.0	-	-	-	nS	14

Group Limits and Parameter (applicable to all settings: Sel133/100# = x)

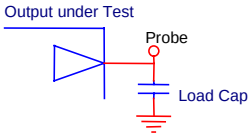
Symbol	Parameter	Min	Typ	Max	Units	Notes
TDC	Duty Cycle	45	50	55	%	6, 8, 9
Toff1	CPU(0:1) to PCI(_F,0:5) offset	1.0	2.0	4.0	nS	6, 8, 9 CPU leads PCI
Toff2	CPU(0:1) to AGP(0:1) offset			500	pS	6, 8, 9

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per table 5 below.
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.7A and Fig.7B)
Note 8: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at 1.25V for 2.5V signals. (see Figs.7A & 7B)
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figs. 7A & 7B)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when both SEL1 And SEL0 are low
Note 14: CPU_STP# and PCI_STP# setup time with respect to any PCI_F clock to guarantee that the effected clock will stop or start at the next PCI_F clock's rising edge.

Output name	Max Load (in pF)
CPU(0:1), IOAPIC	20
PCI(_F,1:5), SDRAM(0:12)	30
48_24#MHz , REF(0:1), AGP(0:1)	20

Table 5.

Test and Measurement Setup



3.3V signals

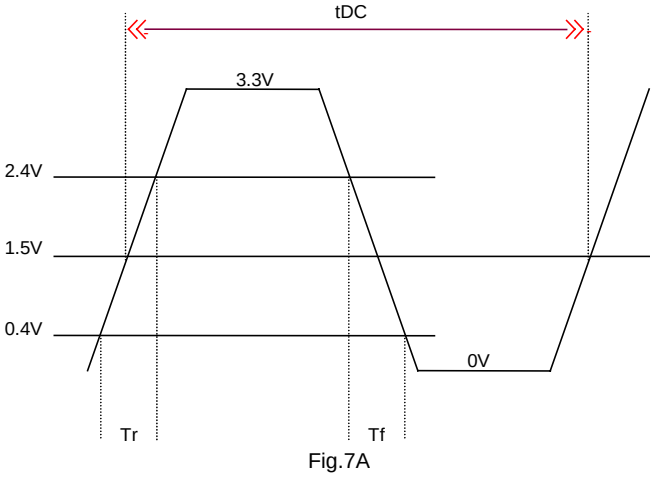


Fig.7A

2.5V signals

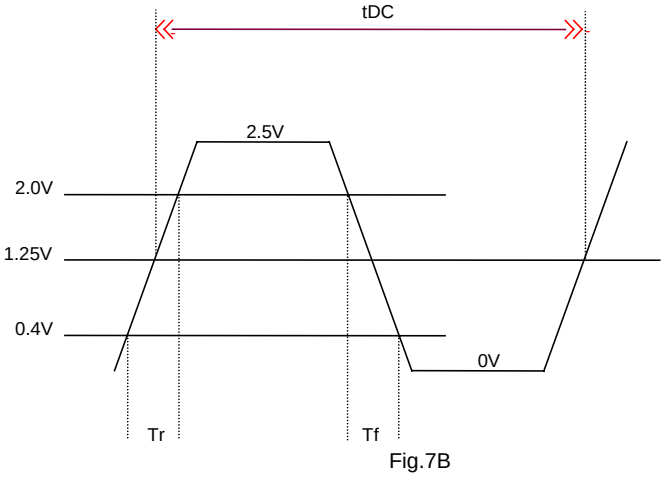


Fig.7B

Output Buffer Characteristics (VDD = VDDR = VDDP = VDD48 = VDD3V66 = 3.3V ±5%, VDDC = VDDC/2 = VDDPIC = 2.5 ± 5%, TA = 0ºC to +85ºC)

Buffer Characteristics for CPU (0:1), IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-12			mA	Vout=VDDC-0.5 Volts
Pull-Up Current	IOH_2	-26			mA	Vout=1.2 Volts
Pull-Down Current	IOL_1	12			mA	Vout=0.4 Volts
Pull-Down Current	IOL_2	27			mA	Vout=1.2 Volts
Output Impedance	Z0	13.5		45	Ω	

Buffer Characteristics for SDRAM(0:12)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-72			mA	Vout=VDDC-0.5 Volts
Pull-Up Current	IOH_2	-68			mA	Vout=1.4 Volts
Pull-Down Current	IOL_1	23			mA	Vout=0.4 Volts
Pull-Down Current	IOL_2	64			mA	Vout=1.5 Volts
Output Impedance	Z0	10		25	Ω	

Buffer Characteristics for PCI(F, 1:5), AGP(0:1)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-33			mA	Vout=VDDC-0.5 Volts
Pull-Up Current	IOH_2	-30			mA	Vout=1.4 Volts
Pull-Down Current	IOL_1	9.4			mA	Vout=0.4 Volts
Pull-Down Current	IOL_2	28			mA	Vout=1.5 Volts
Output Impedance	Z0	12		55	Ω	

Buffer Characteristics for 48_24 MHz and Ref(0:2)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-27			mA	Vout=VDDC-0.5 Volts
Pull-Up Current	IOH_2	-27			mA	Vout=1.4 Volts
Pull-Down Current	IOL_1	9			mA	Vout=0.4 Volts
Pull-Down Current	IOL_2	26			mA	Vout=1.5 Volts
Output Impedance	Z0	20		60	Ω	

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	18	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 36pF
In order to meet the specification for CL = 16pF following the formula:

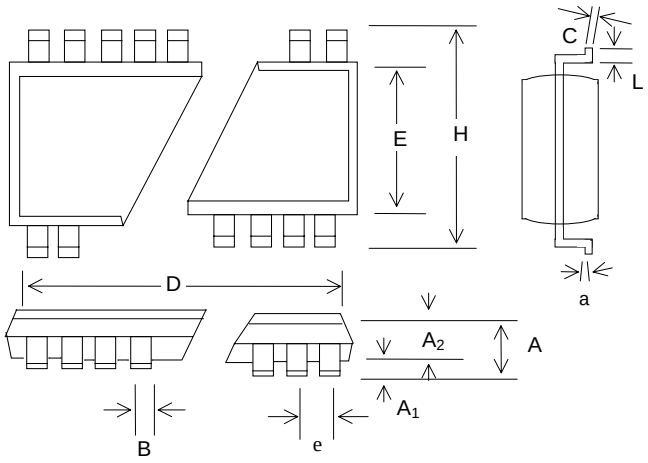
$$C_L = \frac{C_{XIN} x C_{XOUT}}{C_{XIN} + C_{XOUT}}$$

Then the board trace capacitance between Xin and the crystal should be no more than 2pF. (same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 32pF. Similarly the total capacitance between the crystal and Xout will be 32pF. Hence using the above formula:

$$C_L = \frac{32\,pF x 32\,pF}{32\,pF + 32\,pF} = 16\,pF$$

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	0.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.630	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.635 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.020	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

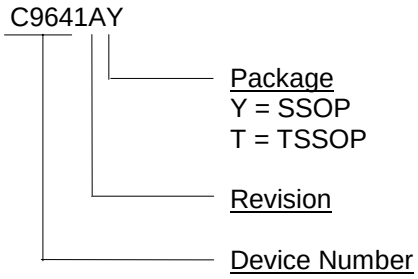
48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9641AY	48 PIN SSOP	Commercial, 0ºC to +70ºC
C9641AT	48 PIN TSSOP	Commercial, 0ºC to +70ºC

Marking: Example: Cypress
C9641AY
Date Code, Lot #



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Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106965	06/12/01	IKA	Convert from IMI to Cypress