C9726

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

Approved Product

Product Features

- 1 differential pair and 1 single ended open drain CPU clocks
- 6 PCI clocks
- 2 REF (3.3V) clocks at 14.318 MHz
- 1 48 MHz (3.3V), and one 24/48 MHz clock
- Power Management through PWR_DN#
- 13 SDRAM clocks for 3 DIMMs
- Cypress Spread Spectrum for best EMI reduction
- 8 Spread Spectrum settings each frequency
- 48 Pin SSOP Package
- SMBUS clock control with readback capability
- Fine resolution frequency programming via Dial-a-Frequency® Function

Product Description

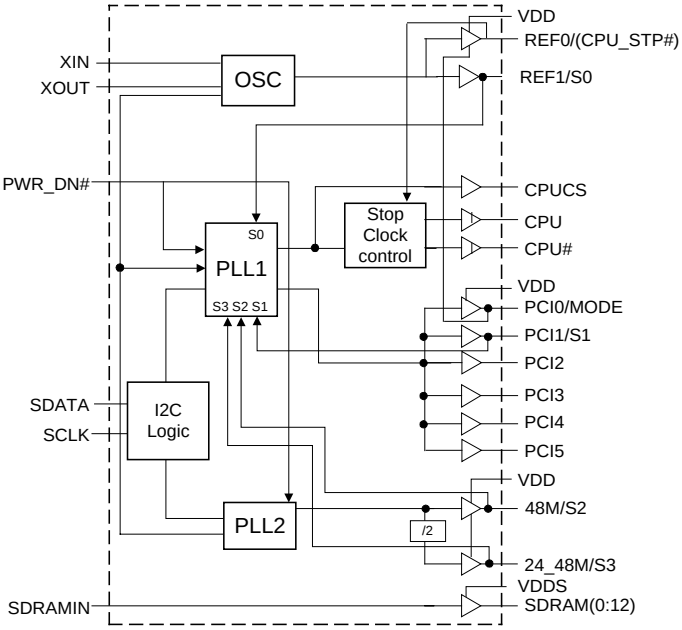
The C9726 is a main clock synthesizer chip for VIA VT8371 (KX133) chipset and AMD Athlon (K7) CPU based systems. This device provides all clocks required with spread spectrum for EMI reduction. It also includes a comprehensive SMBUS control interface to permit individual clock enable, frequency, and spread controls via system software.

Frequency Table

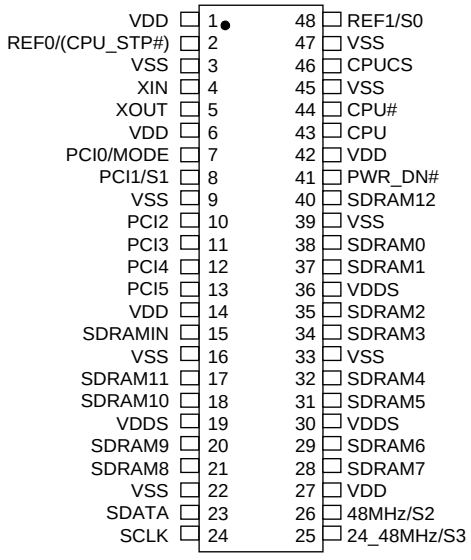
S3	S2	S1	S0	CPU	PCI	Spread Spectrum
1	1	1	1	133.3	33.3	+/- .5%
1	1	1	0	75	37.5	+/- .5%
1	1	0	1	100.2	33.3	+/- .5%
1	1	0	0	66.8	33.4	+/- .5%
1	0	1	1	79	39.5	OFF
1	0	1	0	110	36.7	OFF
1	0	0	1	115	38.3	OFF
1	0	0	0	120	30	OFF
0	1	1	1	133.3	33.3	OFF
0	1	1	0	83.3	27.7	OFF
0	1	0	1	100.2	33.3	OFF
0	1	0	0	66.8	33.4	OFF
0	0	1	1	124	31.0	OFF
0	0	1	0	129	32.3	OFF
0	0	0	1	138	34.5	OFF
0	0	0	0	143	35.8	OFF

Table 1

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	TYPE	Description
2	**REF0 / CPU_STP#**	I/O	This is a bi-directional pin with an internal pull-up. The direction of this pin is determined by the state of signal MODE (pin 7). If Mode = 0, this pin is a CPU_STP# input pin. When CPU_STP# is asserted low, CPU and CPU-OD are forced LOW and CPU# is in Tristate. If Mode = 1, this pin is REF0, a buffer output of the signal applied at Xin.
4	**XIN**	I	This is the input pin to the crystal oscillator, which is an internal amplifier. It is typically connected to a parallel resonant crystal. It may also be driven from an alternative clock source.
5	**XOUT**	O	This is the output pin of the crystal oscillator, which is an internal amplifier. It is typically connected to a parallel resonant crystal. If Xin is driven from an alternative clock source, then this pin should be unconnected.
7	**PCI0 / MODE**	I/O	This is a power on bi-directional strapping pin with an internal pull-up (see app note, page 4). During power up, this pin is an input “Mode” for setting the direction of Pin 2. When the power reaches the rail, this pin becomes a PCI0 clock output.
8	**PCI1 / S1**	I/O	This is a power on bi-directional strapping pin with an internal pull-up (see app note, page 4). During power up, this pin is an input “S1” for frequency selection, see table 1, p.1. When the power reaches the rail, this pin becomes a PCI1 clock output.
10,11,12,13	**PCI(2:5)**	OUT	PCI clock outputs. Synchronous to CPU clocks.
15	**SDRAMIN**	IN	LVTTL Input pin to the SDRAM(0:12) distribution buffers.
40,38,37,35, 34,32,31,29, 28,21,20,18,17	**SDRAM (0:12)**	OUT	SDRAM Buffered Outputs. They are buffered outputs of the signal applied at SDRAMIN. When PWR_DN# is low. These signals are forced low regardless of the signal at SDRAMIN.
23	**SDATA**	I/O	Serial data input pin. Conforms to the SMBUS specification of a Slave Receiver/Transmitter device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting. See SMBUS function description, p.8.
24	**SCLK**	I	Serial clock input pin. Conforms to the SMBUS 100KHz Specification
25	**24_48MHz / S3**	I/O	This is a power on bi-directional strapping pin with an internal pull-down (see app note, page 4). During power up, this pin is an input “S3” for frequency selection, see table 1, p.1. When the power reaches the rail, this pin becomes a SIO clock output programmed to 24MHz or 48MHz via byte3, bit6 in the SMBUS table. It defaults to 24MHz.
26	**48MHz / S2**	I/O	This is a power on bi-directional strapping pin with an internal pull-up (see app note, page 4). During power up, this pin is an input “S2” for frequency selection, see table 1, p.1. When the power reaches the rail, this pin becomes a 48MHz, USB clock output.
41	**PWR_DN#**	IN	LVTTL input with an internal pull-up. When this pin is asserted low, the device is in power down condition, all clocks are stopped in a Low state except CPU# will be in tristate.
43, 44	**CPU, CPU#**	O	Open Drain Differential CPU outputs. They require external pull-up to 1.5V. See table 1 page 1 for frequency selection.
46	**CPUCS**	O	3.3V Host clock output for driving the chipset. It is in phase with CPU clock (pin 43).
48	**REF1 / S0**	IN/OUT	This is a power on bi-directional strapping pin with an internal pull-up (see app note, page 4). During power up, this pin is an input “S0” for frequency selection, see table 1, p.1. When the power reaches the rail, this pin becomes a REF1, a buffered clock output of the signal applied at Xin.
1,6,14,27, 42	**VDD**	PWR	Common 3.3V Power Supply.
19, 36, 30	**VDDS**	PWR	Power supply for SDRAM. Nominally 3.3V
3, 9, 16, 22, 33, 39, 45, 47	**VSS**	GND	Ground

Power on Bi-Directional Pins

Please see App Note AN-0021 for a description on the Power-On Bi-Directional Pins and strapping resistor options

Power Management Functions

Power Management on this device is controlled by CPU_STP# (pin2) and PWR_DN# (pin41).

When CPU_STP# is forced low, all CPU signals are synchronously (no glitch) disabled to a low state and CPU# signals are in tristate. The CPU_STP# signal does not directly gate the CPU clocks, the CPU clocks will toggle one to three complete cycles before stopping on a falling edge. When CPU_STP# is released to high, the CPU clocks are synchronously re-enabled. The clocks will wait the equivalent of one to three cycles after CPU_STP# is asserted high then will start toggling on the rising edge.

When PWR_DN# is forced low, CPU-OD, CPU, PCI(0:5), SDRAM(0:12), 48MHz, 48_24MHz, and REF(0:1) signals are synchronously forced low (CPU# is placed in tristate), all internal circuitry (including the crystal buffer) is shutdown and the device is placed in low power (or in power down) mode. After PWR_DN# is forced low, all power supplies (3.3V and 2.5V) may be removed. All power supplies must be re-applied 200mS before releasing PWR_DN# (to high), consequently, the device must then be allowed 1mS before the clock outputs settle to their preset frequencies. (see Fig.1, and table 2 below)

Power Management Timing

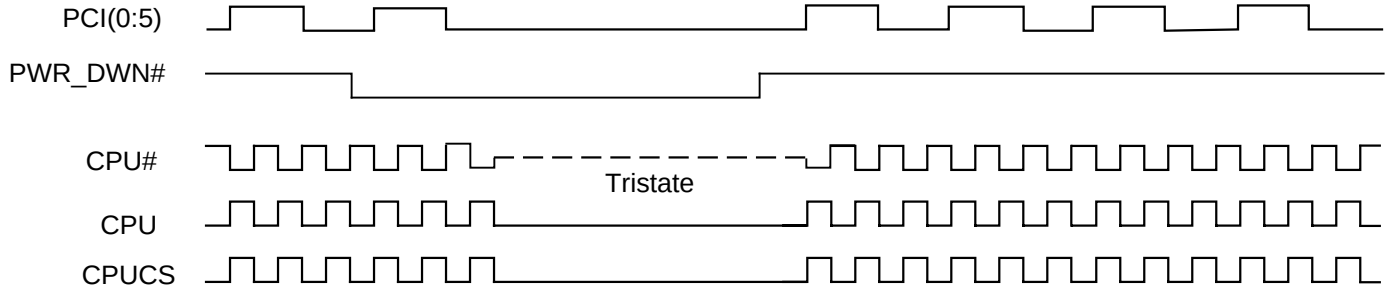

Fig. 1

All functionality is referenced to the edge of PWR_DN#. If the tss timing is met, with respect to the next occurring PCI_F low to high transition, then all clocks that are controlled by CPU_STP# are guaranteed to stay low (stopped) or to rise (run) at the next rising edge of PCI_F. See the AC parameters for tss time. CPU# clocks are stopped in a high state.

Power Management Function Table

CPU_STP#	PWR_DN#	CPUCS	CPU	CPU#	REF(0:1)	PCI(0:5)	48M, 48_24M	SDRAM (0:12)	XTAL, PLLS
X	0	LOW	LOW	Hi-Z	LOW	LOW	LOW	LOW	OFF
0	1	LOW	LOW	Hi-Z	RUN	RUN	RUN	RUN	RUN
1	1	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN

Table 2

Power Down Timing

Power down (asserting the PWR_DN# pin) is an asynchronous event in the device. When PWR_DN is brought low, the device internally removes power from all control logic. All outputs are driven to a logic low level. The exception is the CPU# pins which are released to a high (floating) state. It is the designer's responsibility to ensure all system timing and sequencing needs are met before applying and releasing this pin. It is intended to be used as a system power savings feature and will put the device into its lowest power consumption mode while still retaining the minimum control logic functionally needed to produce an orderly startup when PWR_DN# is released to a high state.

Spectrum Spread Clocking

See Ap Note AN-0024 for a description on Spectrum Spread Clocking.

SBW2	SBW1	SBW0	Spread
0	0	0	± 0.25%
0	0	1	± 0.12%
0	1	0	± 0.37%
0	1	1	± 0.50%
1	0	0	- 0.50%
1	0	1	- 0.25%
1	1	0	- 0.75%
1	1	1	+ 0.25%, - 0.75%

Table 3

2-Wire SMBUS Control Interface

See Ap Note AN-0022 for a description on 2-Wire SMBUS Control Interface

Serial Control Registers

NOTE: The Pin # column lists the affected pin number where applicable. The @Pup column gives the state of the control register at power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2,…) will be valid and acknowledged.

Serial Control Registers (Cont.)

Byte 0: Frequency Control Register (1 = Enable, 0 = Low)

Bit	@Pup	Pin#	Pin Description
7	1	-	Spread Spectrum extension (1= on, 0 = off) see table 4, pg. 10
6	0	-	S2
5	0	-	S1
4	0	-	S0
3	0	-	1 = enable byte 0, bits 6, 5, 4, 2, 1 for frequency selection table 4
2	0	-	S4
1	0	-	S3
0	0	-	See Table 3 below

Byte 1: CPU / SDRAM Clock Register (1=Enable, 0=Low)

Bit	@Pup	Pin#	Pin Description
7	0	-	SBW2 (See SST Page 6, Table 3)
6	0	-	SBW1 (See SST Page 6, Table 3)
5	0	-	SBW0 (See SST Page 6, Table 3)
4	0	-	DASO (See Table 5)
3	1	40	SDRAM12
2	0	-	DAS1 (See Table 5)
1	1	43,44	CPU,CPU# (0 = disabled, CPU in low and CPU# in Hi-Z mode)
0	1	46	CPUCS

Byte0, Bit 7	Byte0, Bit 0	Modes
0	0	Normal operation
0	1	Tri-state
1	0	Spread Spectrum On
1	1	Test mode (Spread Spectrum On)

Table 4

DAS(1:0)		Skew	Description
0	0	Default	Applicable to CPUCS
0	1	- 100 ps	
1	0	- 200 ps	
1	1	+ 200 ps	

Table 5

Serial Control Registers (Cont.)

Byte 2: PCI Control Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin#	Pin Description
7	0	-	Reserved
6	1	7	PCI0
5	0	-	Reserved
4	1	13	PCI5
3	1	12	PCI4
2	1	11	PCI3
1	1	10	PCI2
0	1	8	PCI1

Byte 3: SDRAM Control Register (1=Enable, 0=Stopped)

Bit	@Pup	Pin#	Pin Description
7	0	-	Reserved
6	0	25	0 = output 24MHz. 1 = output 48MHz.
5	1	26	48MHz
4	1	25	24_48MHZ
3	0	-	Reserved
2	1	17,18,20,21	SDRAM(8:11)
1	1	28,29,31,32	SDRAM(4:7)
0	1	34,35,37,38	SDRAM(0:3)

Byte 4: Dial-a-Frequency® Register

Bit	@Pup	Pin#	Pin Description
7	0	-	N7, MSB
6	0	-	N6
5	0	-	N5
4	0	-	N4
3	0	-	N3
2	0	-	N2
1	0	-	N1,
0	0	-	N0, LSB

Byte 5: Register

Bit	@Pup	Pin#	Pin Description
7	0	-	S3 Readback
6	0	-	S2 Readback
5	0	-	S0 Readback
4	0	-	MODE Readback
3	0	-	S1 Readback
2	0	-	Reserved
1	1	46	REF1
0	1	2	REF0

Byte 6: Reserved Register

Bit	@Pup	Pin#	Pin Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

Byte 7: Dial-a-Frequency® Register

Bit	@Pup	Pin#	Pin Description
7	0	-	R6, MSB
6	0	-	R5
5	0	-	R4
4	0	-	R3
3	0	-	R2
2	0	-	R1
1	0	-	R0, LSB
0	0	-	Enable SMBUS N&R

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Frequency Selection Table

Input Conditions					Output Frequency		Spread%	
Data Byte 0, Bit 3 = 1								
Bit2 S4	Bit 1 S3	Bit 6 S2	Bit 5 S1	Bit 4 S0	CPU	PCI	Byte0, Bit7 = 0	Byte0, Bit7 = 1
1	1	1	1	1	133.3	33.3	+/-0.5	See table 3, Page 6
1	1	1	1	0	75	37.5	+/-0.5	See table 3, Page 6
1	1	1	0	1	100.2	33.3	+/-0.5	See table 3, Page 6
1	1	1	0	0	66.8	33.4	+/-0.5	See table 3, Page 6
1	1	0	1	1	79	39.5	OFF	See table 3, Page 6
1	1	0	1	0	110	36.7	OFF	See table 3, Page 6
1	1	0	0	1	115	38.3	OFF	See table 3, Page 6
1	1	0	0	0	120	30	OFF	See table 3, Page 6
1	0	1	1	1	133.3	33.3	OFF	See table 3, Page 6
1	0	1	1	0	83.3	27.7	OFF	See table 3, Page 6
1	0	1	0	1	100.2	33.3	OFF	See table 3, Page 6
1	0	1	0	0	66.8	33.4	OFF	See table 3, Page 6
1	0	0	1	1	124	31.0	OFF	See table 3, Page 6
1	0	0	1	0	129	32.3	OFF	See table 3, Page 6
1	0	0	0	1	138	34.5	OFF	See table 3, Page 6
1	0	0	0	0	143	35.8	OFF	See table 3, Page 6
0	1	1	1	1	85	28.3	OFF	See table 3, Page 6
0	1	1	1	0	87.5	29.2	OFF	See table 3, Page 6
0	1	1	0	1	90	30	OFF	See table 3, Page 6
0	1	1	0	0	92.5	30.8	OFF	See table 3, Page 6
0	1	0	1	1	95	31.7	OFF	See table 3, Page 6
0	1	0	1	0	147	36.8	OFF	See table 3, Page 6
0	1	0	0	1	152	30.4	OFF	See table 3, Page 6
0	1	0	0	0	154	30.8	OFF	See table 3, Page 6
0	0	1	1	1	157	31.4	OFF	See table 3, Page 6
0	0	1	1	0	159	31.8	OFF	See table 3, Page 6
0	0	1	0	1	162	32.4	OFF	See table 3, Page 6
0	0	1	0	0	166	33.2	OFF	See table 3, Page 6
0	0	0	1	1	171	34.2	OFF	See table 3, Page 6
0	0	0	1	0	180	36	OFF	See table 3, Page 6
0	0	0	0	1	190	38	OFF	See table 3, Page 6
0	0	0	0	0	200	40	OFF	See table 3, Page 6

Table 6.

Dial-a-Frequency® Feature

See Ap Note AN-0025 for a description of the Dial-a-Frequency® Feature

P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (S3, S2, S1, S0) or through the software selectors (byte0, bits 6,5,4,2,1). P value may be determined from the following table:

Dial-a-Frequency® Feature (Cont.)

S(4:0)	P
0100X, 00XXX	96016000
01010, 100XX, 10111,11000,11111	64010666.67
01011, 011XX, 10101, 10110, 11001, 1101X, 11101, 11110	48008000
10100, 11100	38406400

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65ºC to + 150ºC

Operating Temperature: 0ºC to +85ºC

Maximum ESD protection 2000V

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	For internal Pull up resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH			5	µA	
Input Low Current (@VIL = VSS)	IIL			-5	µA	For internal Pull down resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH	66		5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	260	mA	S(3:0) = 0111, Note 4
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	30	36	34	pF	Measured from Pin to VSS. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD = 3.3V ±5%, TA = 0° to +70°C						

Note1: Pull-down applicable to pin 25 (S3). Pull-up applicable to pins 2, 7, 8, 26, 41, 48.
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-down/up resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note4: All outputs loaded as per table 5 below.
Note5: Although the device will reliably interface with crystals of a 15pF – 20pF C_L range, it is optimized to interface with a typical C_L = 16pF crystal specifications.

Clock Name	Max Load (in pF)
CPU, REF	20
PCI, SDRAM	30
24MHz, 48MHz	15

Table 5

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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AC Parameters

Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU, CPU#, CPUCS period	7.5	8.0	9.98	10.5	nS	5, 6, 8
Tf	CPU, CPU#, CPUCS fall times	1	-	1	-	V/nS	6
TSKEW0	CPU to CPUCS Skew time	-	-300	-	-300	pS	6, 8, 9,14
TCCJ	CPU Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
Toff	CPUCS to any PCI	1	4	1	4	nS	8
TPeriod	SDRAM[0:12] period	7.5	8.0	10.0	10.5	nS	5, 6, 8
THIGH	SDRAM[0:12] high time	1.87	-	3.0	-	nS	6,10
TLOW	SDRAM[0:12] low time	1.67	-	2.8	-	nS	6, 11
Tr / Tf	SDRAM[0:12] rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TDelay	SDRAMIN to Any SDRAM[0:12]	-	3.5	-	3.5	nS	6, 8, 9
TSKEW1	Any SDRAM to Any SDRAM	-	250	-	250	pS	6, 8, 9
TCCJ	SDRAM[0:12] Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	PCI(0:5) period	29.93	-	29.94	-	nS	5, 6, 8
THIGH	PCI(0:5) period	12.0	-	12.0	-	nS	6,10
TLOW	PCI(0:5) low time	12.0	-	12.0	-	nS	6, 11
Tr / Tf	PCI(0:5) rise and fall times	0.5	2.0	0.5	2.0	nS	6, 7
TSKEW2	(Any PCI clock) to (Any PCI clock)	-	500	-	500	pS	6, 8, 9
TCCJ	PCI(0:5) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	48MHz period (conforms to +167ppm max)	20.8299	20.8333	20.8299	20.8333	nS	5, 6, 8
Tr / Tf	48MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	48MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	24MHz period	41.6598	41.6666	41.6598	41.6666	nS	5, 6, 8
Tr / Tf	24MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	24 MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	REF(0:1) period	69.8413	71.0	69.8413	71.0	nS	5, 6, 8
Tr / Tf	REF(0:1) rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	REF(0:1) Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tpLZ, tpHZ	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tstable	All clock Stabilization from power-up		3		3	mS	12

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per table 5.
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V. (see fig.7.)
Note 8: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals (fig.7) and as in fig.9 for differential CPU clocks
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals (see fig.7)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when Byte0, bit0 is toggled.
Note14: CPUCS leads.

Test and Measurement Setup for Non Differential Clocks

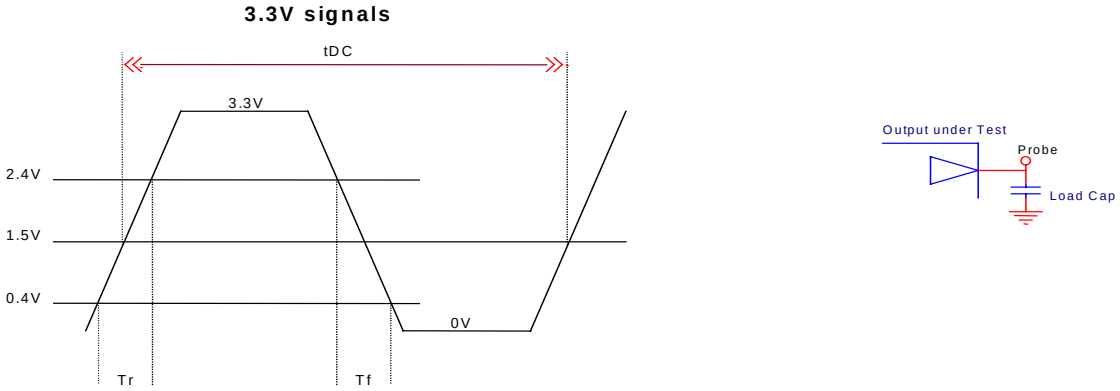

Fig.8

Test and Measurement Setup for CPU Differential Clocks

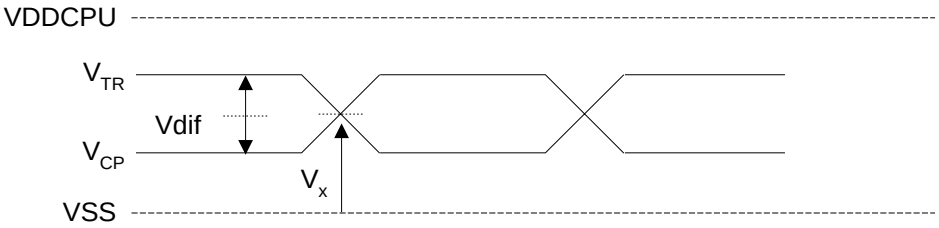

Fig. 9

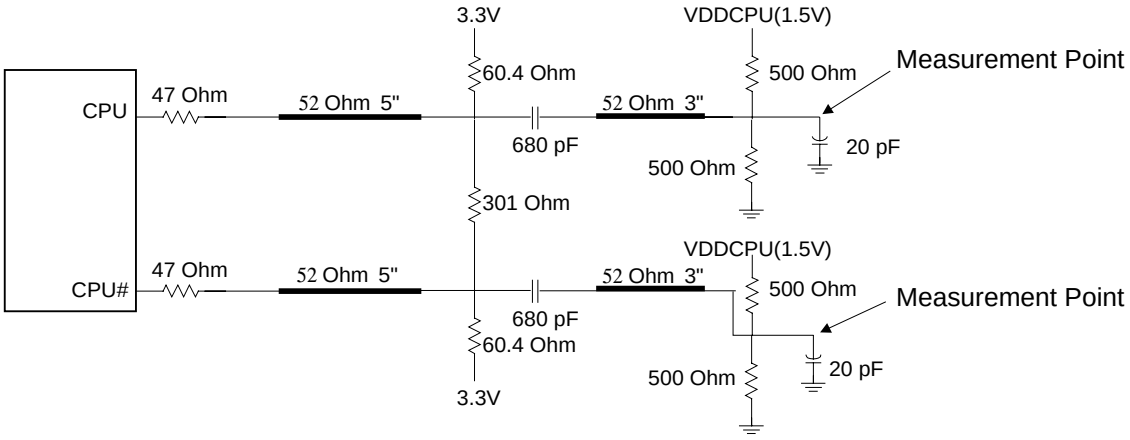

Fig. 10

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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Output Buffer Characteristics

CPU, CPU#

		CPU = 100M			CPU = 133M				
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Low Current	I_{OL}	18	23						V_{DL} = 0.3V
Output Rise Edge Rate	t_r		1.0			1.0		V/ns	
Output Fall Edge Rate	t_f		1.0			1.0		V/ns	
Duty Cycle	t_D	45		55	45		55	%	Measured at 50% point
Jitter, Cycle to Cycle	t_{JC}			250			250	ps	
Output Skew	t_{SK}		TBD			TBD			Measured on rising edge at 750mV
AC Output Impedance	Z_O		50			50		Ω	$V_O = V_X$

PCI(0:5)

Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH_1	-33	-58	-194	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	12		55	Ω	

24MHz, 48MHz, and REF(0:1)

Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH_1	-29	-46	-99	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	20		60	Ω	

SDRAM(0:12), CPUCS

Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH_1	-72	-116	-198	mA	Vout =VDD - 1. 0 V
Pull-Up Current	IOH_2	-68	-110	-188	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	10		24	Ω	

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
	T_A	-	-	5	PPM	Ageing (first year @ 25C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

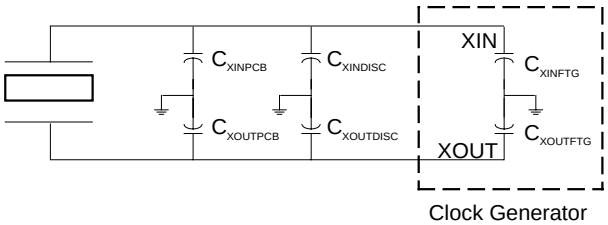
Note 2: Larger values may cause this device to exhibit oscillator startup problems

To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit traces (C_{PCB}), and any onboard discrete load capacitors (C_{DISC}).
The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

- C_{XTAL} = the load rating of the crystal
- $C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
- $C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
- C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
- $C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
- $C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
- $C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground



As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF.

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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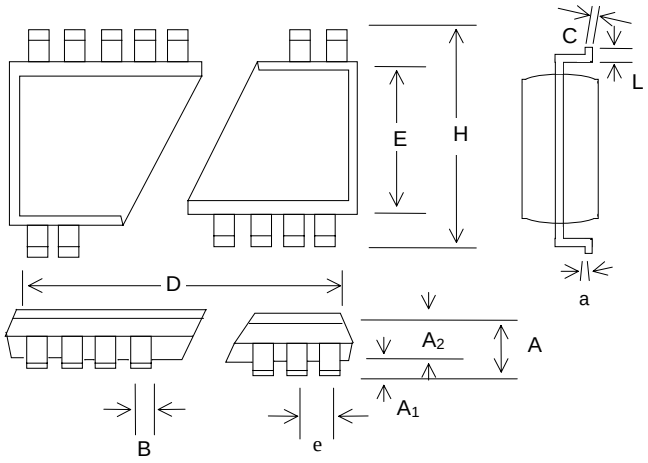
Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9726A	48 Pin SSOP	Commercial, 0ºC to +70ºC

Marking: Example: IMI
C9726A
Date Code, Lot #

C9726AY

Package
Y = SSOP

Revision

Device Number

Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems

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Document Title: C9726 Clock Generator for VIA VT8371/Athlon (K7) Chipset Systems Document Number: 38-07047				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109130	08/29/01	NDP	Convert from IMI to Cypress