NEC Electronics Inc.

CB-C10
2.5-Volt, 0.25-Micron (drawn) CMOS Cell-Based ASIC

Preliminary

March 1997

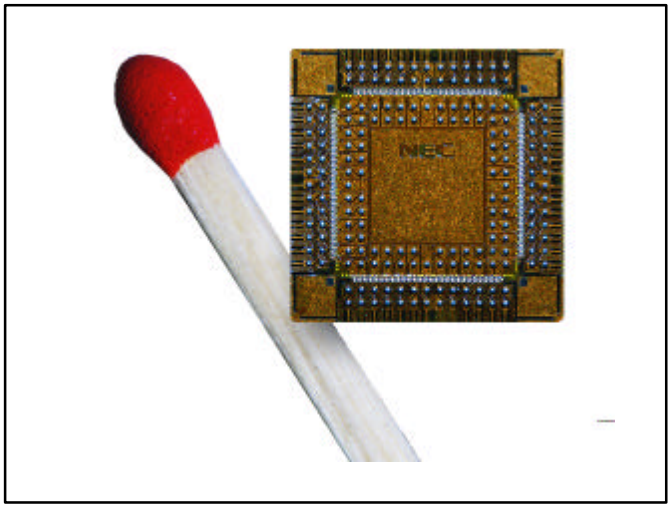
Description

NEC's 0.25 µm drawn (0.18 µm L-effective) CB-C10 family incorporates ultra-high-performance cores with deep sub-micron process technology for high-end applications requiring high speeds, high integration density, and low power dissipation.

The cell-based approach allows the most effective realization of true "system-on-silicon" applications. These system-level ASICs may be composed of user-defined logic, high-density memory, cores such as CPUs and DSPs, intelligent peripherals, and analog functions.

The I/O structure of CB-C10 allows a flexible adaptation to the system requirements at a minimum die size. State-of-the-art interface macros for high-speed or special signaling standards are also supported, including HSTL, GTL+, PCI and IEEE1394.

Figure 1. Chip Size Package (CSP)



Process

CB-C10 designs are manufactured with NEC's advanced titanium-silicide (Ti-Si) process and may use between three and five metal layers (Al) for routing. The CB-C10 ASIC family offers the highest flexibility for power routing, split power supply lines, and other customer-specific requirements.

Applications

Power-sensitive applications such as mobile communication and mobile computing systems can benefit from the extremely low power dissipation of 43 nW/MHz/gate at a 2.5-volt supply voltage. This value is reduced further to 22 nW/MHz/gate in the upcoming 1.8V library version.

The CB-C10 family is also ideal for high-volume products, including consumer products, telecommunications equipment and high-performance graphics workstations.

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Table 1. CB-C10 Series Features and Benefits

CB-C10 Series Features	CB-C10 Series Benefits
• 0.25 µm drawn (0.18 µm L-effective) CMOS process	⇒ Ultra-high density cell structure with high performance
• Extensive support of state-of-the-art cores and interfaces	⇒ Cost effective system-on-silicon solutions
• Available gate counts from 597K to 21.3 million gates	⇒ Support for a wide range of high complexity systems
• Low power dissipation of 43 nW/MHz/gate @ 2.5V	⇒ New application possibilities for low power system solutions
• Optimized 2.5V architecture (operates down to 1.8V)	⇒ Highest speed at ultra-low power consumption
• Analog macro support such as DACs, ADCs, APLL, etc.	⇒ Mixed-signal design options
• Ultra-high pin count using 40 µm pad pitch	⇒ Increased I/O density to achieve smaller die sizes
• Special power rail structure, multi-oxide process	⇒ Mixed 2.5V and full-swing 3.3V I/O for full system compatibility
• Flexible I/O structure supports LVDS, HSTL, GTL+, PCI, etc.	⇒ Effective adaptation to today's system requirements
• Advanced packages such as TapeBGA, Flip Chip+BGA, etc.	⇒ Cost-effective and state-of-the-art packaging
• NEC's OpenCAD® design environment	⇒ Flexible design flow for short design times

Table 2. Product Outline

Step		B86	C24	C62	D01	D39	D78	E16	E54	E93	F31	F70	G08	G46	G85
Available gates (1)		597K	777K	980K	1.2M	1.45M	1.72M	2.02M	2.33M	2.67M	3.04M	3.42M	3.83M	4.26M	4.72M
Pad count (2)		300	348	396	444	492	540	588	636	684	732	780	828	876	924
Step		H23	H62	J00	J38	J77	K15	K54	K92	L30	L69	M07	M46	M84	S58
Available gates (1)		5.20M	5.70M	6.23M	6.77M	7.35M	7.94M	8.56M	9.20M	9.86M	10.6M	11.3M	12.0M	12.7M	21.3M
Pad count (2)		972	1020	1068	1116	1164	1212	1260	1308	1356	1404	1452	1500	1548	2016
Toggle frequency (min.)		1.6 GHz													
Delay time	Internal	31.5 ps (F/O = 2, L = 0 mm); 93.4 ps (F/O = 1, L = 0.5 mm) (F322)													
	Input	79.7 ps (F/O = 2, L = 0 mm) (FI01)													
	Output	1.363 ns (C_L = 50 pF) (FO02)													
Consumed power	Internal	43 nW/MHz/gate (2.5V); 23 nW/MHz/gate (1.8V)													
	Input	1.66 µW/MHz (F/O = 2, L = 0 mm)													
	Output	167 µW/MHz (C_L = 15 pF)													
Power supply voltage		2.5V ± 0.2V (operation down to 1.8V possible)													
Operating temperature		-40 to +85°C													
Interface level		2.5V / 3.3V CMOS level, LVTTL level, GTL+, HSTL, PCI, pECL													
Technology		Standard cell 0.25 µm (0.18 µm L-effective) silicon gate CMOS: 3, 4 or 5* metal layers													

Notes:

(1) Utilization depends on the content and conditions of each design. Typical utilization may be 65% for 3LM, and 70% for 4LM. One gate is equivalent to one 2-input NAND gate. Number of available gates assumes 3 grids per gate.

(2) Total pad count, including power and ground pins.

*5th metal layer used for flip-chip packaging

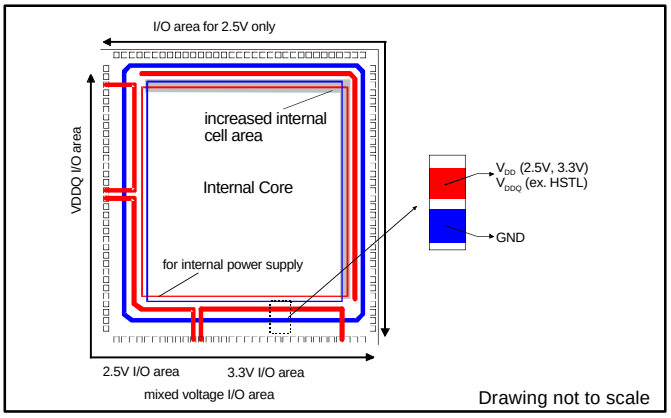
Interface Macro Support

The CB-C10 interface area is realized by using cell-based structures that provide a variety of interface options, including both 2.5-volt and 3.3-volt full-swing interface buffers.

For special applications, several high-speed I/O buffer types are available. These include 3.3-volt PCI cells, AGP for 66 MHz and 133 MHz applications, GTL (Gunning Transceiver Logic), HSTL (class 1,2,3,4) and pseudo-ECL (pECL) buffers. These high-speed buffers are available for special applications. Table 3 summarizes the available interface options.

2.5-Volt / 3.3-Volt Mixed I/O Interfacing. Although CB-C10 is a 2.5-volt optimized technology with thin gate oxide, NEC offers 3.3-volt-compatible I/O interfacing. The full-swing 3.3-volt interfacing is achieved through a multi-oxide process in the I/O area. The buffers for 2.5-volt / 3.3-volt interface levels can be mixed. This is supported by the special power rail structure shown in Figure 2.

Figure 2. Example for Power Rail Option



HSTL / PCI Interfacing. A third power rail (V_{DDQ}) is available for interface types that require a reference voltage (such as HSTL, GTL+, and AGP). These buffers may also be located anywhere in the I/O area.

Table 3. CB-C10 I/O Buffer Types

Buffer Type	Options and Possible Combinations
Standard I/O Interface Buffers	Pull-up 50 kΩ, 5 kΩ / Pull-down 50 kΩ Schmitt Trigger input Fail-safe LVCMOS / LVTTL level Output buffers: Open drain, tri-state Tri-state Low noise (slew-rate controlled) Driveability: 2.5V interface: 3, 6, 9, 12, 18, 24 mA/slot 3.3V interface: 3, 6, 9, 12 mA/slot
High-Speed I/O Buffers	PCI (3.3V, up to 64 bit / 66 MHz) GTL / GTL+, pECL, HSTL, SSTL, LVDS* AGP, IEEE1394*, USB*

Note: *Under development. Please check the availability of the advanced interfaces with your nearest NEC design center.

Block Library Support

CB-C10's functional blocks are designed to be backward-compatible with previous families. Thus, an easy migration from previous designs is possible.

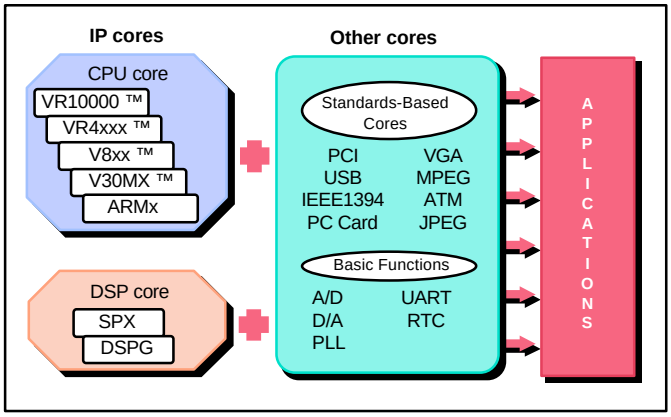
The CB-C10 family offers a wide variety of advanced blocks, including combinational gates, shift registers, adders and counters. In addition, memory blocks such as RAM and ROM are provided. The CB-C10 primitive macros are available in up to four performance/power options per primitive. With a range of options available, popular design synthesis tools are able to make the optimal size/performance/power choice for each path.

A wide range of different interface blocks allows easy integration in 2.5-volt and 3.3-volt systems. Advanced high-speed buffers are also available for special applications. Table 3 summarizes the available interface options.

Macro Library Support

The high-integration density of up to 21.3 million available gates offered by NEC's CB-C10 technology provides a foundation for complete system-on-silicon integration. NEC also provides complex functions targeted at particular market applications. NECs basic core support concept is shown in Figure 3. Table 5 also contains a list of some of the cores supported in the CB-C10 library.

Figure 3. Example for Power Rail Option



Note: The figure above only shows a subset of usable cores.

The macro library is continuously growing and NEC also offers custom macro design services based on customer requests. The macros are completely supported by NEC's OpenCAD environment, which includes high-quality simulation and test pattern generation support.

Memory Macros. CB-C10 supports a wide variety of synchronous memory macros. These memory blocks are generated with advanced memory compiler tools, ensuring the optimal fit to design requirements. The compiled blocks are output as hard macros to offer the highest possible density. The memory compilers are described in Table 4.

Table 4. CB-C10 Memory Compilers

Type (Function)	Max. Size (words x bits)	Access Time [ns]*
RAM		
Super high-speed single port	2k w x 32 b	2.7
High-speed dual port	2k w x 64 b	3.4
High-speed single port	2k w x 64 b	3.4
High-density dual port	4k w x 64 b	5.3
High-density single port	4k w x 64 b	5.3
ROM	32k w x 64 b	5.8

*512k w x 8 b, worst condition, C_L = 0 pF

Analog Macros. A variety of A/D and D/A converters are available for mixed-signal applications. Analog-to-digital converters (ADCs) are under development with a bit resolution in the range of 7 to 12 bits and a frequency of 100 kHz (for general-purpose applications) up to 30 MHz. Digital-to-analog converters (DACs) will also be developed with resolutions of 7 to 12 bits and a frequency of 100 kHz to 220 MHz for high-speed conversion.

Mega Macros. NEC offers a large set of megamacros and cores to cope with today's system requirements. Table 5 shows a subset of the macro portfolio.

Table 5. CB-C10 Mega Macro Library (subset listing)

Type	Description	Type	Description
CPU	V30xx: 16-bit microprocessor (several derivates)	I/F Peripheral	71054: programmable timer/counter
CPU	70008: 8-bit Z80™ microprocessor	I/F Peripheral	71055: programmable parallel interface (3x 8bit)
CPU	V8xx: 32-bit RISC microcontroller (several derivates)	/F Peripheral	71059: interrupt controller unit
CPU	ARM7TDMI	I/F Peripheral	ATM (25 MHz, 155 MHz)
CPU	VR4xxx: 64-bit RISC microcontroller (several derivates)	I/F Peripheral	CODEC (modem, voice)
Datapath	High-speed multiplier/accumulator	I/F Peripheral	Ethernet 10/100 Base
DSP	OAK: digital signal processor	I/F Peripheral	IEEE 1284: bidirectional centronics
DSP	PINE: digital signal processor	I/F Peripheral	IEEE1394: High-speed serial bus
DSP	SPRX: digital signal processor	I/F Peripheral	MPEG2
I/F Peripheral	16550: UART with FIFO and 16450 mode	I/F Peripheral	PCI Controller
I/F Peripheral	4993: 8-bit parallel I/O real-time clock	I/F Peripheral	RAC: RAMBUS ASIC Cell
I/F Peripheral	71037: DMA controller	I/F Peripheral	USB: Universal Serial Bus interface
I/F Peripheral	71051: USART, 300k bit/s, full-duplex	DPLL	Digital PLL (up to 250 MHz)
		APLL	Analog PLL (up to 500 MHz)

Packaging

The advanced pad pitch of 40 µm allows high-pin-count applications and gives a significant benefit for pad-limited designs. EA-C10, the new high-performance embedded array family, is supported by a variety of advanced packages. For lower pin counts (up to 376 pins), the standard QFP is available, including the heat-spreader package type to improve thermal characteristics.

Package Type	Maximum Pin/Ball Count
Plastic BGA	672
Tape BGA	1088
QFP	376 (0.4 mm pitch)
Flip-Chip	2016
Chip Scale	500

Plastic BGAs with up to 672 balls can help to cope with high-complexity system requirements by providing excellent electrical and thermal characteristics. Tape BGA packages support up to 1088 balls.

NEC expands the package offering continuously with new advanced packages. For high-performance applications with high pin counts, the 2-layer tape BGA with enhanced electrical characteristics is available. Applications that require ultra-dense packages can be realized with the flip-chip package. This technique can also be used for Multi-Chip Module (MCM) structures, where die mounting was previously necessary.

CAD Support

NEC takes up the challenges of the new ultra-high-density 0.25 µm technology by having close relationships with leading EDA vendors to fulfill the design requirements during the whole design flow.

Fully supported by NEC's sophisticated OpenCAD design framework, CB-C10 maximizes design quality and flexibility while minimizing ASIC design time.

NEC's OpenCAD system allows designers to combine the EDA industry's most popular third-party design tools with proprietary NEC tools, including those for advanced floorplanner, clock tree synthesis, automatic test pattern generation (ATPG), full-timing simulation, accelerated fault grading and advanced place and route algorithms. The latest OpenCAD system is open for sign-off using standard EDA tools. NEC offers RTL- and STA-(Static Timing Analysis) sign-off procedures to shorten the ASIC design cycle of high-complexity designs.

Support of High-Speed Systems. High-speed systems require tight control of clock skew on the chip and between devices on a printed circuit board. CB-C10 provides two features to control clock skew: the Digital PLL (DPLL) working at frequencies up to 250 MHz for chip-to-chip skew minimization and Clock Tree Synthesis (CTS). CTS — supported by an NEC proprietary design tool — is used for clock skew management through the automatic insertion of a balanced buffer tree. The clock tree insertion method minimizes large capacitive trunks and is especially useful with the hierarchical, synthesized design style being used for high-integration devices. RC values for actual net lengths of the clock tree are used for back annotation after place and route operations. A skew as low as ±60 ps can be achieved.

Accurate Design Verification. Nonlinear timing calculation is a very important requirement of the high-density, deep sub-micron ASIC designs. NEC makes use of the increased accuracy delivered by the nonlinear table look-up delay calculation methodology and offers consistent wire load models to ensure a high accuracy of the design verification.

Design Rule Check. A comprehensive design rule check (DRC) program reports design rule violations as well as chip utilization statistics for the design netlist. The generated report contains such information as net count, total pin and gate counts, and utilization figures.

Layout. During design synthesis, wire load models are used to get delay estimations in a very early state of the design flow. In general, there's no need for customers to perform the floorplanning to meet the required timing. During layout, enhanced in-place optimization (IPO) features of the layout tools and engineering change order (ECO) capabilities of the synthesis tools are used to optimize critical timing paths defined by the given timing constraints. These features can reduce the total design time.

Test Support

The CB-C10 family supports automatic test generation through a scan test methodology. It includes internal scan, boundary scan (JTAG) and built-in-self-test (BIST) architecture for easy and high-performance production RAM testing. This allows higher fault coverage, easier testing and faster development time.

Test of embedded megamacros is supported from NEC's test bus concept, which allows the use of predefined test pattern sets for integrated core macros.

Supplemental Publications

This data sheet contains preliminary specifications and operational data for the CB-C10 embedded array family. Additional information is available in NEC's CB-C10 Design Manual, Block Library and other related documents. Please refer also to the CMOS-10 and EA-C10 data sheets to get more information about 0.25 µm gate array and cell-based ASIC products.

Please contact your local NEC design center for additional information; see the back of this data sheet for locations and telephone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	3.6 V
Input voltage, V_I	
2.5V input buffer	3.6 V
3.3V input buffer	4.6 V
Output voltage, V_O	
2.5V buffer	3.6 V
3.3V buffer	4.6 V
Latch-up current, I_{LATCH}	1 A
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input / Output Capacitance

V_{DD}=V_I=0 V; f=1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	4	6	pF
Output	C_{OUT}	4	6	pF
I/O	$C_{I/O}$	4	6	pF

Note: Values do not include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal cell (@ 2.5V supply voltage, loaded)	0.04	µW/MHz
Input block (FI01, F/O=2, L=0)	1.66	µW/MHz
Output block (F002 @ 15 pF)	167	µW/MHz

Recommended Operating Conditions

		2.5V Buffer		3.3V Buffer		3.3V PCI		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Power supply voltage	V_{DD}	2.3	2.7	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	-40	+125	-40	+125	-40	+125	°C
Low-level input voltage	V_{IL}	0	0.7	-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	V
High-level input voltage	V_{IH}	1.7	V_{DD}	0.5 V_{DD}	V_{DD}+ 0.5	0.5 V_{DD}	V_{DD}+ 0.5	V
Input rise or fall time	t_R, t_F	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	0	10	ms

AC Characteristics

V_{DD} = 2.5 V ± 0.2 V; T_j = 0 to +125°C

Parameter	Symbol	Best	Typ	Worst	Unit	Conditions
Toggle frequency	f_{TOG}		1.6		GHz	D-F/F; F/O = 1
Delay time						
2-input power - NAND (F322)	t_{PD}	23.9	31.5	51.3	ps	F/O = 2; L = 0 mm
	t_{PD}	69.7	93.4	152	ps	F/O = 1; L = 0.5 mm
Flip-flop (F611)	t_{PD}	288	401	663	ps	F/O = 1; L = 0 mm
	t_{PD}	388	539	881	ps	F/O = 2; L = 0.5 mm
	t_{SETUP}	240	270	360	ps	—
	t_{HOLD}	300	340	410	ps	—
Input buffer (FI01)	t_{PD}	77.8	103	188	ps	F/O = 1; L = 0.5 mm
	t_{PD}	63.0	79.7	144	ps	F/O = 2; L = 0 mm
Input buffer (3.3V) *	t_{PD}	190	286	510	ps	F/O = 1; L = 0.5 mm
	t_{PD}	173	255	451	ps	F/O = 2; L = 0 mm
Output buffer (12 mA) 2.5V	t_{PD}	287	439	779	ps	C_L = 0 pF
Output buffer (12 mA) 2.5V	t_{PD}	932	1363	2312	ps	C_L = 50 pF
Output buffer (12 mA) 3.3V *	t_{PD}	457	659	1192	ps	C_L = 0 pF
Output buffer (12 mA) 3.3V *	t_{PD}	1386	2115	3554	ps	C_L = 50 pF
Output rise time (12 mA)	t_R	0.73	1.03	1.83	ns	C_L = 15 pF; 10-90%
Output fall time (12 mA)	t_F	0.75	0.93	1.55	ns	C_L = 15 pF; 10-90%

Note: *including delay of level shifter circuit

DC Characteristics

V_{DD} = 2.5 V ± 0.2 V; T_j = 0 to +125° C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current						
<= 2000K gates	I_{DDS}		40	800	µA	$V_I = V_{DD}$ or GND
> 2000K gates	I_{DDS}		70	1400	µA	$V_I = V_{DD}$ or GND
Off-state output leakage current						
2.5V output	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
3.3V output	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
Output sink current with pull-up (V_O = 2.5V)	I_R				µA	V_{PU} = 3.3 V, R_{PU} =2kΩ
Output sink short circuit current	I_{OS}			-250	mA	V_O = GND
Input leakage current						
Regular	I_I		$\pm 10^{-4}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I		TBD		µA	V_I = GND
5 kΩ pull-up	I_I		TBD		mA	V_I = GND
50 kΩ pull-down	I_I		TBD		µA	$V_I = V_{DD}$
Pull-up resistor						
50 kΩ pull-up	R_{PU}		TBD		kΩ	
5 kΩ pull-up	R_{PU}		TBD		kΩ	
50 kΩ pull-down	R_{PD}		TBD		kΩ	
Low-level output current						
2.5V buffers						
3 mA	I_{OL}	11.0	8.8	5.2	mA	V_{OL} = 0.4V
6 mA	I_{OL}	22.3	17.6	11.5	mA	V_{OL} = 0.4V
9 mA	I_{OL}	33.5	26.5	15.8	mA	V_{OL} = 0.4V
12 mA	I_{OL}	44.5	35.3	21.2	mA	V_{OL} = 0.4V
18 mA	I_{OL}	66.7	52.9	31.7	mA	V_{OL} =0.4V
24 mA	I_{OL}	88.7	70.5	42.3	mA	V_{OL} = 0.4V
3.3V buffers (full-swing)						
3 mA	I_{OL}	20.5	14.5	8.3	mA	V_{OL} = 0.4V
6 mA	I_{OL}	30.3	21.7	12.5	mA	V_{OL} = 0.4V
9 mA	I_{OL}	40.5	29.0	16.7	mA	V_{OL} = 0.4V
12 mA	I_{OL}	46.8	36.0	20.8	mA	V_{OL} = 0.4V
Low-level output voltage						
2.5V buffers	V_{OL}			0.1	V	I_{OL} = 0 mA
3.3V buffers	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage						
2.5V buffers	V_{OH}	V_{DD} - 0.1			V	I_{OH} = 0 mA
3.3V buffers	V_{OH}	V_{DD} - 0.1			V	I_{OH} = 0 mA

THIRD-PARTY DESIGN CENTERS

SOUTH CENTRAL/SOUTHEAST

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  Longwood, FL 32750

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  FAX 407-260-6227

- Integrated Silicon Systems Inc.
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  Durham, NC 27713

  TEL 919-361-5814
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