C9950

3.3V, 180MHz, Multi-Output Clock Driver

Approved Product

Product Features

- 180MHz Clock Support
- Supports PowerPC™, Intel and RISC Processors
- 9 Clock Outputs: Frequency Configurable
- Oscillator or Crystal Reference Input
- Output Disable Control
- ±100ps Cycle-to-Cycle Jitter
- Spread Spectrum Compatible
- Pin Compatible with MPC950
- 32-Pin TQFP Package

Block Diagram

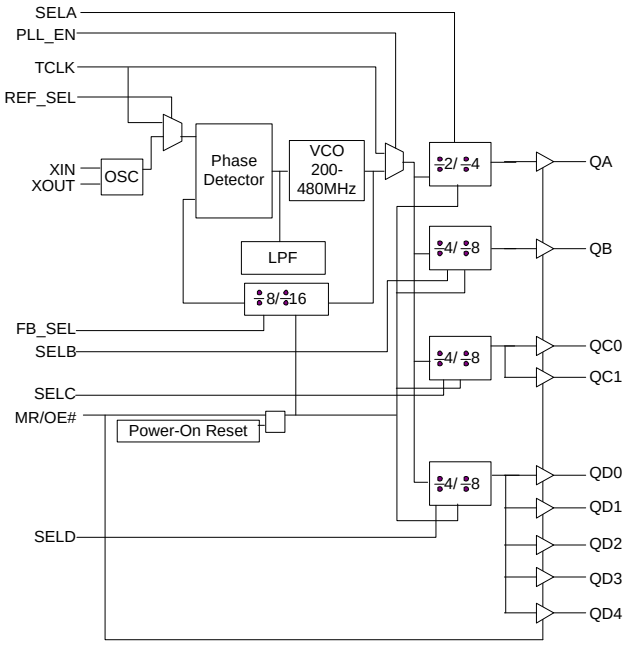


Figure 1

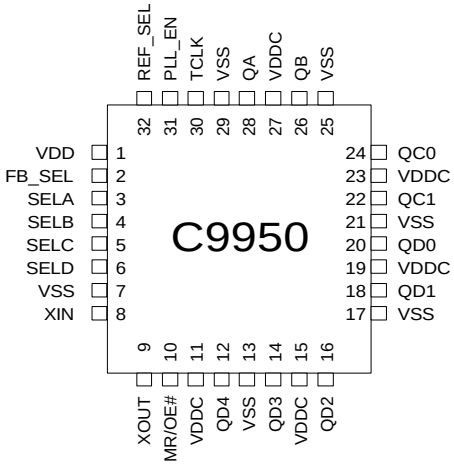
Frequency Table

SEL (A:D)	FB_SEL = 1				FB_SEL = 0			
	QA	QB	QC (0,1)	QD (0:4)	QA	QB	QC (0,1)	QD (0:4)
0000	4x	2x	2x	2x	8x	4x	4x	4x
0001	4x	2x	2x	x	8x	4x	4x	2x
0010	4x	2x	x	2x	8x	4x	2x	4x
0011	4x	2x	x	x	8x	4x	2x	2x
0100	4x	x	2x	2x	8x	2x	4x	4x
0101	4x	x	2x	x	8x	2x	4x	2x
0110	4x	x	x	2x	8x	2x	2x	4x
0111	4x	x	x	x	8x	2x	2x	2x
1000	2x	2x	2x	2x	4x	4x	4x	4x
1001	2x	2x	2x	x	4x	4x	4x	2x
1010	2x	2x	x	2x	4x	4x	2x	4x
1011	2x	2x	x	x	4x	4x	2x	2x
1100	2x	x	2x	2x	4x	2x	4x	4x
1101	2x	x	2x	x	4x	2x	4x	2x
1110	2x	x	x	2x	4x	2x	2x	4x
1111	2x	x	x	x	4x	2x	2x	2x

Table 1

* x = is the reference input frequency

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	TYPE	Description
8	**XIN**		I		Oscillator Input. Connect to a crystal.
9	**XOUT**		0		Oscillator Output. Connect to a crystal.
30	**TCLK**		I	PD	External Test Clock Input.
28	**QA**	VDDC	O		Clock Output. See Frequency Table.
26	**QB**	VDDC	O		Clock Output. See Frequency Table.
22, 24	**QC(1,0)**	VDDC	O		Clock Outputs. See Frequency Table.
12, 14, 16, 18, 20	**QD(4:0)**	VDDC	O		Clock Outputs. See Frequency Table.
2	**FB_SEL**		I	PD	Feedback Select Input. If FB_SEL = 1, then the (÷8) counter is selected in the PLL feedback loop. If FB_SEL = 0, then the (÷16) counter is selected in the PLL feedback loop.
10	**MR/OE#**		I	PD	Master Reset/Output Enable Input. When asserted high, resets all of the internal flip-flops and also disables all of the outputs. When pulled low, releases the internal flip-flops from reset and enables all of the outputs.
31	**PLL_EN**		I	PU	PLL Enable Input. When asserted high, PLL is enabled. And when set low, PLL is bypassed.
32	**REF_SEL**		I	PD	Reference Select Input. When high, TCLK is the reference clock and when low, the crystal oscillator is selected.
3, 4, 5, 6	**SEL(A:D)**		I	PU	Frequency Select Inputs. See Frequency Table. If SEL_ = 1, then QA divider = ÷4, QB:D divider = ÷8 If SEL_ = 0, then QA divider = ÷2, QB:D divider = ÷4
11, 15, 19, 23, 27	**VDDC**				3.3V Power Supply for Output Clock Buffers.
1	**VDD**				3.3V Power Supply for PLL
7, 13, 17, 21, 25, 29	**VSS**				Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.