# C9840

## Clock Generator for Pentium® Systems with Rambus® Support

Preliminary

### Product Features

- Three CPU clocks (66MHz, 2.5V)
- One DRCGREF clock (66/50 MHz, 2.5V)
- Eight PCI clocks (1 free running during PCISTOP mode) (33 MHz, 3.3V)
- Two IOAPIC clocks (16.67 MHz, 2.5V)
- Two 48M's (48 MHz, 3.3V), not affected by SS
- One 48M2V (48 MHz, 2.5V), not affected by SS
- Two REF's (14.318 MHz, 3.3V), not affected by SS
- EMI reducing Spread Spectrum (SS) technology
- Support for both Mobile and Desktop Power-down and OE modes

### Product Description

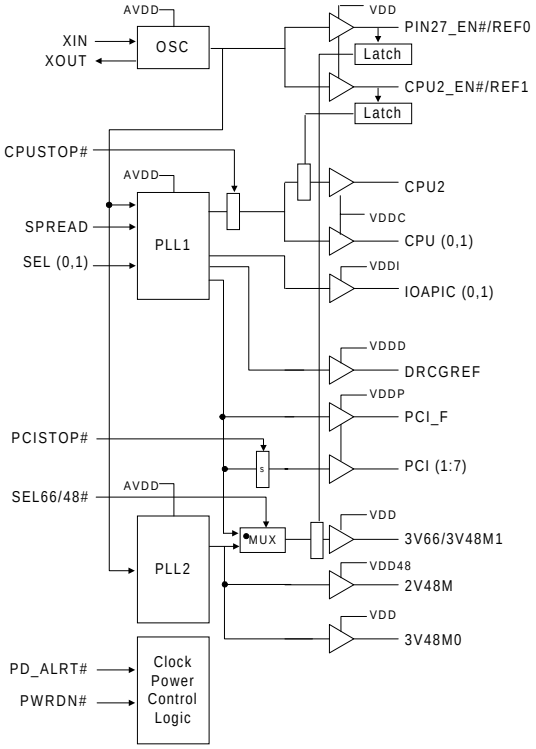
The C9840 is a clock generator solution that supports Intel Pentium III based Rambus memory architecture designs. It operates at a fixed CPU frequency of 66 MHZ and supplies the DRCG reference clock required to drive the Rambus channel. Supplied in a 48 pin SSOP package it includes the patented and design proven Spread Spectrum EMI noise reduction technology. This device integrates IMI Spread Spectrum clock technology to produce low EMI.

### Select Input Functionality

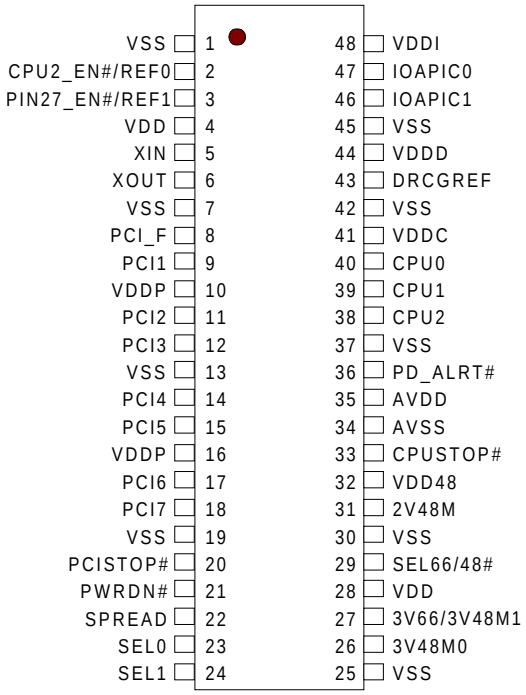
| SEL 1 | SEL 0 | CPU (0:2) | DRCGREF | PCI (F,1:7) | 3V48M0; 2V48M | 3V66/3V48M1 | | REF (0,1) | IOAPIC (0,1) |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | P29 = 0 | P29 = 1 | | |
| 0 | 0 | 3-state | 3-state | 3-state | 3-state | 3-state | 3-state | 3-state | 3-state |
| 0 | 1 | 66 MHz | 50 MHz | 33 MHz | 48 MHz | 48 MHz | 66 MHz | 14.318 MHz | 16.67 MHz |
| 1 | 0 | XIN/3 | XIN/4 | XIN/6 | XIN/2 | XIN/2 | XIN/2 | XIN | XIN/12 |
| 1 | 1 | 66 MHz | 66 MHz | 33 MHz | 48 MHz | 48 MHz | 66 MHz | 14.318 MHz | 16.67 MHz |

Table 1

### Block Diagram




### Pin Configuration



## Pin Description

| PIN No. | Pin Name | I/O | Description |
|---|---|---|---|
| 3* | PIN27_EN# REF1 | I/O | During power-up, this pin is a latched input that controls Pin 27 (3V66/3V48M1). If this pin is pulled low during power up, the device will output a 66 or 48 MHz 3.3V clock on pin 27. If it is left disconnected or polled to a high level during power up, it disables (3-state) Pin 27 after power up. After power-up, this pin is a 14.318 MHz clock output |
| 2* | CPU2_EN# /REF0 | I/O | During power-up, this pin first acts as a latched input that enables CPU2 (Pin 38) to run if it is pulled to a low level. If left disconnected or pulled to a high level during power up, it will cause the a CPU2 clock to be disabled (tri-state) after power-up. After power-up, this pin is a 14.318MHz clock output. |
| 8 | PCI_F | O | Free-running 3.3V PCI clock output. This clock does not stop when PCI_STOP# = 0. |
| 9,11,12,14, 15,17,18 | PCI[1:7] | O | 3.3V PCI clock outputs. These clocks synchronously (no glitch) stops in a low state when PCI_STOP# is asserted low. |
| 39, 40 | CPU[1:0] | O | 2.5V CPU clock outputs. See Table1, page 1 for frequency selection. |
| 38 | CPU2 | O | 2.5V CPU clock output. If Pin 2 is latched with a high logic level during power-up, this pin is placed into 3-state mode and not active. When Pin 2 latches a low during power-up, this pin functions as a normal CPU clock output. |
| 43 | DRCGREF | O | 2.5V reference clock output for external DRCG device. See Table 1, page1 for frequency selection. |
| 46, 47 | IOAPIC[1:0] | O | 2.5V 16.67 MHz IOAPIC clock output. |
| 6 | XOUT | O | On-chip reference oscillator pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected. |
| 5 | XIN | I | On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal |
| 31 | 2V48M0 | O | 2.5V 48M clock output. |
| 27* | 3V66/ 3V48M1 | O | Dual function 3.3V clock output pin. When Pin 29 is at a logic high level, This Pin functions a 3.3V 66 MHz output; when Pin 29 is latched as a logic low level, this Pin functions as a 3.3V 48 MHz output. |
| 26* | 3V48M0 | O | 3.3V 48M clock output. |
| 4, 28 | VDD | Pwr | 3.3V I/O power supply. |
| 10, 16 | VDDP | Pwr | 3.3V I/O power supply for PCI(1:7) and PCI_F clock output buffers. |
| 48 | VDDI | Pwr | 2.5V I/O power supply for IOAPIC(0,1) clock output buffers. |
| 44 | VDDD | Pwr | 2.5V I/O power supply for DRCGREF clock output buffer. |
| 32 | VDD48 | Pwr | 2.5V I/O power supply for 2V48M clock buffers. |
| 41 | VDDC | Pwr | 2.5V I/O power supply for CPU clock output buffers. |
| 1, 7, 13, 19, 25, 30, 37, 42, 45 | VSS | Pwr | Common ground |
| 35 | AVDD | Pwr | 3.3V core/PLL power supply. |
| 34 | AVSS | Pwr | Chip ground (paired with AVDD) for core/PLL circuitry |
| 22* | SPREAD | I | Active high Spread Spectrum enable input for CPU, PCI, IOAPIC, DRCGREF, and 3V66 outputs. This pin has a weak pull-up internally to ensure spread is active when no external pull-ups are used. |
| 21 | PWRDN# | I | Active low power down input for all clocks; turns off PLLs and all outputs are driven low. |

## Pin Description (Cont.)

| PIN No. | Pin Name | I/O | Description |
|---|---|---|---|
| 20 | PCISTOP# | I | Active low PCI stop clock. Stops all PCI outputs to low state (see pg 7). |
| 33 | CPUSTOP# | I | Active low CPU stop clock. Stops all CPU outputs to low state (see pg 6). |
| 24* | SEL1 | I | Frequency and function Select input pin (see table on pg 1). |
| 36* | PD_ALRT# | I | Mobile power-down feature; when pulled low, all outputs will be driven low except for CPU2; PLLs will remain running. |
| 23* | SEL0 | I | Frequency and function select input pin (see table on pg 1). |
| 29* | SEL66/48# | I | Pin 28 controlling input pin; when this pin is pulled high, Pin 28 functions as a 3.3V 66 MHz output; when this pin is pulled low, Pin 28 functions as a 3.3V 48 MHz output. |

Note: Pins marked with * have internal pullup devices present.

## Device Configuration Table

| CPU2_EN# Latched on Power Up (Pin 2) | PIN27_EN# Latched on Power Up (Pin 3) | SEL1 (Pin 24) | SEL0 Pin (23) | SEL66/48# (Pin 29) | CPU2 (Pin 38) | 3V66/3V48M1 (Pin 27) |
|---|---|---|---|---|---|---|
| 1 | 1 | X | X | X | 3-State | 3-State |
| X | X | 0 | 0 | X | 3-State | 3-State |
| 0 | 1 | 0 | 1 | X | 66 MHz | 3-State |
| 0 | 1 | 1 | 0 | X | XIN/3 | 3-State |
| 0 | 1 | 1 | 1 | X | 66MHz | 3-State |
| X | X | 0 | 0 | X | 3-State | 3-State |
| 1 | 0 | 0 | 1 | 0 | 3-State | 48 MHz |
| 1 | 0 | 0 | 1 | 1 | 3-State | 66 MHz |
| 1 | 0 | 1 | 0 | 0 | 3-State | XIN/2 |
| 1 | 0 | 1 | 0 | 1 | 3-State | XIN/3 |
| 1 | 0 | 1 | 1 | 0 | 3-State | 48 MHz |
| 1 | 0 | 1 | 1 | 1 | 3-State | 66 MHz |
| 0 | 0 | 0 | 1 | 0 | 66 MHz | 48 MHz |
| 0 | 0 | 0 | 1 | 1 | 66 Mhz | 66 MHz |
| 0 | 0 | 1 | 0 | 0 | XIN/3 | XIN/2 |
| 0 | 0 | 1 | 0 | 1 | XIN/3 | XIN/3 |
| 0 | 0 | 1 | 1 | 0 | 66 MHz | 48 MHz |
| 0 | 0 | 1 | 1 | 1 | 66 MHz | 66 MHz |

*NOTE: XIN is the frequency of the clock on Pin 5 (the XIN clock pin) of the device.*

## VDD Power-Down Removal Sequencing

Some designs that use the C9840 device require specific power-down procedure protocols to be observed. This is done to allow for multiple devices in a system to share voltage regulators, The C9840 allows the removal of power from its VDD voltage pins (Pins 4, 10, 16, and 28) using the following specific procedures.

## Entering Power Down Mode

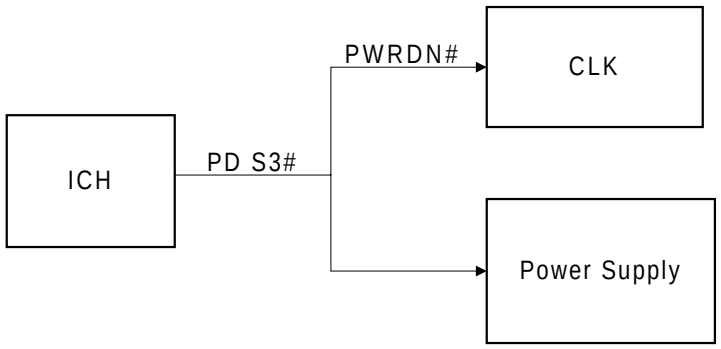
1. Assert the PWRDN# signal of the clock.
2. Remove power from the VDD pins of the clock.
3. All input pins of the clock must be either powered down or driven to ground.
4. The VDD power plane will be pulled to or discharge to <250 mV.
5. The 2.5V pins must remain powered at 2.5V.

## Recovering from Power Down Mode

1. Apply 3.3V to all of the VDD power pins.
2. Wait 2000 mSec.
3. De-assert the PWRDN# signal.
4. Wait 10 mSec.
5. Resume operation.

## Power Management

A typical implementation of PWRDN# in a system is shown in the diagram below:




In this implementation, the PD_S3# input drives both the PWRDN# and power supply pins that effect shutdown of the C9840. When the C9840 is off, the PD_S3# releases (pulls high). The clock (and the power supply) maintain a high-Z path to ground during power-down to properly allow PD_S3# to pull both the clock and the power supply out of power down mode quickly. This is accomplished by a small series resistor on the input structure of this pin inside the C9840.

## Power Management Functions

| Signal | Signal State | Latency No. of Rising Edges PCICLK |
|---|---|---|
| CPU_STOP# | 0 (disabled) | 1 |
| | 1 (enabled) | 1 |
| PCI_STOP# | 0 (disabled) | 1 |
| | 1 (enabled) | 1 |
| PWRDN# | 1 (normal operation) | 3 mS |
| | 0 (power down) | 2 max. |
| PD_ALRT# | 1 (normal operation) | 3 mS |
| | 0 (power down) | 2 max. |

**Notes:**
Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
Power up latency is when PWRDN# goes inactive (high) to when the first valid clocks are driven from the device.

## Maximum Lumped Capacitive Output Loads

| Clock | Max Load | Units |
|---|---|---|
| CPU Clocks | 20 | pF |
| PCI Clocks Note1 | 30 | pF |
| DRCGREF | 20 | pF |
| 3V66/3V48 | 30 | pF |
| 48 MHz Clock | 20 | pF |
| REF | 20 | pF |
| IOAPIC | 20 | pF |

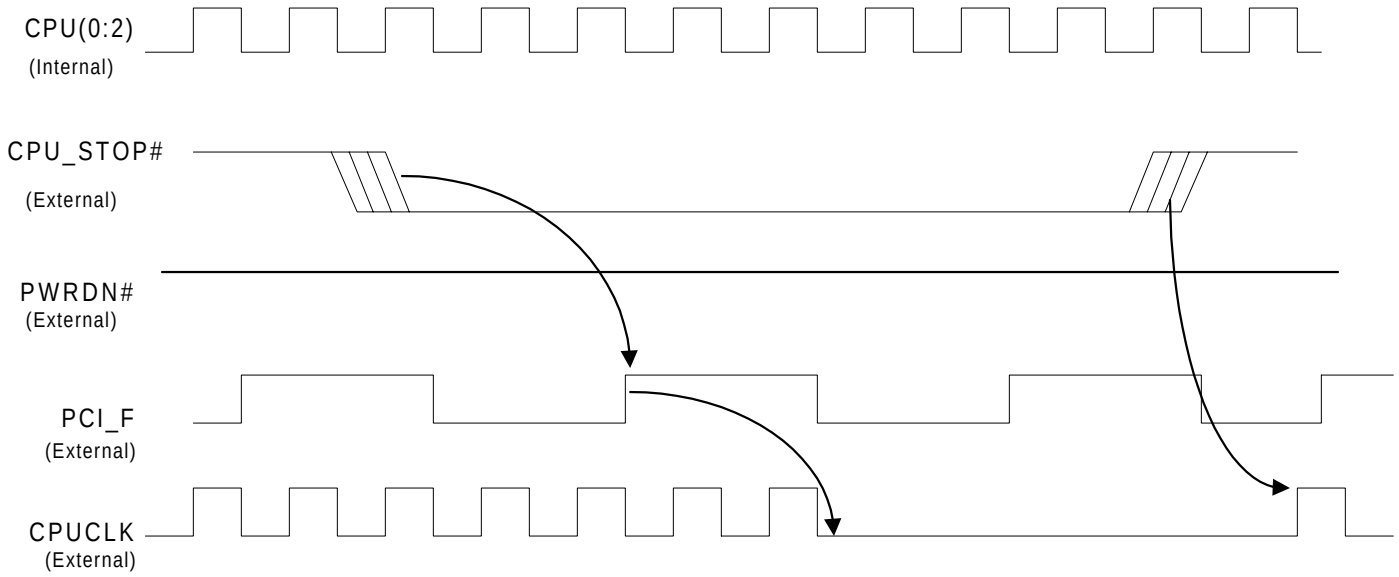
Table 2

## Maximum Allowed Current

| Power Management | Max 2.5V supply consumption<br>Max discrete cap load,<br>All 2.5 Volt Vdd's = 2.625V<br>All static inputs = 3.3 Volts or VSS | Max 3.3V supply consumption<br>Max discrete cap loads<br>All 3.3 Volt VDD = 3.465V<br>All static inputs = 3.3 Volts or VSS. |
|---|---|---|
| Powerdown Mode (PWRDN# and PD_ALRT# = 0) | 100 uA | 200 uA |
| Full Active<br>CPUSTOP#, PCISTOP# = 1,<br>PD_ALRT# =1 | 75 mA | 160 mA |

CPU_STOP# is an input to the clock generator. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic and is internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU is always stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. Only one rising edge of PCI_F occurs after the clock control logic is switched for both the CPU outputs to become enabled/disabled.

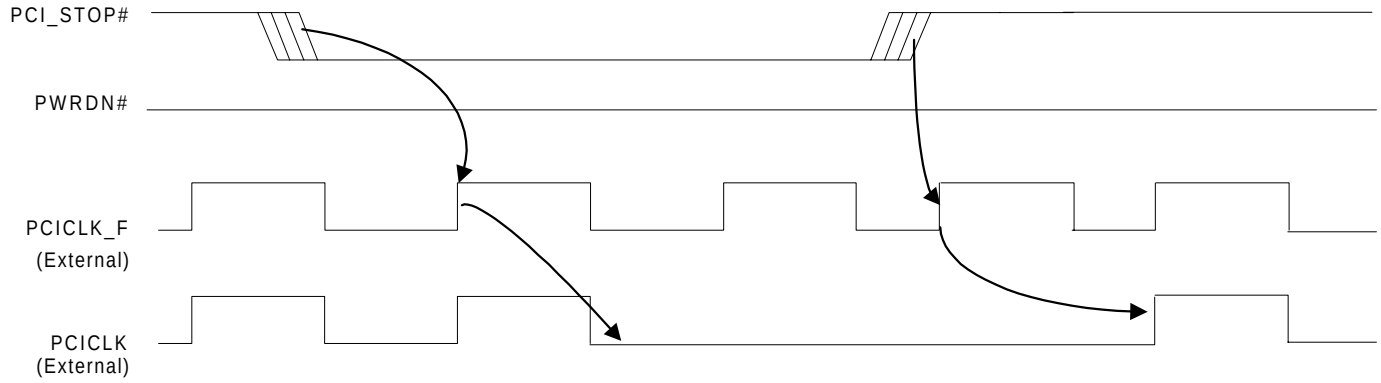
## CPU_STOP# Timing Diagram




**Notes:**
1. All internal timing is referenced to the CPUCLK.
2. The internal label means inside the chip and is a reference only.
3. CPU_STOP# signal is an input signal that is made synchronous to free running PCI_F.

PCI_STOP# is an input to the clock generator and is made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are stopped in a low state and started such that a full high pulse width is guaranteed. ONLY one rising edge of PCI_F occurs after the clock control logic switched for the PCI outputs to become enabled/disabled.

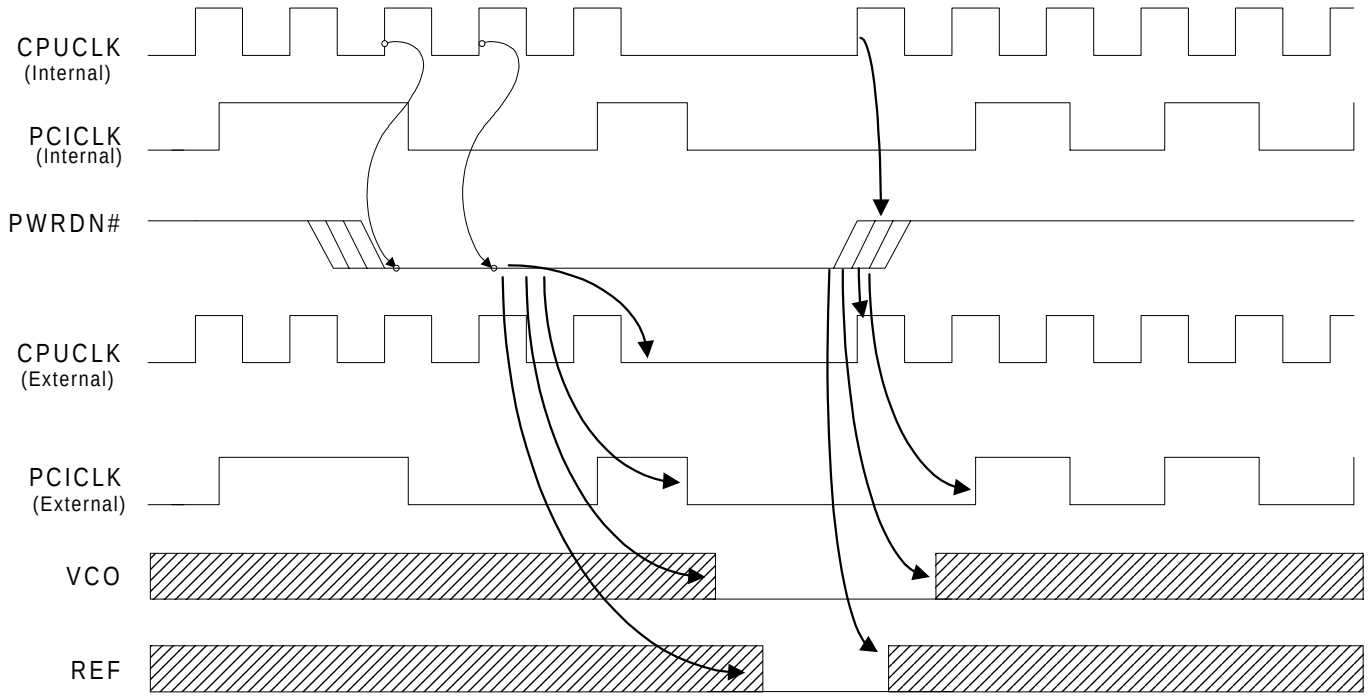
## PCI_STOP# Timing Diagram




**Notes:**
1. All internal timing is referenced to the CPUCLK.
2. All other clocks continue to run undisturbed.

The power down selection is used to put the part into a very low power state without turning off the power to the part. PWRDN# is an asynchronous active low input. This signal is synchronized internal by the device prior to powering down itself. PWRDN# is an asynchronous function for powering up and down systems. Internal clocks are not running after the device is put in it's power down mode of operation. When PWRDN# is active low all clocks are driven to a low value and held prior to turning off the VCO's and the crystal oscillator. The power-up latency time of the C9840 is less than 3 mS. The power down latency is guaranteed to conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48 MHz clocks are stopped in the LOW state during power down mode. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW may require more than one clock cycle to complete.

## PWRDN# Timing Diagram

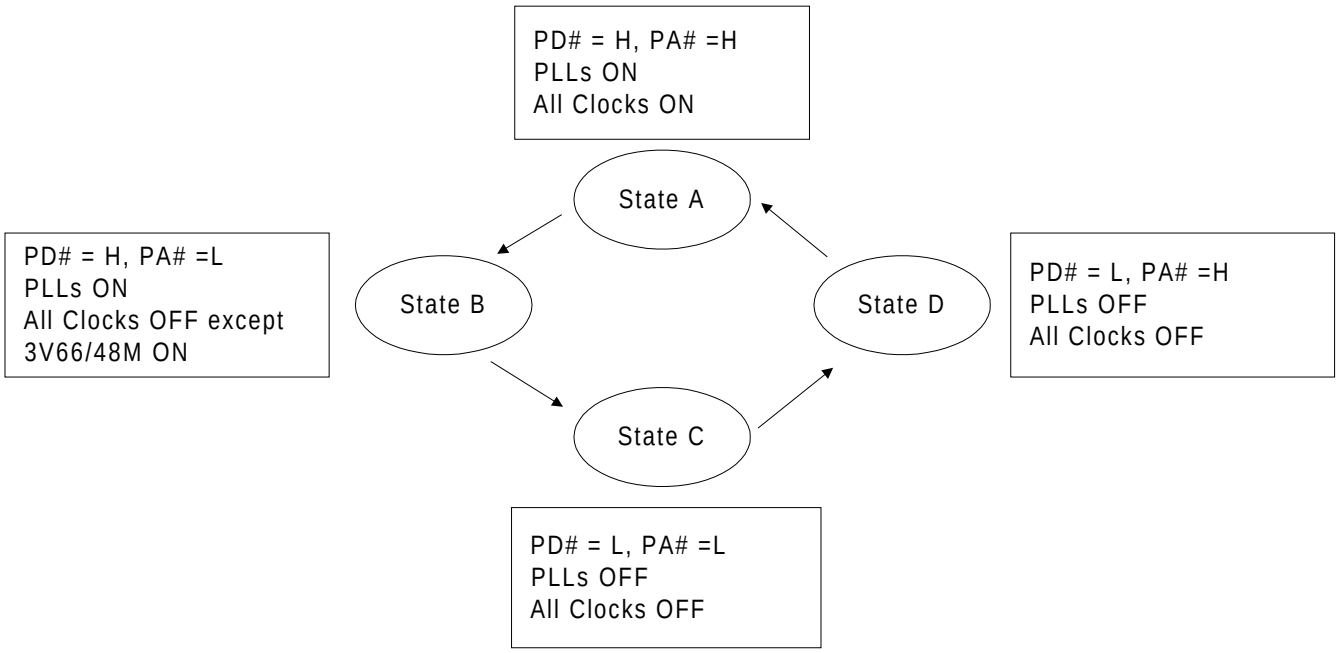



**Notes:**
1. All internal timing is referenced to the CPU clock.
2. Internal means inside the chip.
3. PWRDN# is an asynchronous input. This signal is synchronized inside the part.
4. The shaded sections of the VCO and the REF signals indicate an active clock.

## PWRDN# and PD_ALRT#

The PD_ALRT# pin on the device is used to activate a special mobile-specific power-down mode. When PD_ALRT# is pulled low, all outputs are driven low in a similar fashion to a PWRDN# assertion EXCEPT for the 3V66/48M output (Pin 27) while the PLLs remain locked. Latency requirements for assert/de-assert of this feature are identical to PWRDN#. From this state, the device is placed back into full normal operation by de-assertion of PD_ALRT# or into full power-down by assertion of PWRDN#.

The state diagram below illustrates the various usages of PD_ALRT# and PWRDN#. The boxes represent the states of the PD_ALRT# and PWRDN# pins and the usage condition:




In a mobile application, the PD_ALRT# pin is pulled low, causing the clock chip to drive all outputs low EXCEPT for the 3V66/48M output (Pin 27) with the PLLs inside the device still running [State B]. The system will then (approximately 100ms later) pull PWRDN# high which causes all outputs to go low and the PLLs to shut off [State C]. When coming out of power down, the system will release PD_ALRT# by pulling this output high prior to releasing PWRDN# [State D], at which time all clocks will revert to running normally. PWRDN# is then pulled high to complete the state transitions [State A].

Several other situations may occur to alter its power down state.

1. If the device is in State C (PD_ALRT# = low, PWRDN# = low), and PWRDN# is pulled high before PD_ALRT#, the device reverts to State B with only the 3V66/48M output operating. While not a normal or desired state transition from a system perspective, this provides a consistent behavior the clock in case of this condition occurring.

2. If the device is in State A (PD_ALRT# = high, PWRDN# = high), and PWRDN# is pulled low before PD_ALRT# pulls low, the device moves to State D with all output clocks running normally.

For desktop systems, the PD_ALRT# and PWRDN# pins will ALWAYS be tied together to implement power down; this means that a desktop system will only toggle between State A and State C in the diagram above.

## Spectrum Spread Clocking

Spread Spectrum is a modulation technique for reducing Electro Magnetic radiation (EMI) at the source, which in this case is the clock. The concept is based on redistributing the energy of a frequency over a finite bandwidth (also referred to as spread percentage), therefore reducing the measured emission. Fig5 represents an actual measurement on a spectrum analyzer showing the EMI reduction as a result of Spread Spectrum.

Down Spread is when the modulation is swept from the resting frequency in a downward (lower in frequency) direction and then back to the resting frequency point. The energy is redistributed asymmetrically in a downward (in frequency) on the downward sides of the resting frequencies power spectrum.

In the case of the C9840, the resting (non-spread) frequency is 66.6 MHz in the unspread mode. This will remain the same when spread spectrum is enabled but the modulation will sweep from the 66.6 MHz maximum frequency to a minimum frequency of 65.6 MHz.

When Spread Spectrum is enabled only the CPU, IOAPIC, DRCGREF, PCI, and 3V66 clocks are spread.

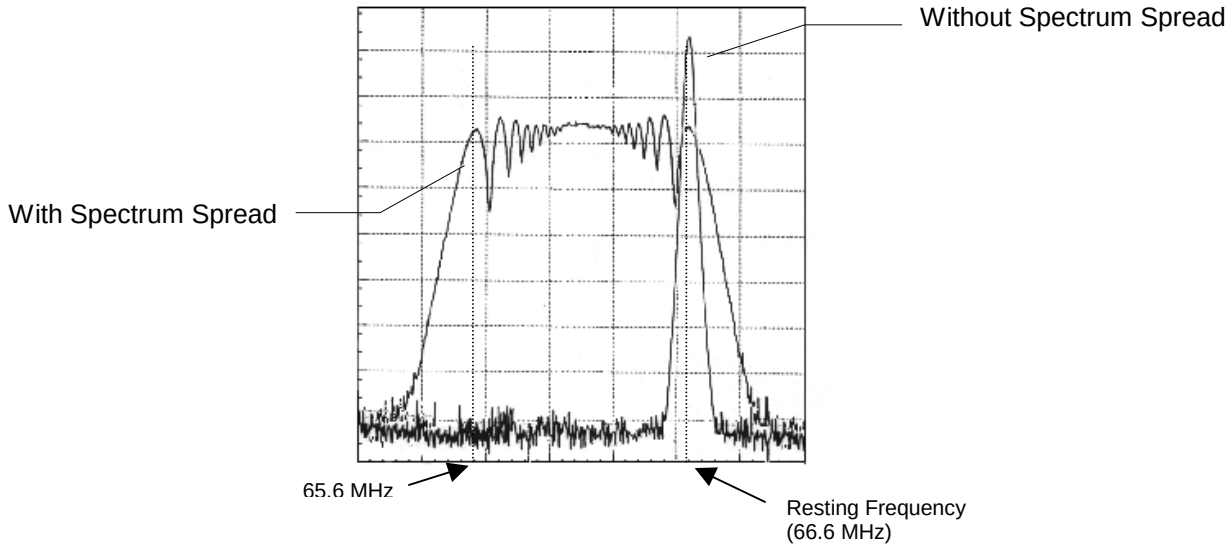



**Figure 5**
**Spectrum Analysis**

## Spectrum Spreading Selection Table

| Min Freq (MHz) | Resting Freq. (MHz) | Max Freq (MHz) | Min Period (nSec) | Average Period* (nSec) | Max Period (nSec) | CPU Frequency | % OF FREQUENCY SPREADING | MODE |
|---|---|---|---|---|---|---|---|---|
| 65.59 | 66.66 | 66.66 | 15.25 | 15.12 | 15.00 | 66.66 | 0.60% (-0.6% + 0%) | Down Spread |

*1 μS sampling period

## Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS – 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65° to +150°C
Operating Temperature: 0° to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

## DC Parameters (VDD = VDDP = AVDD = 3.3V +/- 5%, VDDP = VDDI = VDDD = VDD48 = VDDC = 2.5 + /- 5%, TA = 0°C to + 85°C)

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL1 | - | - | 1.0 | Vdc | Note 1 |
| Input High Voltage | VIH1 | 2.0 | - | - | Vdc | |
| Input Low Current (@VIL = VSS) | IIL | -66 | | -5 | µA | For internal Pull up resistors, Note 1 and Note 2 |
| Input High Current (@VIL = VDD) | IIH | | | 5 | µA | |
| Tri-State leakage Current | Ioz | - | - | 10 | µA | |
| Dynamic Supply Current | Idd3.3V | - | - | 160 | mA | Notes 3, 4 |
| Dynamic Supply Current | Idd2.5V | - | - | 90 | mA | Notes 3, 4 |
| Static Supply Current | Isdd | - | - | 400 | µA | Notes 3, 5 |
| Input pin capacitance | Cin | - | - | 5 | pF | |
| Output pin capacitance | Cout | - | - | 6 | pF | |
| Pin Inductance | Lpin | - | - | 7 | nH | |
| Crystal pin capacitance | Cxtal | 32 | 36 | 40 | pF | See suggested crystal oscillator section of this data sheet (page16) |
| Crystal Startup time | Txs | - | - | 40 | µS | From Stable 3.3V power supply. |

**Note1:** Applicable to input signals: SEL(0:1), SPREAD#, PWRDN#, CPUSTOP#, PCISTOP#.
**Note2:** Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.
**Note3:** All outputs loaded as per table 2 Page 5.
Note4: PWRDN#, PCISTOP# are at a logic high level.
Note5: PWRDN# at a logic low level.

## AC Parameters

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| CPU Output Frequency | $F_{CPU}$ | | | 66.66 | MHz | XIN= 14.31818 MHz |
| Output Enable Delay | $T_{oeA}$ | 1 | - | 10 | nSec | All Output Clocks |
| Output Disable Delay | $T_{oeD}$ | 1 | - | 10 | nSec | All Output Clocks |
| Power up to Stable Output | $T_{PU}$ | - | - | 3 | mSec | All Output Clocks |
| Clock Duty Cycle (CPU, DRCGREF, IOAPIC, 3V48M0, 2V48M, 3V66M(0,1), PCI and REF) | $T_{DC1}$ | 45 | 50 | 55 | % | 2.5 Volt clocks are measured between 0.4V & 2.0V, triggering at 1.25 Volts and at full rated capacitive loading. 3.3 Volt clocks are measured between 0.4V & 2.4V, triggering at 1.5 Volts and at full rated capacitive loading. |
| Clock Jitter (CPU, DRCGREF and 2V48) | $T_{j1}$ | | | 250 | pSec | |
| Clock Jitter (IOAPIC, 3V66, 3V48M(0,1) and PCI) | $T_{j2}$ | | | 500 | pSec | |
| Clock Jitter (REF) | $T_{j3}$ | | | 1000 | pSec | |
| Output Skew CPU to CPU | $T_{OS1}$ | | | 175 | pSec | |
| Output Skew PCI to PCI | $T_{OS2}$ | | | 500 | pSec | |
| Output Skew IOAPIC to IOAPIC and 3V66M0 to 3V66M1 | $T_{OS3}$ | | | 250 | pSec | |
| Maximum PLL Lock Time[(1)] | tLOCK | | | 10 | ms | Stable power supply, valid clocks presented on REF pins |

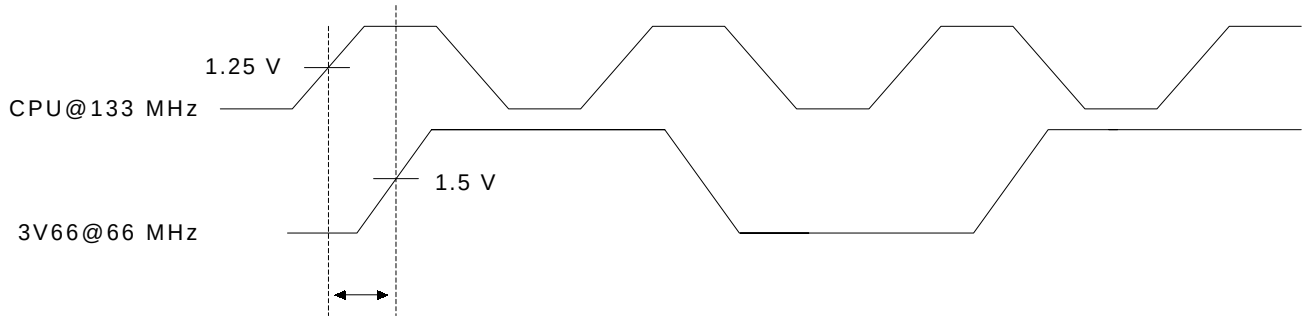
**Notes:**

1. Parameter is guaranteed by design and characterization. Not 100% tested in production. All parameters specified with equally loaded outputs, input rise/fall max 2nS.

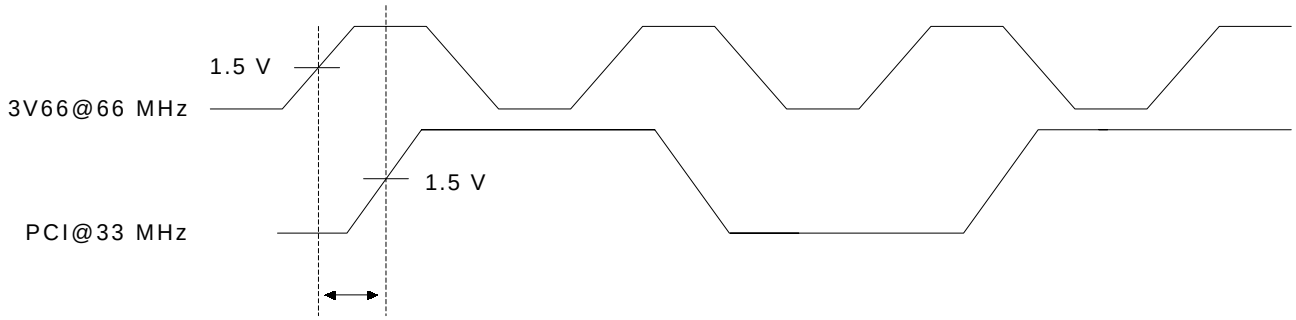
## Clock Group Offset Limits

| Clock Groups | Skew Offset | Conditions |
|---|---|---|
| CPU to 3V66 | 0.0 to 1.5 nSec, CPU Leads | CPU and IOAPIC clocks are measured at 1.25 Volts and at full rated capacitive loading. 3V66 and PCI clocks are measured at 1.5 Volts and at full rated capacitive loading. |
| 3V66 to PCI | 1.5 to 3.5 nSec, 3V66 Leads | |
| CPU to PCI | 1.5 to 3.5 nSec, CPU Leads | |
| CPU to IOAPIC | 1.5 to 3.5 nSec, CPU Leads | |

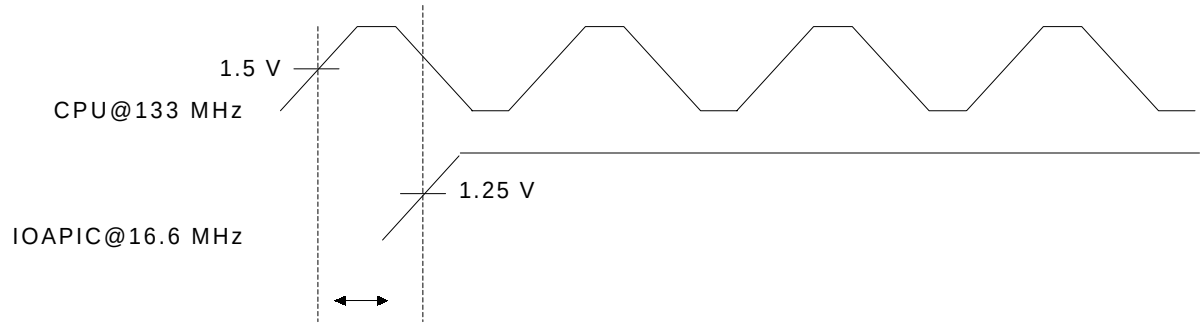
## Group Offset Waveforms




CPU leads 3V66

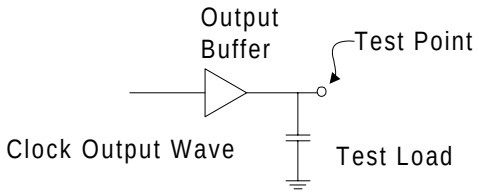


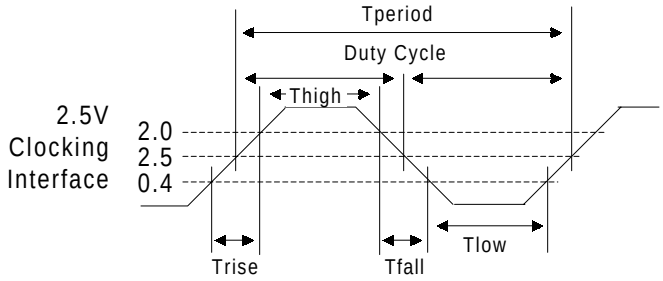

3V66 leads PCI

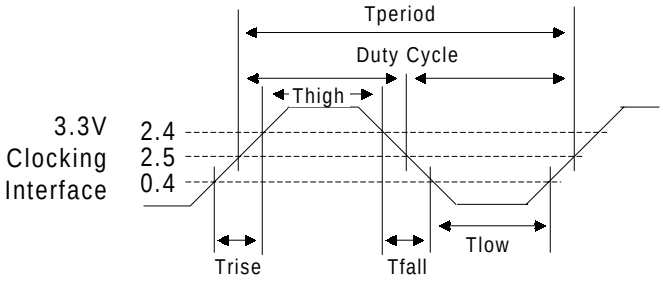



CPU leads IOAPIC

## Clock Waveforms for Single-Ended Clock Outputs

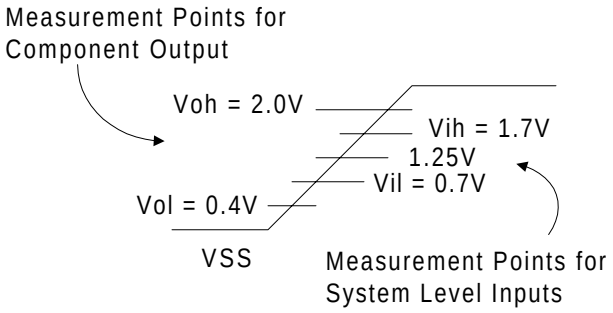


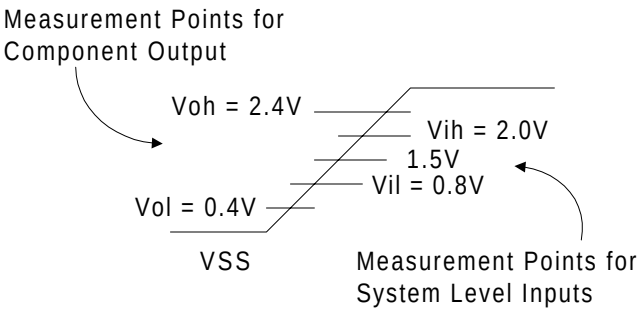




## Component Measurement for Single-Ended Output

**2.5 Volt Measure Points**




**3.3 Volt Measure Points**



## Buffer Characteristics for 3V48M, REF, PCI, 3V66M(0,1)

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-up Current[1] | $I_{ohmin}$ | -8 | - | - | mA | Vout = VDD – 0.5V |
| Pull-up Current[1] | $I_{ohmax}$ | - | - | -190 | mA | Vout = 1.2V |
| Pull-down Current[1] | $I_{olmin}$ | 9.4 | - | - | mA | Vout = 0.4V |
| Pull-down Current[1] | $I_{olmax}$ | - | - | 110 | mA | Vout = 1.2V |
| Output Rise Edge Rate[2] | $T_{rh}$ | 2.0 | - | - | nS | 3.3V ± 5% @ 0.4V – 2.4V |
| Output Fall Edge Rate[2] | $T_{fh}$ | 2.0 | - | - | nS | 3.3V ± 5% @ 2.4V – 0.4V |
| Output Impedance | $Z_o$ | 20 | | 60 | Ohm | 3.135V - 3.465V |

## Buffer Characteristics for CPU, DRCGREF, IOAPIC and 2V48M

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-up Current[1] | $I_{ohmin}$ | -12 | - | - | mA | Vout = VDD – 0.5V |
| Pull-up Current[1] | $I_{ohmax}$ | - | - | -101 | mA | Vout = 1.2V |
| Pull-down Current[1] | $I_{olmin}$ | 12 | - | - | mA | Vout = 0.4V |
| Pull-down Current[1] | $I_{olmax}$ | - | - | 93 | mA | Vout = 1.2V |
| 2.5V Type 1 Output Rise Edge Rate[2] | $T_{rh}$ | 2.0 | - | - | nS | 2.5V ± 5% @ 0.4V – 2.0V |
| 2.5V Type 1 Output Fall Edge Rate[2] | $T_{fh}$ | 2.0 | - | - | nS | 3.3V ± 5% @ 2.4V – 0.4V |
| Output Impedance | $Z_o$ | 13.5 | - | 45 | Ohm | 2.375V – 2.625V |

## Suggested Oscillator Crystal Parameters

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Frequency | $F_o$ | 12.00 | 14.31818 | 16.00 | MHz | |
| Tolerance | $T_C$ | - | - | +/-100 | PPM | Note 1 |
| | $T_S$ | - | - | +/- 100 | PPM | Stability ($T_A$ -10 to +60C) Note 1 |
| | $T_A$ | - | - | 5 | PPM | Aging (first year @ 25C) Note 1 |
| Operating Mode | - | - | - | - | | Parallel Resonant, Note 1 |
| Load Capacitance | $C_{XTAL}$ | - | 20 | - | pF | The crystal's rated load. Note 1 |
| Effective Series Resistance (ESR) | $R_{ESR}$ | - | 40 | - | Ohms | Note 2 |

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

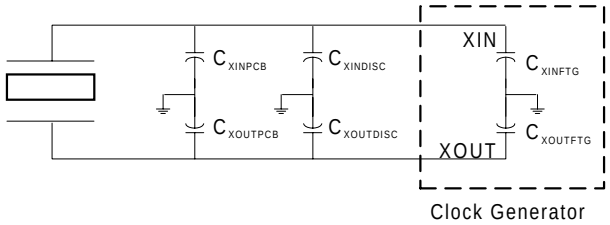
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to $C_{XTAL}$. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance ($C_{FTG}$), any circuit traces ($C_{PCB}$), and any onboard discrete load capacitors ($C_{DISC}$).

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

- $C_{XTAL}$ = the load rating of the crystal
- $C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
- $C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
- $C_{XINPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
- $C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
- $C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
- $C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground

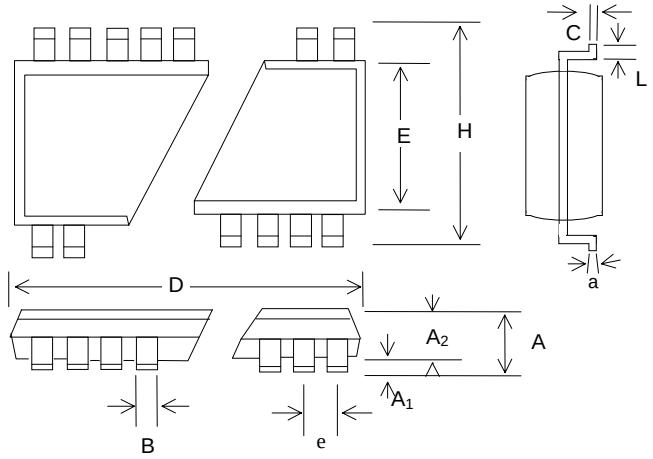



As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors ($C_{DISC}$) and each of the crystal to device PCB traces has a capacitance ($C_{PCB}$) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF. It is the intent of the internal device crystal loading capacitors to eliminate the need of device external crystal loading capacitors.

## Package Drawing and Dimensions




### 48 Pin SSOP Outline Dimensions

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.095 | 0.102 | 0.110 | 2.41 | 2.59 | 2.79 |
| $A_1$ | 0.008 | 0.012 | 0.016 | 0.20 | 0.31 | 0.41 |
| A2 | 0.085 | 0.090 | 0.095 | 2.16 | 2.29 | 2.41 |
| b | 0.008 | 0.010 | 0.0135 | 0.203 | 0.254 | 0.343 |
| c | 0.005 | .008 | 0.010 | 0.127 | 0.20 | 0.254 |
| D | 0.620 | 0.625 | 0.637 | 15.75 | 15.88 | 16.18 |
| E | 0.291 | 0.295 | 0.299 | 7.39 | 7.49 | 7.59 |
| e | 0.025 BSC | | | 0.635 BSC | | |
| H | 0.395 | 0.408 | 0.420 | 10.03 | 10.36 | 10.67 |
| L | 0.024 | 0.030 | 0.040 | 0.61 | 0.76 | 1.02 |
| a | 0º | 4º | 8º | 0º | 4º | 8º |

## Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| C9840AY | 48 Pin SSOP | Commercial, 0ºC to +70ºC |

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
C9840
Date Code, Lot #

C9840AY

- Package: Y = SSOP
- Revision
- IMI Device Number