…when timing is critical

C9836

Low EMI Clock Generator for Intel® Mobile 133MHz/2 SO-DIMM Chipset Systems

Preliminary

Product Features

- Meets Intel's Mobile 133.3MHz Chipset
- 2-CPU Clocks (66.6/100/133.3MHz, 2.5V)
- 4-SDRAM Clocks, 1-DCLK (100/133.3MHz, 3.3V)
- 7-PCI Clocks, One Free Running
- 3-REF Clocks
- 1-48MHz fixed non SSCG Clock (DOT)
- 3- 3V66 Clocks (66.6MHz, 3.3V) ICH, HUBLINK and AGP memory
- Power management using Power Down , CPU Stop and PCI Stop pins
- 3 Function Select pins (include test-mode select)
- IMI Spread Spectrum for best EMI reduction
- I^2C Support with read back
- 48 Pin SSOP and TSSOP Package

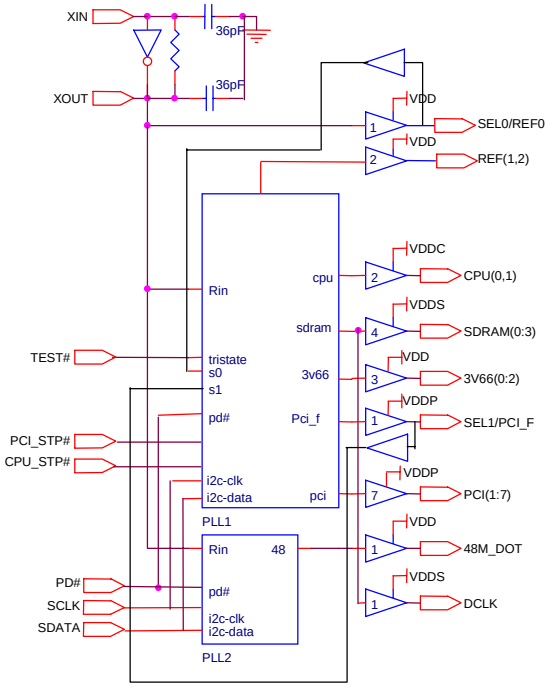
Function Table (MHz)

TEST#	SEL1	SEL0	CPU(0,1)	SDRAM(0:3), DCLK	3V66(0:2)	PCI(F,1:7)	48M_DOT	REF(0:2)
0	X	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	X	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK
1	0	0	66.6	100.0*	66.6	33.3	48	14.318
1	0	1	100.0	100.0*	66.6	33.3	48	14.318
1	1	0	133.3	133.3	66.6	33.3	48	14.318
1	1	1	133.3	100.0*	66.6	33.3	48	14.318

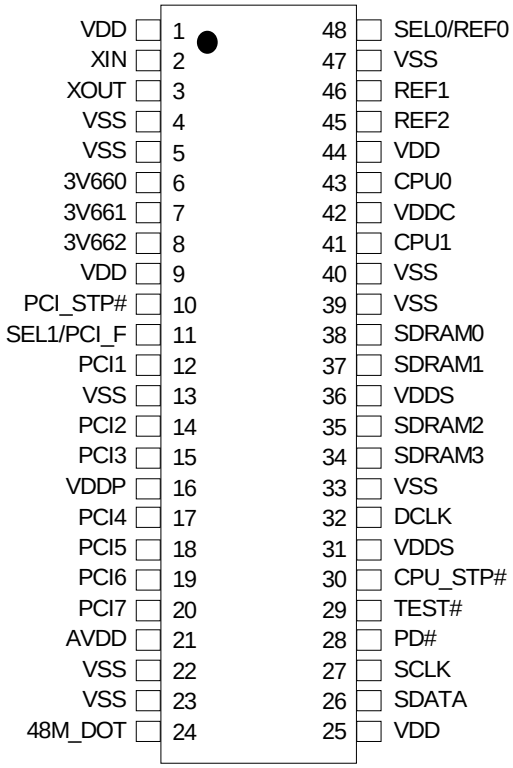
NOTE: These are the frequencies that are selectable after power up using the SEL1 and SEL0 hardware pins. Other frequencies may be chosen using the devices I^2C interface. See the expanded frequency for a complete listing of all of the availible frequencies.
*Will be set to 133MHz when I^2C Byte3, Bit 0 is set to logic 1.

Table 1

Block Diagram



Pin Configuration



Pin Description

PIN	NAME	PWR	TYPE	DESCRIPTION
48	**SEL0/REF0**	VDD	PU	Power-on Bi-directional Input / Output. At power-up, SEL0 is the input. When the power supply voltage crosses the input threshold voltage, REF0 becomes the output. See frequency Table for SEL0 selections.
45, 46	**REF(2,1)**	VDD		3.3V 14.318MHz clock output
2	**XIN**			Oscillator buffer input. Connect to a crystal or to an external clock.
3	**XOUT**			Oscillator buffer output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
41, 43	**CPU(1,0)**	VDDC		2.5V Host bus clock outputs
6, 7, 8	**3V66(0:2)**	VDD		3.3V Fixed 66.6MHz clock outputs
11	**SEL1/PCI_F**	VDDP	PU	Power-on Bi-directional Input / Output. At power-up, SEL1 is the input. When the power supply voltage crosses the input threshold voltage, PCI_F becomes a free running PCI clock. This clock continues to run when PCI_STP# is at a logic low level. See frequency Table for SEL1 selections.
12, 14, 15, 17, 18, 19, 20	**PCI (1:7)**	VDDP		3.3V PCI clock outputs. These clocks synchronously stop in a low state when PCI_STP# is brought to a logic low level. They synchronously resume running when PCI_STP# is brought to a logic high state.
24	**48M_DOT**	VDD		3.3V Fixed 48MHz clock outputs
30	**CPU_STP#**			CPU0 stop clock control input. When this signal is at a logic low level (0), CPU0 clock stops at a logic low level. Using this pin to start and stop CPU0 clock insures synchronous (no short or long clocks) transitioning of this clock.
10	**PCI_STP#**			PCI stop clock control input. When this signal is at a logic low level (0), all PCI clocks (except PCI_F) stop at a logic low level. Using this pin to start and stop PCI clocks insures synchronous (no short or long clocks) transitioning of these clocks. This pin has no effect on the PCI_F clock.
26	**SDATA**			Serial data input pin. Conforms to the Philips I^2C specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See I^2C function description.
27	**SCLK**			Serial clock input pin. Conforms to the Philips I^2C specification. See I2C function description.
28	**PD#**		PU	3.3V LVTTL compatible input. When held LOW, the device enters a power down mode. This pin has an Internal Pull-Up. See power management function.
29	**TEST#**			3.3V LVTTL compatible input for selecting test mode. See Table 1.
32	**DCLK**	VDDS		3.3V SDRAM feedback clock output. See Table1 for frequency selection. See figure 4 for timing relationship.
34, 35, 37, 38	**SDRAM(3:0)**	VDDS		3.3V SDRAM clock outputs
42	**VDDC**			2.5V Power for CPU clock output buffers
31, 36	**VDDS**			3.3V Power for SDRAM and DCLK clock output buffers
16	**VDDP**			3.3V Power for PCI clock output buffers
21	**AVDD**			3.3V Analog Power Supply
1, 9, 25, 44	**VDD**			3.3V Common Power Supply
4, 5, 13, 22, 23, 33, 39, 40, 47	**VSS**			Common Ground pins.

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

PU = Internal Pull-Up. Typically 350k (range 200k to 500k).

Expanded Frequency Selection (MHz) [1,2]

TEST #	ESEL 1	ESEL 0	SEL 1	SEL 0	CPU (0,1)	SDRAM (0:3), DCLK	3V66 (0:2)	PCI_F, PCI(1:7)	Notes
1	0	0	0	0	66.7	100*	66.6	33	0% extension (Default)
	0	0	0	1	100	100*	66.6	33	
	0	0	1	0	133.3	133.3	66.6	33	
	0	0	1	1	133.3	100*	66.6	33	
	0	1	0	0	70	105*	70	35	5% extension
	0	1	0	1	105	105*	70	35	
	0	1	1	0	140	140	70	35	
	0	1	1	1	140	105*	70	35	
	1	0	0	0	73.3	110*	73.3	36.6	10% extension
	1	0	0	1	110	110*	73.3	36.6	
	1	0	1	0	146.7	146.7	73.3	36.6	
	1	0	1	1	146.7	110*	73.3	36.6	
	1	1	0	0	80	120*	80	40	20% extension
	1	1	0	1	120	120*	80	40	
	1	1	1	0	160	160	80	40	
	1	1	1	1	160	120*	80	40	

Note 1: Extended frequencies are only available via I^2C interface. They are accessable via I^2C Byte 5 bits 0,1.
Note 2: 48M_DOT clock is constant at 48MHz and REF is constant at 14.31818MHz for all table selections.
*Will be set to 133MHz and boosted accordingly, when Byte3, Bit0 is set to logic 1.

Table 2

Power Management Functions

Power Management on this device is controlled by the PD#, CPU_STP# and PCI_STP# pins. When PD# is high (default) the device is in normal running mode and all signals are active.

The PD# signal is used to bring all clocks to a low level in an orderly fashion prior to power (all except AVDD) being removed from the part. When PD# is asserted (forced) low, the device transitions to a shutdown (power down) mode and all power supplies (3.3V and 2.5V except for AVDD) may then be removed. When PD# is sampled low by two consecutive rising edges of the CPU clock, then all affected clocks are stopped in a low state on their next high-to-low transition. The REF and DOT clocks are stopped in a low state as soon as possible. When in power down (and before power is removed), all outputs are synchronously stopped in a low state (see Figure 1 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I²C function is also disabled.

At power up, using the PD# select pin, all clocks are started in such a manner as to guarantee a glitch free operation, no partial clock pulses.

Power Management Timing

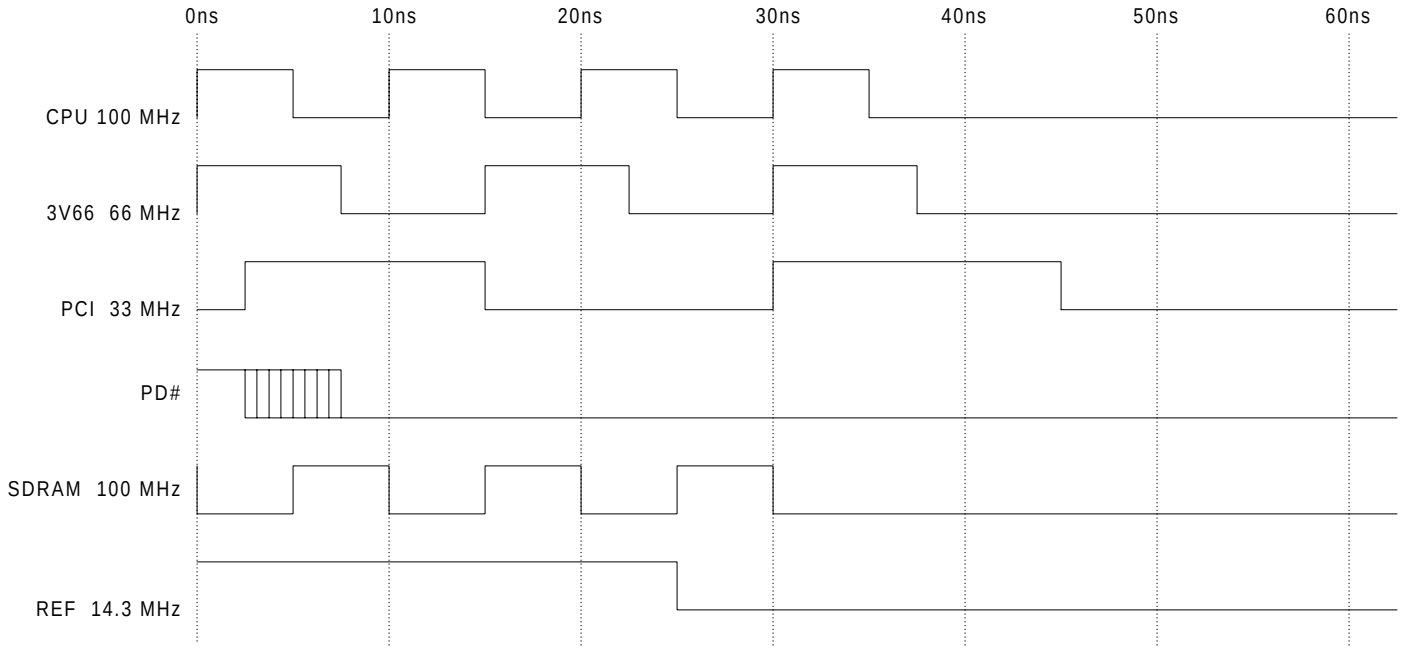


Figure 1

Power Management Current

CONDITIONS	Maximum 2.5 Volt Current Consumption (VDDC = 2.625V)	Maximum 3.3 Volt Current Consumption (VDD = AVDD = VDDS = 3.465V)
Power down (PD# = LOW)	≤ 1mA	≤ 1mA
CPU=66MHz @ max loads	**60mA (Preliminary)**	**160mA (Preliminary)**
CPU=100MHz @ max loads	**75mA (Preliminary)**	**160mA (Preliminary)**
CPU=133MHz @ max loads	**90mA (Preliminary)**	**160mA (Preliminary)**

Table 3

When exiting the power down mode, the application must supply power to the VDD pins a minimum of 200ms before releasing the PD# pin high to insure that an orderly startup will occur and that the initial clocks that the device produces are full and correctly compliant with data sheet specified phase relationships.

CPU_STP# Timing

CPU_STP# is an input to the clock generator. CPU_STP# is asserted asynchronously by the external clock control logic and is internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU0 clock is disabled. The CPU0 is always stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. Only one rising edge of PCI_F occurs after the clock control logic is switched for the CPU0 output to become enabled/disabled.

CPU_STP# Timing Diagram

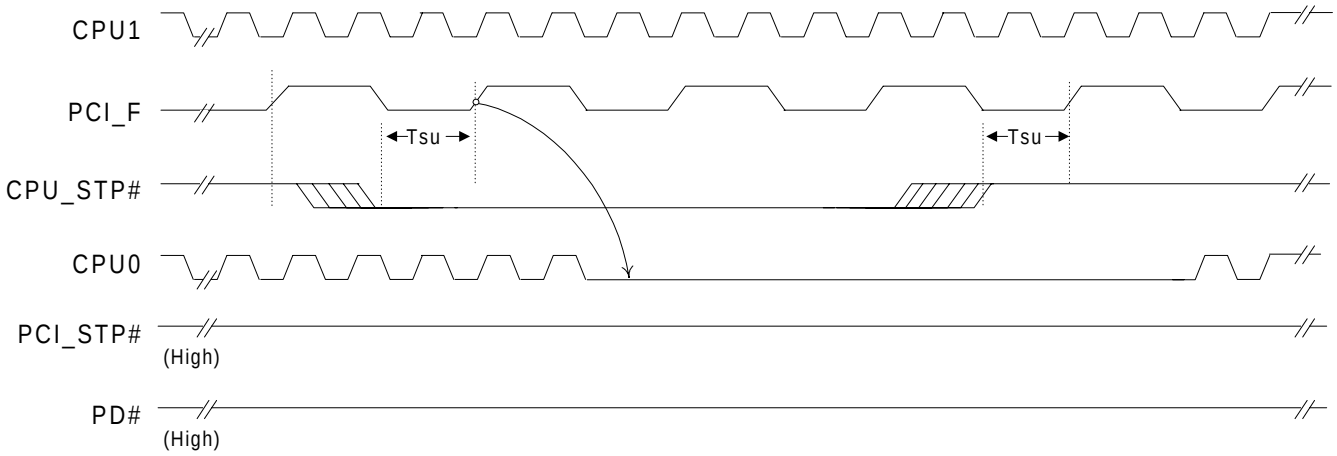


Figure 2

Notes:
1. All internal timing is referenced to the CPU Clock.
2. CPU_STP# signal is an input signal that is made synchronous to free running PCI_F.
3. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

PCI_STP# Timing

PCI_STP# is an input to the clock generator and is made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are stopped in a low state and started such that a full high pulse width is guaranteed. ONLY one rising edge of PCI_F occurs after the clock control logic switched for the PCI outputs to become enabled/disabled.

PCI_STP# Timing Diagram

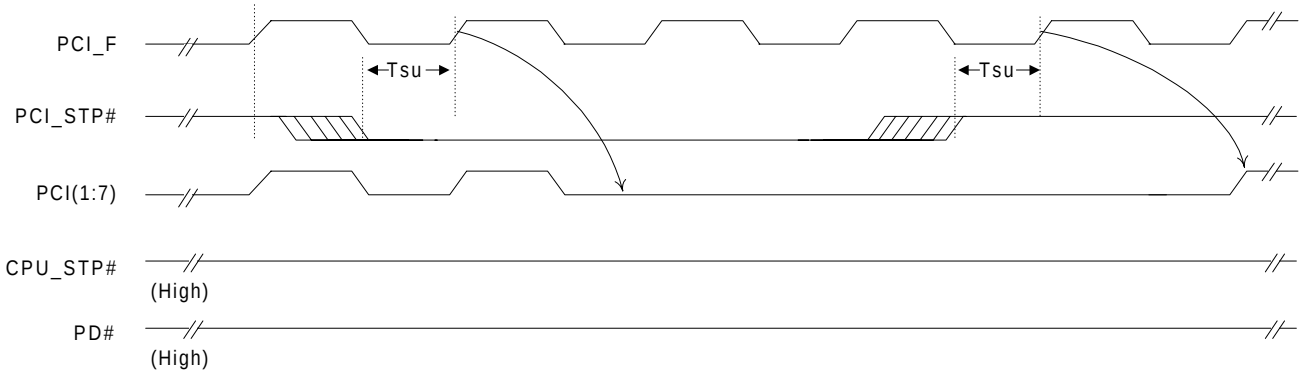


Figure 3

Notes:

1. All internal timing is referenced to the CPU clock.
2. PCI_STP# signal is an input signal which must be made synchronous to PCI_F output.
3. All other clocks continue to run undisturbed.
4. PD# is understood to be in a high state.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

Clock Phase Relationships

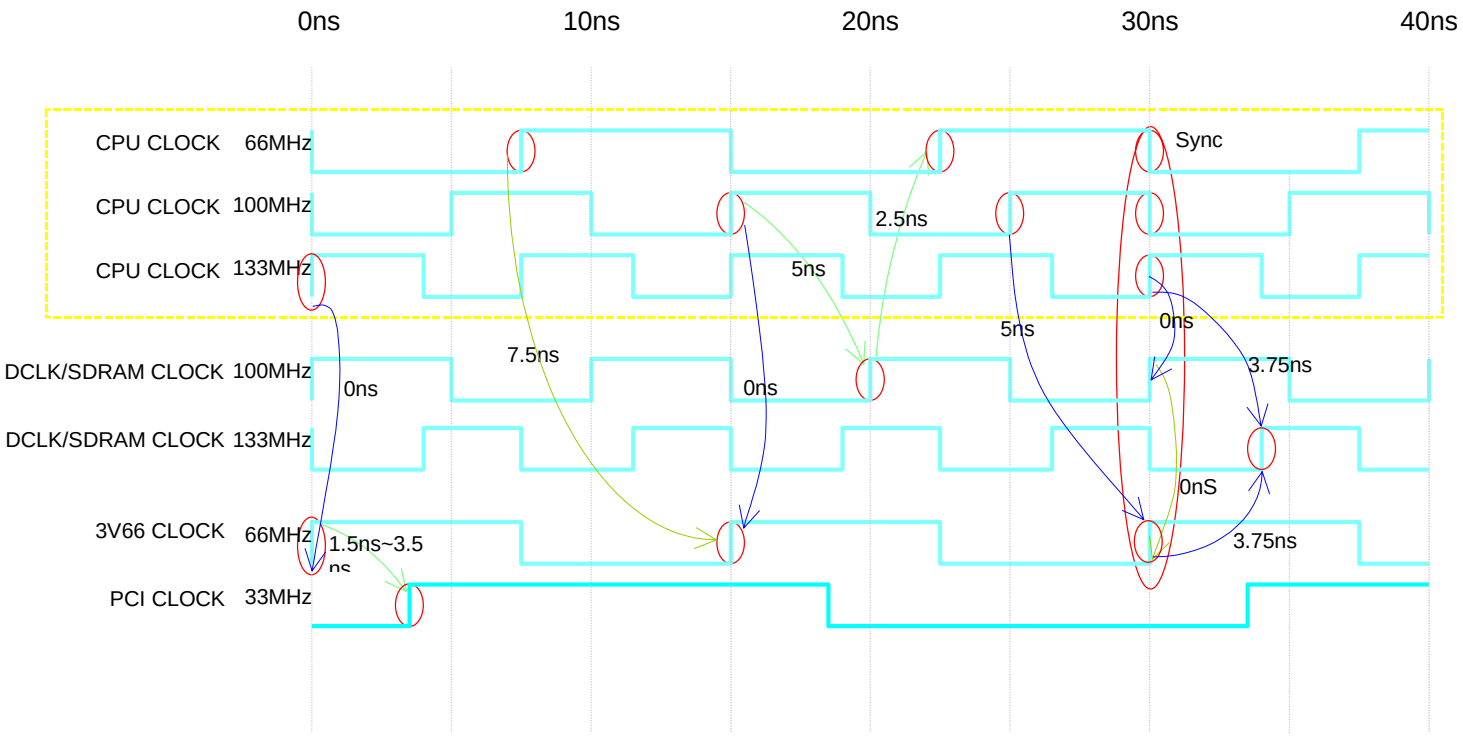


Figure 4

Group Timing Relationships and Tolerances

	CPU = 66.6MHz, SDRAM = 100MHz		
	Offset (ns)	**Tolerance (ps)**	**Conditions**
CPU to SDRAM/DCLK	2.5	500	
CPU to 3V66	7.5	500	180 degrees phase shift
SDRAM/DCLK to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
48M_DOT	Async	N/A	
	CPU = 100MHz, SDRAM = 100MHz		
	Offset (ns)	**Tolerance (ps)**	**Conditions**
CPU to SDRAM/DCLK	5	500	180 degrees phase shift
CPU to 3V66	5	500	CPU leads
SDRAM/DCLK to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
48M_DOT	Async	N/A	
	CPU = 133.3MHz, SDRAM = 100MHz		
	Offset (ns)	**Tolerance (ps)**	**Conditions**
CPU to SDRAM/DCLK	0	500	When rising edges line-up
CPU to 3V66	0	500	
SDRAM/DCLK to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
48M_DOT	Async	N/A	
	CPU = 133.3MHz, SDRAM = 133.3MHz		
	Offset (ns)	**Tolerance (ps)**	**Conditions**
CPU to SDRAM/DCLK	3.75	500	180 degrees phase shift
CPU to 3V66	0	500	
SDRAM/DCLK to 3V66	3.75	500	
3V66 to PCI	1.5-3.5	500	3V66 leads
48M_DOT	Async	N/A	

Table 4

2-Wire I²C Control Interface

The 2-wire control interface implements a read/write slave only interface according to Philips I²C specification. (See Figure 5 below). The device can be read back by using standard I²C command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/s (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. The LSB address Byte = 0 in write mode.

The device will respond to transfers of 10 bytes (max) of data. The device will generate an acknowledge (low) signal on SDATA following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/s. This device will also respond to a D3 address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

When a clock driver is placed in power down mode, the I²C signals SDATA and SCLK must be tri-stated. In power down, the device retains all I²C programming information.

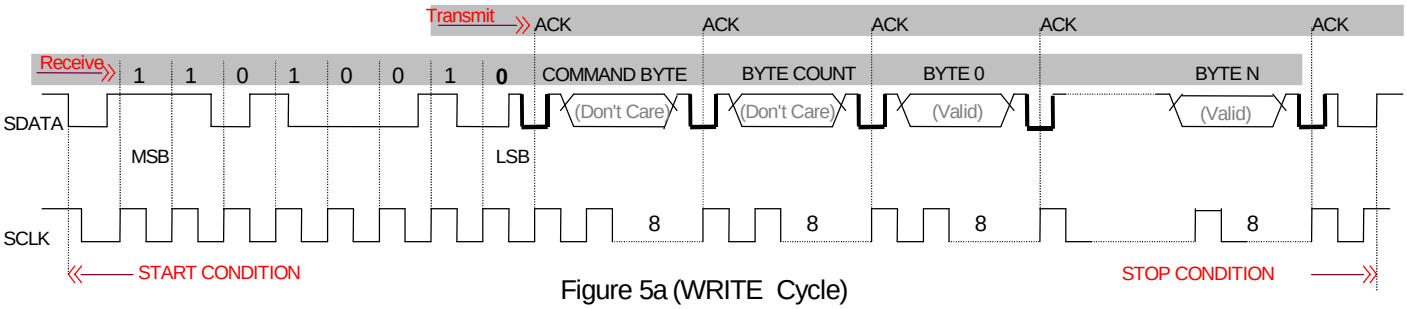


Figure 5a (WRITE Cycle)

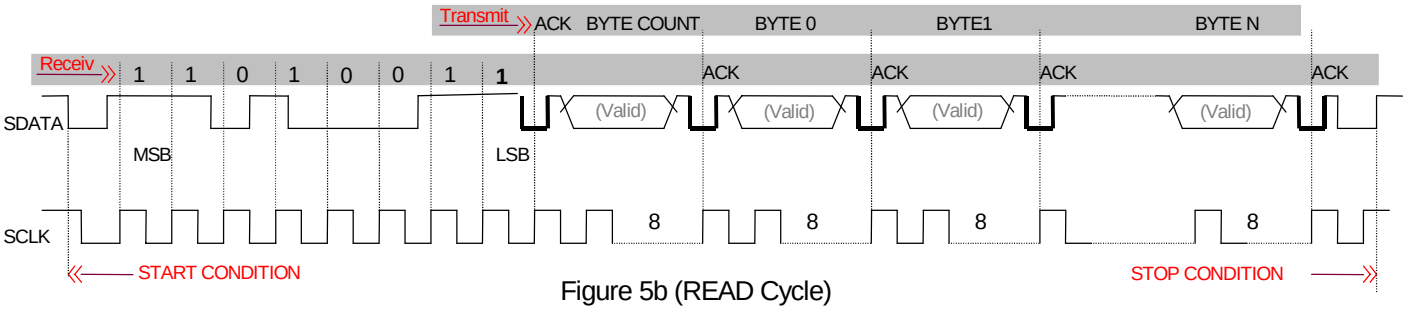


Figure 5b (READ Cycle)

Figure 5. I²C Communications Waveforms

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

Byte 0: CPU Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	-	Reserved. Don't Care
6	1	-	Reserved. Don't Care
5	1	41	CPU1
4	1	43	CPU0
3	0	-	Spread spectrum (1 = enabled)
2	1	24	48M1(DOT)
1	1	-	Reserved. Don't Care
0	0	-	Reserved. Set to 0

Byte 1: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	Reserved. Set to 0
6	0	-	Reserved. Set to 0
5	1	-	Reserved. Don't Care
4	1	-	Reserved. Don't Care
3	1	34	SDRAM3
2	1	35	SDRAM2
1	1	37	SDRAM1
0	1	38	SDRAM0

Byte 2: 3V66 Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	8	3V66_2 (AGP)
6	1	7	3V66_1
5	1	6	3V66_0
4	0	-	Reserved. Set to 0
3	0	-	Reserved. Set to 0
2	0	-	Reserved. Set to 0
1	0	-	Reserved. Set to 0
0	0	-	Reserved. Set to 0

Byte 3: PCI Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	20	PCI7
6	1	19	PCI6
5	1	18	PCI5
4	1	17	PCI4
3	1	15	PCI3
2	1	14	PCI2
1	1	12	PCI1
0	0	-	SDRAM 133MHz Mode Enable. Default is disabled = '0', enabled = '1'

Byte 4: Reserved Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	Reserved. Set to 0
6	0	-	Reserved. Set to 0
5	0	-	Reserved. Set to 0
4	0	-	Reserved. Set to 0
3	0	-	Reserved. Set to 0
2	0	-	Reserved. Set to 0
1	0	-	Reserved. Set to 0
0	0	-	Reserved. Set to 0

Byte 5: SSCG Control Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	0	-	Spread Mode (0=down, 1=center)
6	0	-	Selects spread bandwidth. See Table 5
5	0	-	Selects spread bandwidth. See Table 5
4	0	-	Reserved. Set to 0
3	0	-	Reserved. Set to 0
2	0	-	Reserved. Set to 0
1	0	-	ESEL1 Expanded Freq. Selection MSB, See Table 2
0	0	-	ESEL0 Expanded Freq. Selection LSB, See Table 2

Note: The Pin# column lists the relevant pin number where applicable. The @Pup column gives the default state at power up.

I²C Test Circuitry

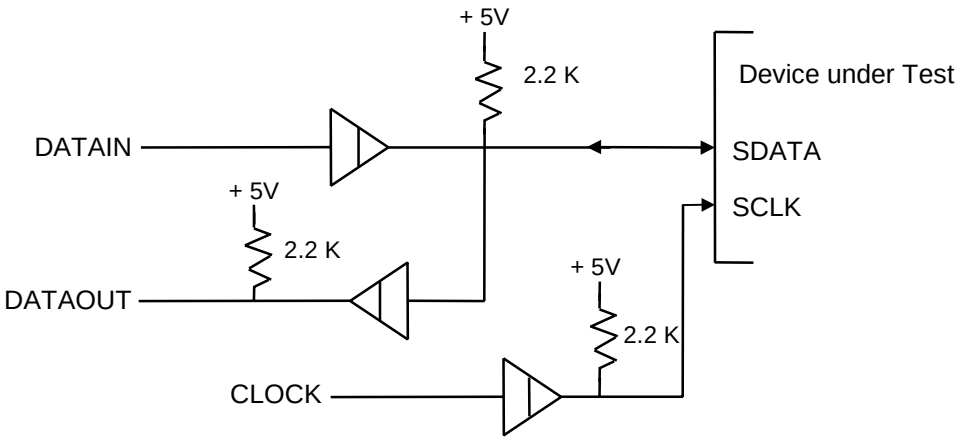


Figure 6

Note: Buffer is 7407 with VCC @ 5.0V

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated by repetitive digital signals, mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore distributing an even amount of energy over a wider spectrum. This technique is achieved by modulating the clock either down (Figure 7a) or around the center (Figure 7b) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting I²C Byte0, bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have I²C accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST(0:2) in I²C Byte 5, bits 5, 6 & 7 following tables 5a, and 5b below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (e.g.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

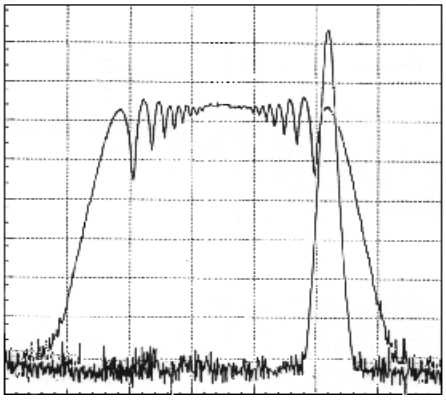


Figure 7a

Center Spread

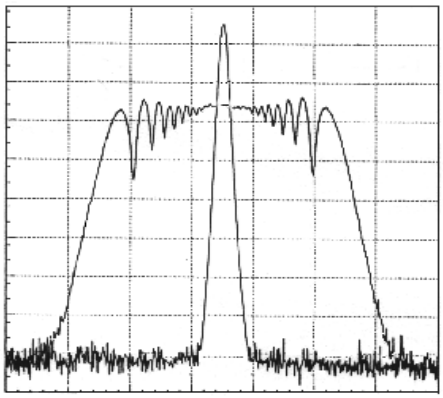


Figure 7b

Spread Spectrum Selection Tables

I²C BYTE 5 Bit		Spread %
6	5	
0	0	- 0.5
0	1	- 0.7
1	0	- 1.0
1	1	- 1.5

Table 5a
(I²C BYTE 5 Bit 7=0), Down Spread

I²C Byte 5 Bit		Spread %
6	**5**	
0	0	± 0.25
0	1	± 0.35
1	0	± 0.5
1	1	±0.75

Table 5b
(I²C BYTE 5 Bit 7=1), Center Spread

Preliminary

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: 0°C to +70°C
Maximum ESD Protection 2KV
Maximum Power Supply: 5.5V

This device contains circuitry that protects the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (All outputs loaded per Table 6 below)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	V	Note 1
Input High Voltage	VIH1	2.0	-	-	V	
Input Low Voltage	VIL2	-	-	1.0	V	Note 2
Input High Voltage	VIH2	2.2	-	-	V	
Input Low Current (@VIL = VSS)	IIL1			-5	µA	For internal Pull up resistors, Note 3
Input High Current (@VIH =VDD)	IIH1			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	160	mA	
Dynamic Supply Current	Idd2.5V	-	-	60	mA	CPU @ 66MHz
		-	-	75	mA	CPU @ 100MHz
		-	-	90	mA	CPU @ 133MHz
Power Down Supply Current	Ipd3.3V			1	mA	PD# = '0'
Power Down Supply Current	Ipd2.5V			1	mA	PD# = '0'
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	34	36	38	pF	Measured from Pin to Ground. Note 4
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µs	From Stable 3.3V power supply.
VDD = VDDS = VDDP = AVDD = 3.3V ±5%, VDDC = 2.5V ± 5%, TA = 0°C to +70°C						

Note 1: Applicable to input signals: SEL(0,1), PD# (pull up), PCI_STP#, CPU_STP#
Note 2: Applicable to SDATA, and SCLK.
Note 3: Internal Pull up and Pull down resistors have a typical value of 350k (200K and 500K).
Note 4: See applications data that is presented later in this data sheet on crystal interfacing.

AC Parameters

Symbol	Parameter	133MHz Host		100MHz Host		66MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	CPU(0,1) period[5,6]	7.5	8.0	10.0	10.5	15.0	15.5	ns
THIGH	CPU(0,1) high time[10]	1.87	-	3.0	-	5.2	-	ns
TLOW	CPU(0,1) low time[11]	1.67	-	2.8	-	5.0	-	ns
Tr / Tf	CPU(0,1) rise and fall times[7]	0.4	1.6	0.4	1.6	0.4	1.6	ns
TSKEW	Any CPU to any CPU Skew[6,9]	-	150	-	150	-	150	ps
TCCJ	CPU(0,1) Cycle to Cycle Jitter[6,9]	-	250	-	250	-	250	ps
TPeriod	SDRAM(0:3) 100MHz and DCLK period[5,6]	10.0	10.5	10.0	10.5	10.0	10.5	ns
THIGH	SDRAM(0:3) 100MHz and DCLK high time[10]	3.0	-	3.0	-	3.0	-	ns
TLOW	SDRAM(0:3) 100MHz and DCLK low time[11]	2.8	-	2.8	-	2.8	-	ns
Tr / Tf	SDRAM(0:3) 100MHz and DCLK rise and fall times[7]	0.4	1.6	0.4	1.6	0.4	1.6	ns
TSKEW	SDRAM(0:3) 100MHz and DCLK Skew[6,9]	-	250	-	250	-	250	ps
TCCJ	SDRAM(0:3) 100MHz, DCLK Cycle to Cycle Jitter[6,9]	-	250	-	250	-	250	ps
TPeriod	3V66-(0:2) period[5,6]	15.0	16.0	15.0	16.0	15.0	16.0	ns
THIGH	3V66-(0:2) high time[10]	5.25	-	5.25	-	5.25	-	ns
TLOW	3V66-(0:2) low time[11]	5.05	-	5.05	-	5.05	-	ns
Tr / Tf	3V66-(0:2) rise and fall times[7]	0.5	2.0	0.5	2.0	0.5	2.0	ns
TSKEW	(Any 3V66) to (any 3V66) Skew[6,9]	-	175	-	175	-	175	ps
TCCJ	3V66-(0:2) Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	ps
TPeriod	PCI(_F,1:7) period[5,6]	30.0	-	30.0	-	30.0	-	ns
THIGH	PCI(_F, 1:7) high time[10]	12.0	-	12.0	-	12.0	-	ns
TLOW	PCI(_F, 1:7) low time[11]	12.0	-	12.0	-	12.0	-	ns
Tr / Tf	PCI(_F, 1:7) rise and fall times[7]	0.5	2.0	0.5	2.0	0.5	2.0	ns
TSKEW	(Any PCI) to (Any PCI) Skew[6,9]	-	500	-	500	-	500	ps
TCCJ	PCI(_F, 1:7) Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	ps
TPeriod	DOT (48M) period (conforms to +167ppm max) [5,6]	20.8299	20.8333	20.8299	20.8333	20.829	20.833	ns
Tr / Tf	DOT rise and fall times[7]	1.0	4.0	1.0	4.0	1.0	4.0	ns
TCCJ	DOT Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	ps

Symbol	Parameter	133MHz Host		100MHz Host		66MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	REF period[5,6]	69.8413	71.0	69.8413	71.0	69.8413	71.0	ns
Tr / Tf	REF rise and fall times[7]	1.0	4.0	1.0	4.0	1.0	4.0	ns
TCCJ	REF Cycle to Cycle Jitter[6]	-	1000	-	1000	-	1000	ps
tpZL, tpZH	Output enable delay (all outputs)[8]	1.0	10.0	1.0	10.0	1.0	10.0	ns
tpLZ, tpHZ	Output disable delay (all outputs)[13]	1.0	10.0	1.0	10.0	1.0	10.0	ns
tstable	All clock Stabilization from power-up[12]		3		3		3	ms
Tduty	Duty Cycle for All outputs[14]	45	55	45	55	45	55	%

Note 5: This parameter is measured as an average over 1us duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per Table 6 below. Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals (figures 8a and 8b).
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Figures 8a and 8b)
Note 8: Measured from when both SEL1 and SEL0 are switched to high (enable).
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figures 8a and 8b)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when both SEL1 and SEL0 are switched to low (disable).
Note 14: Device designed for Typical Duty Cycle of 50%.

Clock Name	Max Load (in pF)
CPU(0,1), REF(0:2)	20
PCI(_F, 1:7), SDRAM(0:3), DCLK, 3V66(0:2)	30
48M_DOT	15

Table 6.

Output Buffer Characteristics

CPU

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-15	-31	-51	mA	Vout =VDDC - 0.5V (or VDDI –0.5V)
Pull-Up Current	IOH_2	-26	-58	-101	mA	Vout = 1.2V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4V
Pull-Down Current	IOL_2	27	56	93	mA	Vout = 1.2V
Output Impedance	Z0	13.5		45	Ω	

PCI, 3V66

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-25	-33	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5V
Output Impedance	Z0	12		55	Ω	

REF, 48M1(DOT)

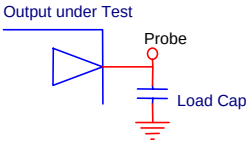
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-12	-16	-28	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5V
Output Impedance	Z0	20		60	Ω	

SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-28	-40	-60	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-67	-107	-184	mA	Vout = 1. 5V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4V
Pull-Down Current	IOL_2	64	98	159	mA	Vout = 1.5V
Output Impedance	Z0	10		24	Ω	
VDD=VDDS=VDDP=AVDD=3.3V ±5%, VDDC=2.5V±5%, TA=0°C to 70°C						

Table 7

Test and Measurement Condition



3.3V signals

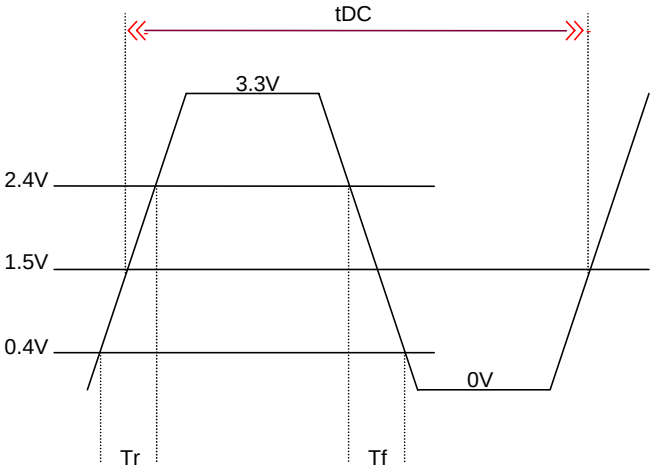


Figure 8a

2.5V signals

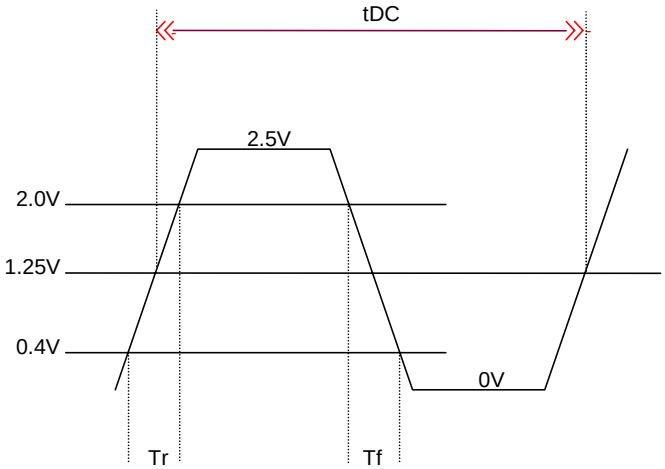


Figure 8b

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	14.17	14.31818	14.46	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Stability	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

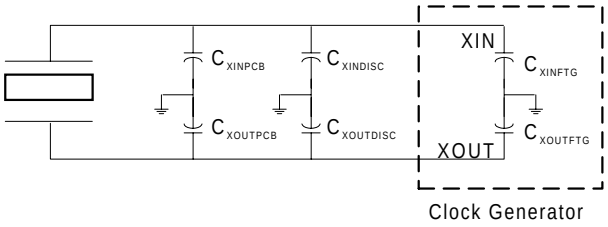
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit trace capacitance (C_{PCB}), and any onboard discrete load capacitance (C_{DISC}).

The following formula and schematic illustrates the application of the loading specification of a crystal (C_{XTAL})for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground



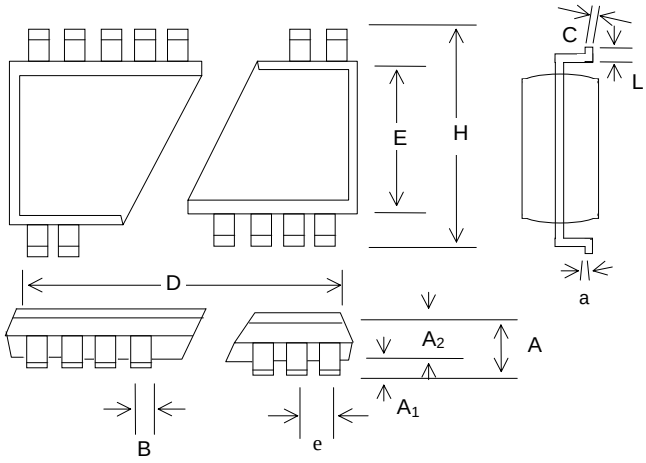
As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF.

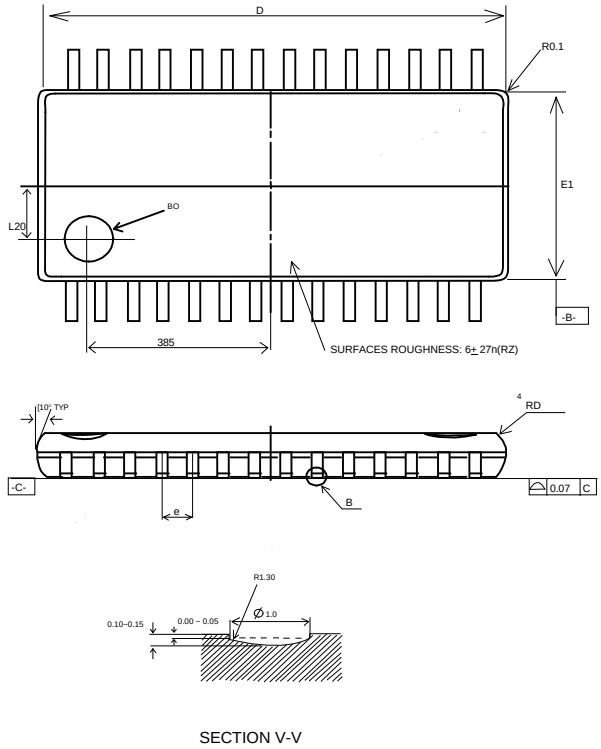
Preliminary

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	0.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.630	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.635 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.020	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º



SECTION V-V

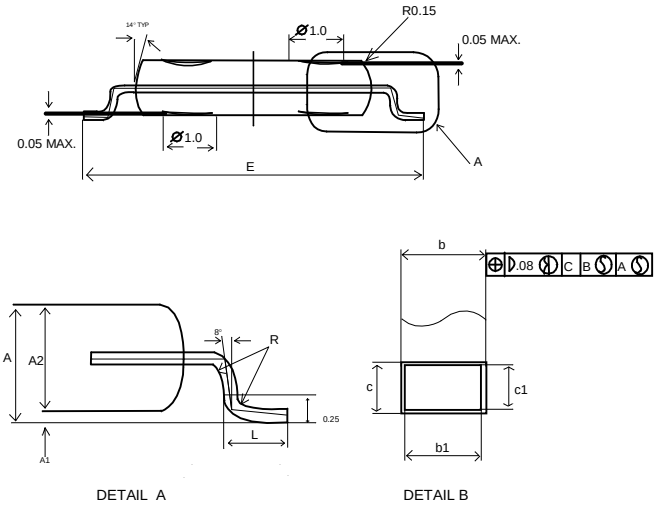
48 Pin TSSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.0433	-	-	1.10
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.033	0.035	0.037	0.85	0.90	0.95
L	0.019	0.023	0.029	0.50	0.60	0.75
R	0.043	-	-	0.10	-	-
b	0.006	-	0.010	0.170	-	0.27
b1	0.006	0.008	0.009	0.170	0.20	0.225
c	0.004	-	0.007	0.105	-	0.175
c1	0.004	0.005	0.006	0.105	0.125	0.145
θ	0°	-	8°			
e	0.020 BSC			0.50 BSC		
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.313	0.319	0.325	7.95	8.1	8.25
E1	0.236	0.240	0.244	6.00	6.1	6.20

Preliminary

Package Drawing and Dimensions (Cont.)

(48 Pin TSSOP



Ordering Information

Part Number	Package Type	Production Flow
C9836AY	48 PIN SSOP	Commercial, 0° to 70°C
C9836AT	48 PIN TSSOP	Commercial, 0° to 70° C

Marking: Example: IMI
C9836
Date Code, Lot #

IMIC9836AY

Package
Y = SSOP
T = TSSOP

Revision

IMI Device Number