C9834

Low EMI Clock Generator for Intel 810 Chipset / Pentium® II and Pentium® III Systems

Preliminary

Product Features

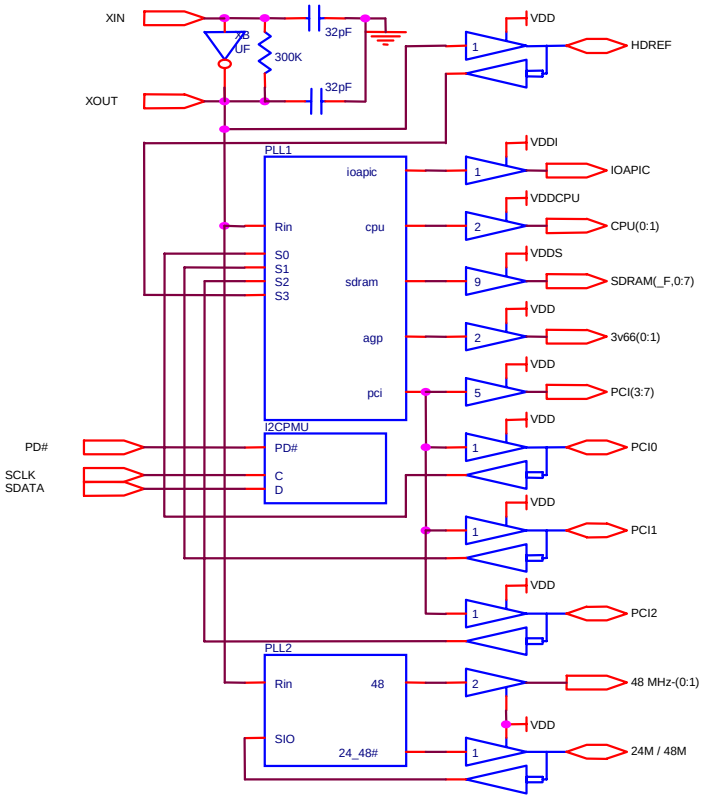
- Supports Pentium® II and Pentium® III processors
- Designed to the Intel 810 chipset specifications
- Low Jitter, High Speed Host Bus Clock (155Mhz)
- I²C for programmability and power management
- < 175pS Skew.
- 2 CPU at 2.5V
- 1 IOAPIC at 2.5V
- 9 SDRAM clocks at 3.3V
- 2 3V66 at 3.3V, for Graphics
- 8 PCI clocks at 3.3V
- 2 48 MHz at 3.3V fixed
- 1 24_48 MHz at 3.3V programmable
- 1 Ref at 3.3V , 14.318 MHz
- Wide range of selectable frequencies
- Available in 48 pin SSOP (300 mills)
- IMI Spread Spectrum for EMI reduction

Frequency Table MHz

S(4:0)	CPU	SDRAM	3V66	PCI	IOAPIC
00000	83.33	125.00	83.33	41.67	20.83
00001	90.00	135.00	90.00	45.00	22.50
00010	75.33	113.00	75.33	37.67	18.83
00011	150.00	150.00	75.00	37.50	18.75
00100	150.00	75.00	50.00	25.00	12.50
00101	166.67	83.33	55.56	27.78	13.89
00110	180.00	90.00	60.00	30.00	15.00
00111	190.00	95.00	63.33	31.67	15.83
01000	200.00	100.00	66.67	33.33	16.67
01001	114.00	114.00	76.00	38.00	19.00
01010	110.00	110.00	73.33	36.67	18.33
01011	125.00	125.00	62.50	41.67	20.83
01100	66.80	100.20	66.80	33.40	16.70
01101	100.20	100.20	66.80	33.40	16.70
01110	133.60	133.60	66.80	33.40	16.70
01111	133.60	100.20	66.80	33.40	16.70
10000	125.00	125.00	83.33	41.67	20.83
10001	127.00	127.00	84.67	42.33	21.17
10010	127.00	95.25	63.50	31.75	15.88
10011	72.00	108.00	72.00	36.00	18.00
10100	140.00	140.00	93.33	46.67	23.33
10101	140.00	105.00	70.00	35.00	17.50
10110	145.00	145.00	96.67	48.33	24.17
10111	129.00	96.75	64.50	32.25	16.13
11000	121.00	121.00	80.67	40.33	20.17
11001	117.00	117.00	78.00	39.00	19.50
11010	112.00	112.00	74.67	37.33	18.67
11011	107.00	107.00	71.33	35.67	17.83
11100	190.00	190.00	95.00	47.50	23.75
11101	166.67	166.67	83.33	41.67	20.83
11110	180.00	180.00	90.00	45.00	22.50

Table 1

Block Diagram



Pin Configuration

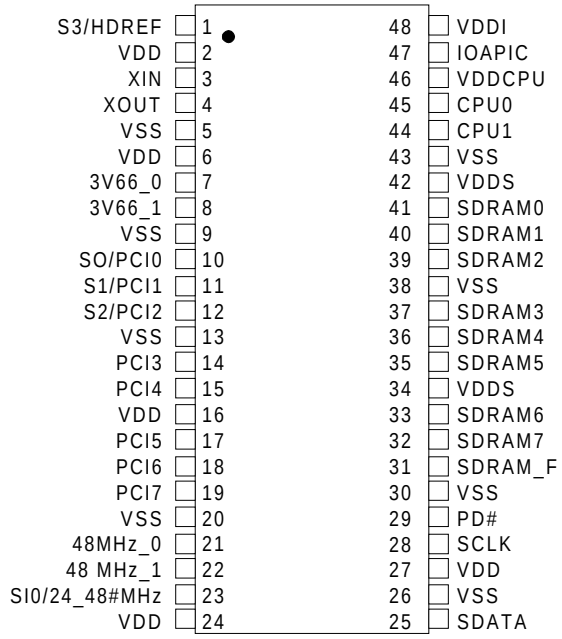


Fig. 2

Pin Description

PIN No.	Pin Name	PWR	TYPE	Description
1	**S3 / HDREF**	VDD	PU	This is a bi-directional pin. See page 3 for input strapping. When this pin is an input, it functions as part of the frequency selection address,S3 (see Table 1,p1). When it is an output, it is HDREF a high drive buffered output of the signal applied at Xin
3	**XIN**	VDD	OSC1	14.318 MHz Crystal input. See Crystal Spec. page 11.
4	**XOUT**	VDD	OSC1	14.318 MHz Crystal output
7, 8	**3V66 (0,1)**	VDD		3.3 V AGP clock outputs, Synchronous to CPU clocks, see table 1 page1.
10, 11, 12	**S0 / PCI0** **S1 / PCI1** **S2 / PCI2**		PU PD PU	These are bi-directional pins. See Application Note,p.3, for input strapping. When they are in input mode, they function as the frequency selectors S0,S1,S2 (see Table 1,p1). When they are in output mode, they function as PCI(0:2) clock outputs, and they are synchronous to the CPU clocks.
14, 15, 17, 18, 19	**PCI (3:7)**	VDD		3.3 V PCI clock outputs, they are synchronous to CPU clocks. See page 9 for timing.
21, 22	**48MHz-(0:1)**			These are fixed 48MHz outputs for USB and HUB clocks.
23	**24M_48MHz / SIO**		PU	This is a bi-directional pin. See Application Note,p.3, for input strapping. When this pin is an input, it functions as a SIO select pin for selecting the clock frequency at this same pin. If SIO is strapped high, then output = 24 MHz. If SIO is strapped low, then output = 48MHz.
25	**SDATA**	VDD	PU	Serial data input pin. Conforms to the Philips I²C specification of a Slave Receiver device. This pin is an input when receiving data. It is an open drain output when acknowledging. See I²C function description,p.5.
28	**SCLK**	VDD	PU	Serial clock input pin. Conforms to the Philips I²C 100KHz Specs.
29	**PD#**	VDD	PU	When this input pin is asserted low, the device is in Power Down mode; all outputs are held low, and internal PLL's are shutoff.(see p.4)
47	**IOAPIC**	VDD		2.5V clock output synchronous to the CPU clocks. See Table 1, p1.
31, 32, 33, 35, 36, 37, 39, 40, 41	**SDRAM (0:7,_F)**	VDD		3.3V High Speed SDRAM outputs. They are synchronous to CPU.
44, 45	**CPU(0,1)**	VDD		2.5 V Host bus clock outputs. They are powered by VDDCPU.
34, 42	**VDDS**	-		3.3 V Power Supply for SDRAM
46	**VDDCPU**	-		2.5V Power Supply pin for CPU(0:1)
48	**VDDI**	-		2.5V Power Supply pin for IOAPIC
5,9,13,20,26, 30,38, 43	**VSS**	-	-	Common Ground pins.
2,6,16,24,27	**VDD**	-		3.3 V Common Power Supply pins.

Table 2

PU: This denotation refers to an internal pull up of 250kΩ Typical. (applies to signals: S3, S2, S0, SIO, and PD#)
PD: This denotation refers to an internal down up of 250kΩ Typical. (applies to signal: S1)
S4: is an internal signal with a pull-down. It will therefore, default to a '0' after powerup. This signal may only be programmed through I²C, Byte4, Bit1.

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

Power on Bidirectional Pins

Power Up Condition:

Pins 1, 11, 12, 13, and 23 are Power up bi-directional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig 3, below), therefore, they are considered input select pins internal to the IC. After a settling time, the Selection data is latch into internal control registers and these pins become toggling clock outputs.

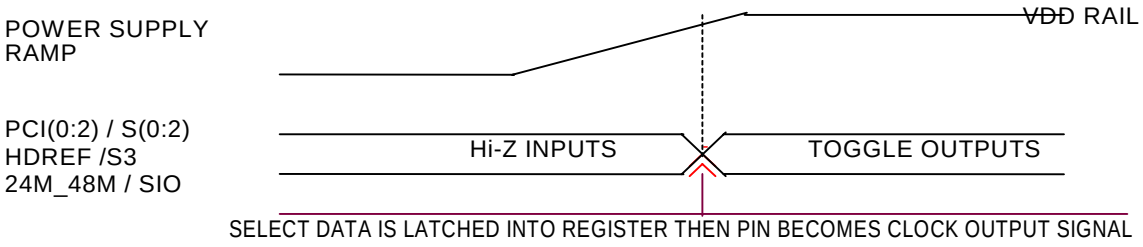


Fig. 3

Strapping Resistor Options:

The power up bidirectional pins have internal pullup (pins 1, 10, 12, 23, 25, 28, and 29) or pulldown (pin 11) resistors connected to them internally. These resistors insure that if these input pins are not connected through an external resistor to Vdd or Vss at power up that they will load the default values into the device's internal resisters. If the Vdd power supply ramps from 0 to Vdd is more than 3 ms at power up, it is recommended that an external 50K resistor be added to this internal device to guarantee that the device will correctly sense these programming selections. In this case, the designer may choose one of two configurations, see Fig. 4A and Fig. 4B.

Fig. 4A represents an additional pull up resistor 10KΩ connected from the pin to the power line, which allows a faster pull to a high level. If a selection "0" is desired, then a jumper is placed on JP1 to a 10KΩ resistor as implemented as shown in Fig.4A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 4B represent a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

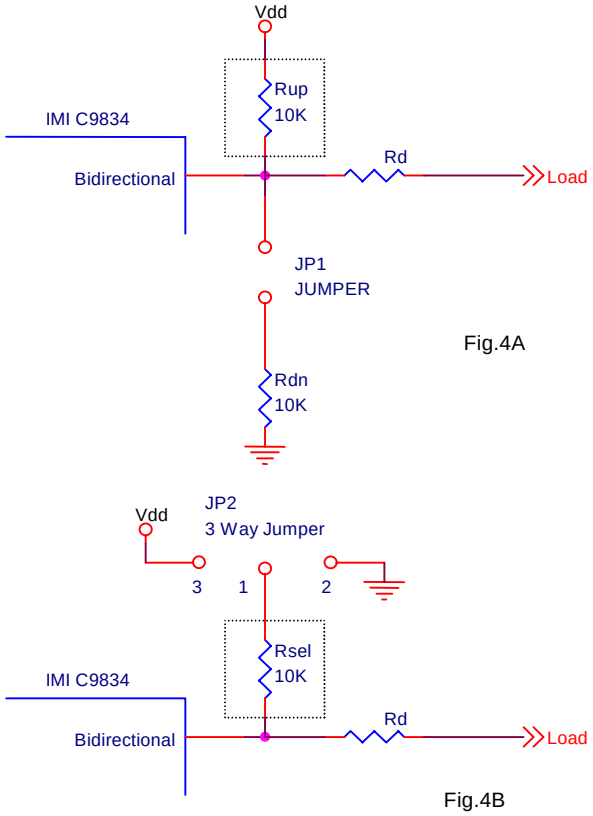


Fig.4A

Fig.4B

Preliminary

Power Management

Power Management on this device is controlled by a single pin, PD# (pin29). When PD# is high (default) the device is in running and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down). When in power down, all outputs are synchronously stopped in a low state (see fig.5 below), all PLL's are shut, and the crystal oscillator is disabled. When the device is shutdown the I^2C function is also disabled.

Power Management Timing

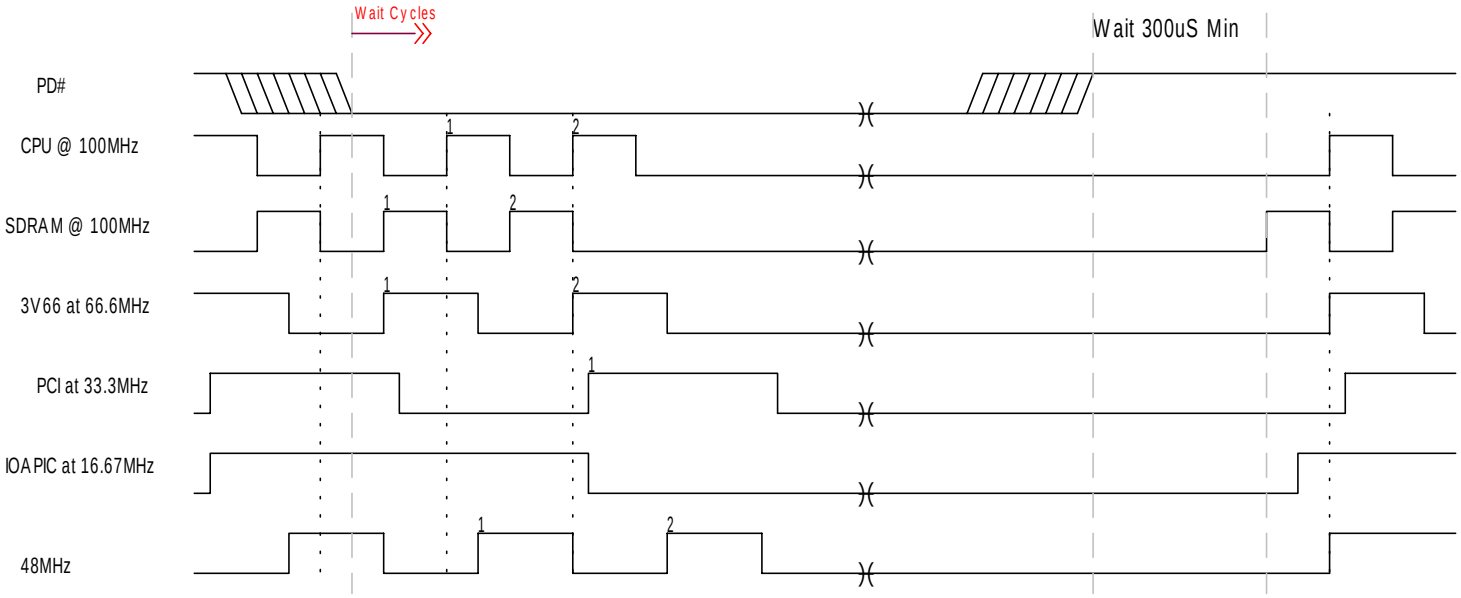


Figure 5

Current Consumption

Signal	Maximum 2.5 Volt Current Consumption (VDD2.5 =2.625)	Maximum 3.3 Volt Current Consumption (VDD3.3 = 3.465 V)
PD# = Logic Low	100µA	1 mA
66.8 MHz (PD# = 1, S3=1, S2=1, S1=0, S0=0)	70 mA	280 mA
100.2 MHz (PD# = 1, S3=1, S2=1, S1=1, S0=0)	100 mA	280 mA

Table 2

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200mS before releasing the PD# pin high.

2-Wire I²C Control Interface

The 2-wire control interface implements a read/write slave only interface according to Philips I²C specification. The device can be read back by using standard I²C command bytes. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode. R/W# = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. If the device should be read then an address **D3** must be sent. Data is transferred MSB first at a max rate of 100kbits/S.
The device will not respond to any other control interface conditions, and previously set control registers are retained.

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte , two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

Byte 0: Peripheral Clock Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Pin Description
7	0	-	BW1, See SST table3, page 8
6	0	-	BW0, See SST table3, page 8
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	1	23	24M_48M
1	1	21, 22	48 MHz
0	0	-	Reserved

Byte 1: SDRAM Clock Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Pin Description
7	1	32	SDRAM7
6	1	33	SDRAM6
5	1	35	SDRAM5
4	1	36	SDRAM4
3	1	37	SDRAM3
2	1	39	SDRAM2
1	1	40	SDRAM1
0	1	41	SDRAM0

Byte 2: PCI Clock Register (1=Enable, 0= Disable)

Bit	@Pup	Pin#	Pin Description
7	1	19	PCI7
6	1	18	PCI6
5	1	17	PCI5
4	1	15	PCI4
3	1	14	PCI3
2	1	12	PCI2
1	1	11	PCI1
0	1	10	PCI0

Byte 3: Control Register (1 = enable, 0 = Disable)

Bit	@Pup	Pin#	Pin Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

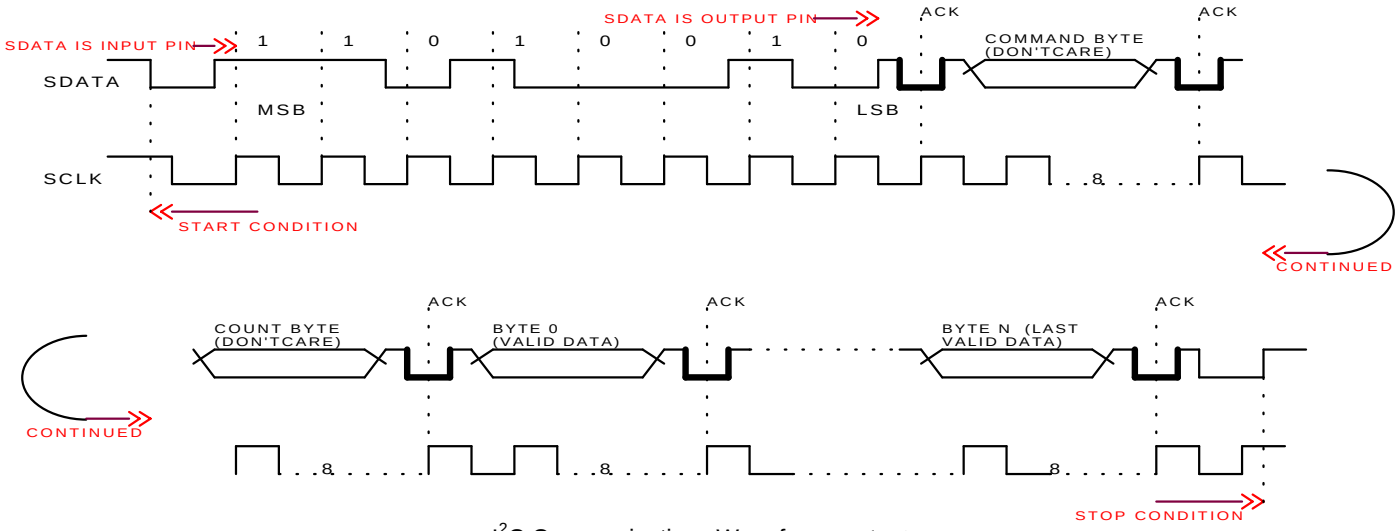
2-Wire I²C Control Interface (Cont.)

Byte 4: Sel Clock Register (1 = select high, 0 = select low)

Bit	@Pup	Pin#	Pin Description
7	0	-	S3
6	0	-	S2
5	0	-	S1
4	0	-	S0
3	0	-	0 = Hardware Frequency Selection from external jumpers, 1= Software Frequency selection from bits1,4,5,6,7
2	0	-	Spread Enable(1)/ disable(0)
1	0	-	S4
0	0	-	Reserved

Byte 5: Control Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Pin Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved



I²C Communications Waveforms. Fig. 6

I²C Test Circuitry

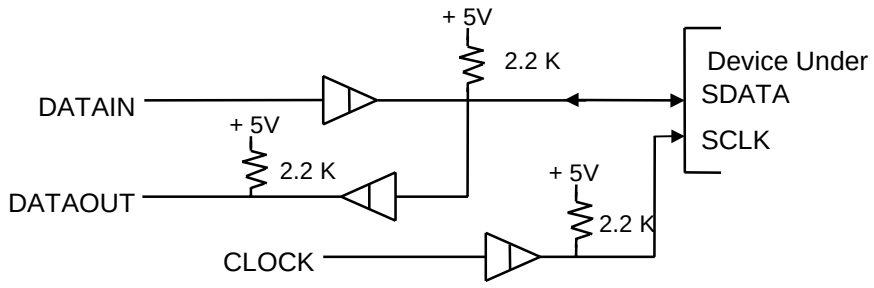


Fig. 7

Note1: Buffer is 7407 with VCC @ 5.0 V

Spectrum Spread Clocking

Spread Spectrum is a modulation technique for reducing Electro Magnetic radiation (EMI) at the source, which in this case is the clock. The concept is based on redistributing the energy of a frequency over a finite bandwidth (also referred to as spread percentage), therefore reducing the measured emission. Fig8A and 8B. present actual measurements on a spectrum analyzer showing the EMI reduction as a result of Spread Spectrum.

Spread Spectrum function is enabled through I²C byte4, Bit 2. At power up, this bit defaults to low (SST Disabled). In order to enable the Spread Spectrum function, Bit 2 in I²C byte 4, should be programmed to a 1.

Up Spread (see table 3 below for selection) is when the modulation is directed up from the resting (non spread) frequency. Fig.8B

This option causes the center frequency to shift up by half the spread percentage: Fcs = Fcr + (Fcr*|p|/2).
Where,

Fcs is the new center frequency
Fcr: is the center frequency of the non spread clocck
|P|: is the absolute value of the Spread Percentage
e.g.: if the non spread spectrum frequency, Fcr, is 100.2MHz and the spread is enabled with a +0.5% spread option, then the new center frequency:
Fcs = 100.2M + (100.2M*0.005/2) = 100.45MHz

Spectrum Spread Clocking (Cont.)

Center Spread (Fig.8A) is when the modulation does not effect the center frequency and the energy is redistributed equally on both sides of the center, which remains the same as the center frequency in the non-spread mode. Therefore, in Center spread, Fcs = Fcr.

Center Spread Spectrum

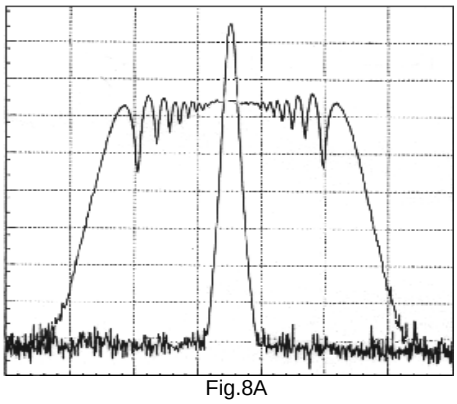


Fig.8A

Up Spread Spectrum

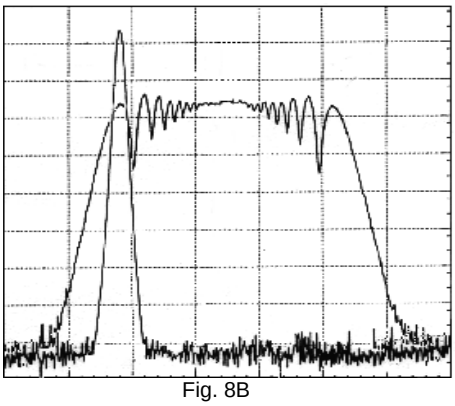


Fig. 8B

Spread Spectrum Selection Table‡

BW1 (Byte0-bit7), BW0 (Byte0-bit6)	Spread%
10	+0.5
11	+/-0.125
01	+/-0. 5
00	+/-0.25, Default

Table 3.

Note‡ In the default spread option, (+/- 0.25), spread spectrum is applicable to all frequencies in Table 1. For other spread options, (+0.5, +/-0.125, and +/-0.5), spread spectrum is applicable to those frequencies at the following selection:

S(4:0) = 01100
S(4:0) = 01101
S(4:0) = 01110
S(4:0) = 01111

Maximum Ratings

Maximum Input Voltage Relative to VSS:	VSS - 0.3V
Maximum Input Voltage Relative to VDD:	VDD + 0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +85ºC
Maximum ESD protection	2000V
Maximum Power Supply:	5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	For internal Pull up / Pull down resistors, Note 3
Input High Current (@VIH = VDD)	IIH			5	µA	
Dynamic Supply Current	Idd3.3V	-	-	280	mA	CPU=100.2MHz, Note 4
Dynamic Supply Current	Idd2.5V	-	-	100	mA	CPU = 100.2MHz, Note 4
Static Supply Current	Isdd	-	-	1	mA	note 4
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin capacitance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	28	30	38	pF	Measured from Pin to Ground. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD = VDDP = 3.3V ±5***%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC***						

Note 1: Applicable to PD# input
Note 2: Applicable to SDATA and SCLK inputs
Note 3: Applicable to S3, S2, S1, S0, SIO, PD#, SDATA, and SCLK inputs. The pull-down resistor has a typical value of 250KΩ, but may vary between 200KΩ to 500KΩ.
Note 4: This measurement is applicable with Spread Spectrum ON or OFF.
Note 5: Although the device will reliably interface with crystals of a 14pF – 20pF C_L range, it is optimized to interface with a typical C_L = 16pF crystal specifications.

Preliminary

AC Parameters

Symbol	Parameter	66.8 MHz Host		100.2 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU(0:1) period (Spread OFF)	14.95	15.5	9.977	10.5	nS	5, 6, 8
THIGH	CPU(0:1) high time	5.2	-	3.0	-	nS	6,10
TLOW	CPU(0:1) low time	5.0	-	2.8	-	nS	6, 11
Tr / Tf	CPU(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	CPU0 to CPU1 Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	CPU(0:1) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	SDRAM(_F, 0:7) period (Spread OFF)	9.977	10.5	9.977	10.5	nS	5, 6, 8
THIGH	SDRAM(_F, 0:7) high time	3.0	-	3.0	-	nS	6,10
TLOW	SDRAM(_F, 0:7) low time	2.8	-	2.8	-	nS	6, 11
Tr / Tf	SDRAM(_F, 0:7) rise and fall times	0.4	1.33	0.4	1.33	nS	6, 7
TSKEW	CPU0 to CPU1 Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	SDRAM(_F, 0:7) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	IOAPIC period (Spread OFF)	59.88	64	59.88	64	nS	5, 6, 8
THIGH	IOAPIC high time	25.3	-	25.3	-	nS	6,10
TLOW	IOAPIC low time	25.3	-	25.3	-	nS	6, 11
Tr / Tf	IOAPIC rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TCCJ	IOAPIC Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	3V66_(0:1) period (Spread OFF)	14.95	15.5	14.95	15.5	nS	5, 6, 8
THIGH	3V66_(0:1) high time	5.2	-	5.2	-	nS	6,10
TLOW	3V66_(0:1) low time	5.0	-	5.0	-	nS	6, 11
Tr / Tf	3V66_(0:1) rise and fall times	0.5	2.0	0.5	2.0	nS	6, 7
TSKEW	3V66_0 to 3V66_1 Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	3V66_(0:1) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	PCI(_F,1:6) period (Spread OFF)	29.94	-	29.94	-	nS	5, 6, 8
THIGH	PCI(_F,1:6) high time	12.0	-	12.0	-	nS	6,10
TLOW	PCI(_F,1:6) low time	12.0	-	12.0	-	nS	6, 11
Tr / Tf	PCI(_F,1:6) rise and fall times	0.5	2.0	0.5	2.0	nS	6, 7
TSKEW	(Any PCI clock) to (Any PCI clock) Skew time	-	500	-	500	pS	6, 8, 9
TCCJ	PCI(_F,1:6) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	48MHz period (conforms to +167ppm max)	20.8299	20.8333	20.8299	20.8333	nS	5, 6, 8
Tr / Tf	48MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	48MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	24MHz period	41.659	41.667	41.659	41.667	nS	5, 6, 8
Tr / Tf	24MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	24MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	REF period	69.8413	71.0	69.8413	71.0	nS	5, 6, 8
Tr / Tf	REF rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	REF Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8
tstable	All clock Stabilization from power-up		3		3	mS	12

VDD = VDDP = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC

Group Limits and Parameter (Applicable to all frequency settings)

Symbol	Parameter	Min	Typ	Max	Units	Notes
TDC	Duty Cycle	45	50	55	%	6, 8, 9
Tskew2	3V66_(0:1) to PCI(0:7) offset, 3V66_(0:1) lead	1.5	-	4.0	nS	6, 8, 9
Tskew3	CPU(0:1) to SDRAM(_F,0:7) offset, CPU lead	0.0	-	250	pS	6, 8, 9, 14, 16, Fig.9
Tskew4	CPU(0:1) to 3V66_(0:1) offset, CPU(0:1) lead	0.0	-	250	pS	6, 8, 9, 14, 15, Fig.9
Tskew5	IOAPIC to PCI(_F,0:1) offset, IOAPIC leads	0.0	-	500	pS	6, 8, 9, Fig.9
VDD = VDDP = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per table 4 below.
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.10)
Note 8: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at 1.25V for 2.5V signals. (see Fig.10)
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Fig. 10)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 13: As this function is available through I²C only, therefore, the time specified is guaranteed by design.
Note 14: These signals are 180 degrees out-of-phase.
Note 15: Applicable when CPU frequency is the same as 3V66 frequency. (namely, 66.8MHz). When CPU = 100.2MHz and 3V66 = 66.8MHz, tSKEW4 is applicable to every **rising** edge of the 3V66 clock and the edge of every 1.5 CPU periods.
Note 16: Applicable when CPU frequency is the same as SDRAM frequency. (namely, 100.2MHz). When CPU = 66.8MHz and SDRAM = 100.2MHz, Tskew3 is applicable to every **falling** edge of the CPU clock and the edge of every 1.5 SDRAM periods.

Loading and Measurement Conditions:

Output name	Max Load (in pF)
CPU(0:1), IOAPIC, HDREF	20
PCI(0:7), SDRAM(_F, 0:7), 3V66(0:1)	30
48 MHz	15

Table 4.

Signal Timing Relationship Diagram

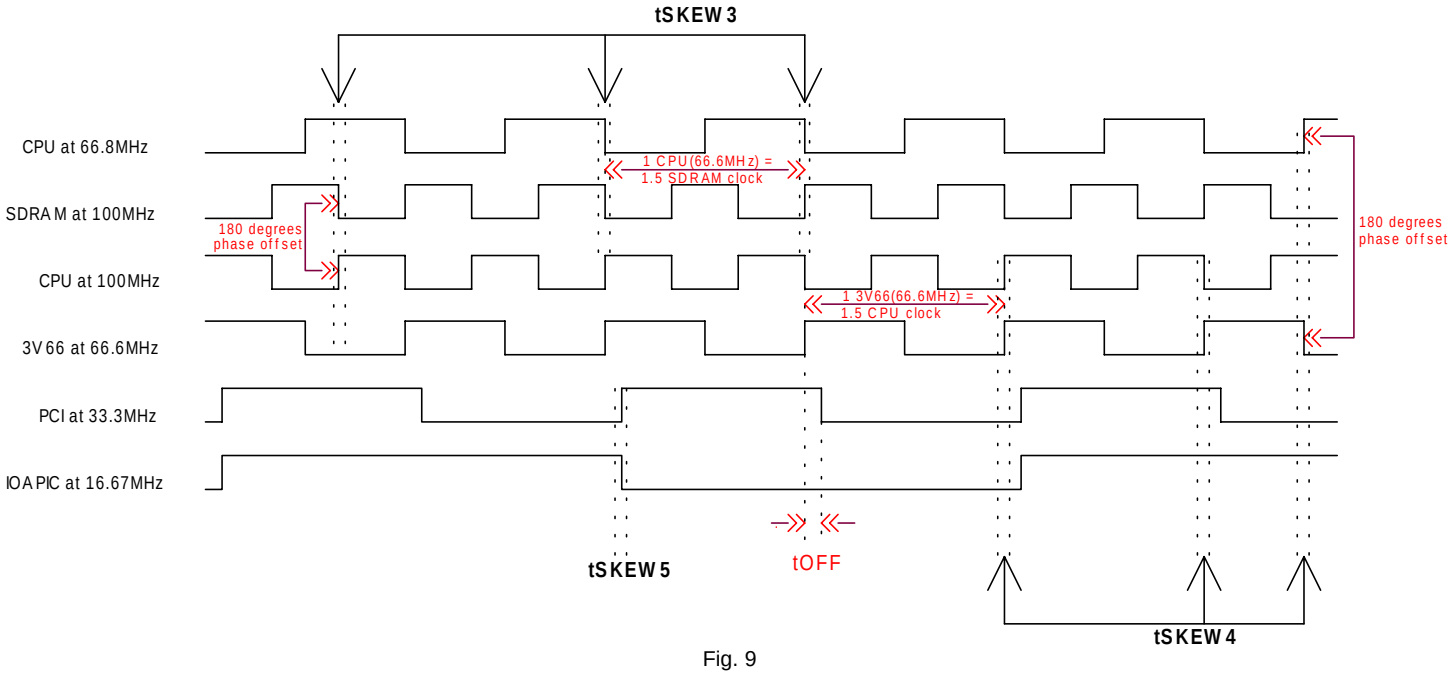
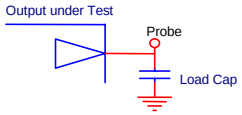
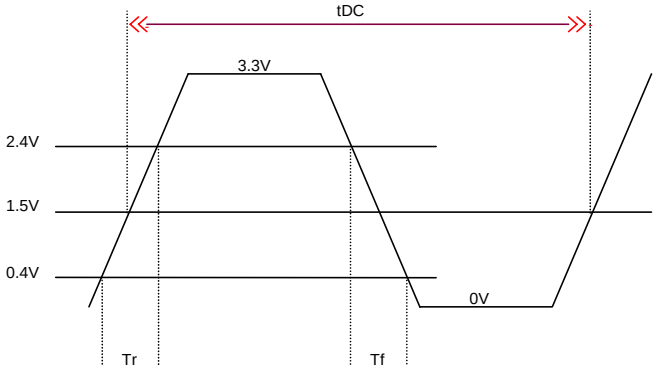


Fig. 9

Measurement Setup



3.3V signals



2.5V signals

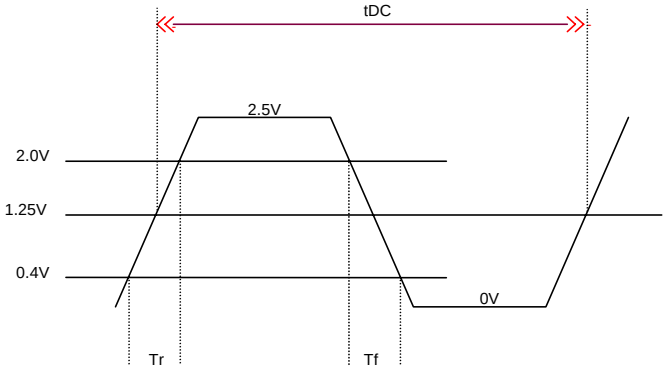


Fig.10

Output Buffer Characteristics

Buffer Characteristics for CPU (0:1), IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-16	-	-	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-32	-	-	mA	Vout = VDDC/2
Pull-Down Current	IOL_1	14	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	34	-	-	mA	Vout = VDDC/2
Dynamic Output Impedance	Z0	13.5		45	Ohm	
Rise/Fall Time Between 0.4 and 2.0 V	Tr / Tf	0.4	-	1.6	nS	See table 5, Page 10

Buffer Characteristics for 24/48 MHz

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-6	-	-	mA	Vout =VDD – 0.5 V
Pull-Up Current	IOH_2	-15	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	6	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	22	-	-	mA	Vout = VDD/2
Dynamic Output Impedance	Z0	20		60	Ohm	
Rise/Fall Time Between 0.4 and 2.4 V	Tr / Tf	0.4	-	4.0	nS	See table 5, Page 10

Buffer Characteristics for SDRAM (0:7, _F), HDREF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-	-	mA	Vout =VDDS – 0.5 V
Pull-Up Current	IOH_2	-56	-	-	mA	Vout = VDDS/2
Pull-Down Current	IOL_1	19	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	63	-	-	mA	Vout = VDDS/2
Dynamic Output Impedance	Z0	10		24	Ohm	
Rise Time MinBetween 0.4 and 2.4 V	Tr	0.4	-	1.33	nS	See table 5, Page 10

Buffer Characteristics for PCI(0:7, F), 3v66_(0:1)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-14	-	-	mA	Vout =VDD – 0.5 V
Pull-Up Current	IOH_2	-35	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	13	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	40	-	-	mA	Vout = VDD/2
Dynamic Output Impedance	Z0	12		55	Ohm	
Rise/Fall Time Between 0.4 and 2.4 V	Tr / Tf	0.4	-	2.0	nS	See table 5, Page 10
VDD = VDDS =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	16	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 30pF
In order to meet the specification for CL = 16pF following the formula:

$$C_L = \frac{C_{XIN} x C_{XOUT}}{C_{XIN} + C_{XOUT}}$$

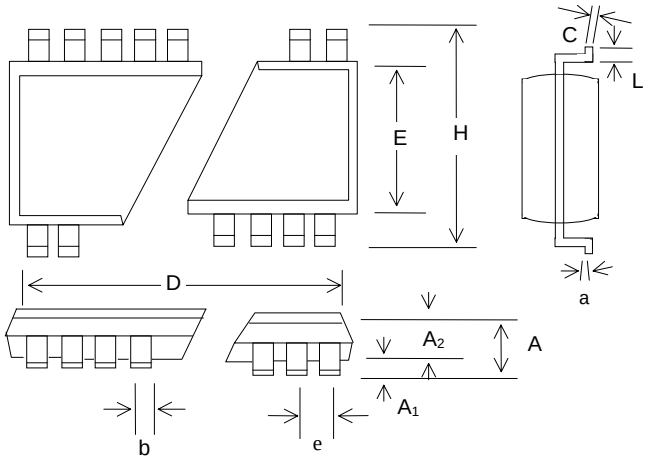
Then the board trace capacitance between Xin and the crystal should be no more than 2pF. (same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 36pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

$$C_L = \frac{32\,pF x 32\,pF}{32\,pF + 32\,pF} = 16\,pF$$

Preliminary

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

Ordering Information

Part Number	Package Type	Production Flow
C9834AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Marking: Example: IMI
C9834
Date Code, Lot #

IMIC9834AYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

IMI Device Number