SignalSphere™ 3G CDMA2000-A Baseband Processor: CBP4.0

OVERVIEW

LSI Logic's SignalSphere™ chip is a highly integrated CDMA Baseband Processor for wireless handsets and data applications. The CBP4.0 has all of the baseband processing logic required to support CDMA2000 Cellular, PCS and AMPS, and is backward compatible to IS-95B. Utilizing the company's leading-edge G12® CMOS process technology, which features 0.13-micron (Leff) gate length devices, the CBP4.0 offers high performance and functionality in a smaller footprint, supported by advanced packaging capabilities. Wireless-product manufacturers can leverage these benefits to reduce overall product size and power consumption while increasing reliability.

The SignalSphere processor integrates voice coding—including mixed-signal analog and digital capabilities–with a seamless interface to speakers, microphones, memory and IF/RF devices. The specific CDMA blocks include:

- Two standard CDMA vocoders (EVRC and QCELP13)
- AMPS capability
- Receive filter
- Transmit filter
- Receive analog-to-digital converter (ADC)
- Transmit digital-to-analog converter (DAC)
- Receive and transmit modems
- Phase-locked loops (PLL)
- Auxiliary DACs and ADCs
- Voice codec
- Real time clock (RTC)

The CBP4.0 also includes an on-chip ARM7TDMI™ control processor with on-chip RAM, two OakDSPCore® digital signal processors (DSPs), DSP programmable RAM/ROM, data RAM, accelerators, glue logic, and digital logic for most modem functions.

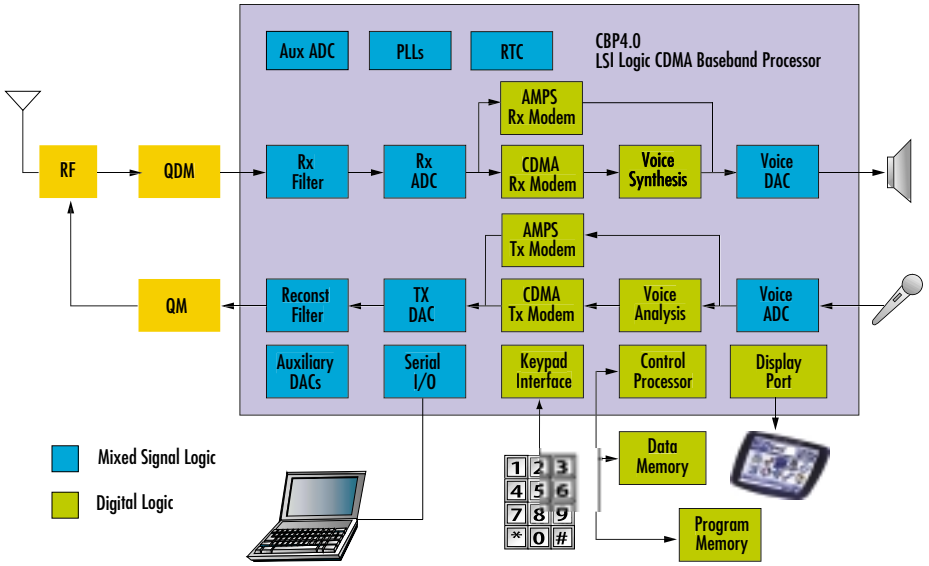

Figure 1. Simplified Block Diagram - SignalSphere™ CDMA Baseband Processor: CBP4.0

FEATURES

- An ARM7TDMI™ control processor (CP). The CP performs all control functions, including protocol stack, user interface, and hardware interface
- Two OakDSPCore® digital signal processors. One DSP assists the modem hardware. The other performs vocoder operations for QCELP-13 and EVRC
- Mixed-signal logic for the Rx analog-to-digital (ADC), Rx Filter, Tx Filter, Tx digital-to-analog (DAC), PLL, voice codec, and auxiliary DAC and ADC functions
- Special purpose logic providing signal processing, modulation, demodulation, hardware accelerators, and interfaces for keypad and display

BENEFITS

- Power: Ultra-low chip quiescent current for increased standby time in both QPCH and PCH modes
- Slotted-Paging Implementation: Increases standby time over conventional implementations
- Small Size: The CBP at 16mm x 16mm with 0.8mm pitch, featuring LSI Logic's 280-pin Chip Scale Package (CSP) mounting technology, is unmatched in its size-to-performance ratio
- Cost: Single-chip integration of both digital and mixed-signal functions greatly reduces manufacturing and material costs, optimizing end-product value
- Performance: The CBP4.0 meets CDMA2000-A requirements including support for 153Kbps data rate
- Time-to-Market: LSI Logic's software and chips undergo comprehensive system and chip validation in multiple environments, and are backed by unmatched support
- Backward Compatibility: The CBP4.0 is backward compatible to IS-95B and LSI Logic's CBP3.0

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3G CDMA2000-A Baseband Processor

Figure 2. Applications of the future on today's CBP platform.

FLEXIBILITY

As with so many other SoC applications in the communications and networking arena, LSI Logic's unique CoreWare® design methodology and library of building blocks provides system designers with unsurpassed flexibility. Wireless-device manufacturers can take advantage of CoreWare technology to add value and specific features to the single CDMA chip for dramatic product differentiation–all while accelerating time to market by shortening the product development cycle and paving a smooth technology migration path into the future. Value-added functionality can be achieved with voice recognition options and a customized MMI (man/machine interface).

INTEGRATION AND POWER

The single-chip integration helps reduce power consumption because the signals pass between the on-chip functions blocks rather than between multiple chips at the I/O drive level. Additionally, the single-chip's digital circuitry operates at only 1.8 volts, significantly reducing power consumption. Working in conjunction with on-chip 3.0 volt mixed-signal circuitry (which includes a phase-locked loop, voice codec, receive and transmit paths, and auxiliary ADC and DAC units), the chip's digital 1.8 volt operation and sophisticated power-saving capabilities pave the way for increased battery life.

DEVELOPMENT TOOLS

The CBP4.0 comes with powerful development tools, including development/integration systems, reference designs, ETS (Engineering Test Software) and GAT (Graphical Analysis Tool). The ETS package provides low-level data access for system integration and phone calibration capability for production-test functionality. The GAT software package works with ETS to provide graphical view of the essential data during development and field-testing.

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