CBP3.0 CDMA Baseband Processor

World's First Single Chip CDMA Baseband Processor

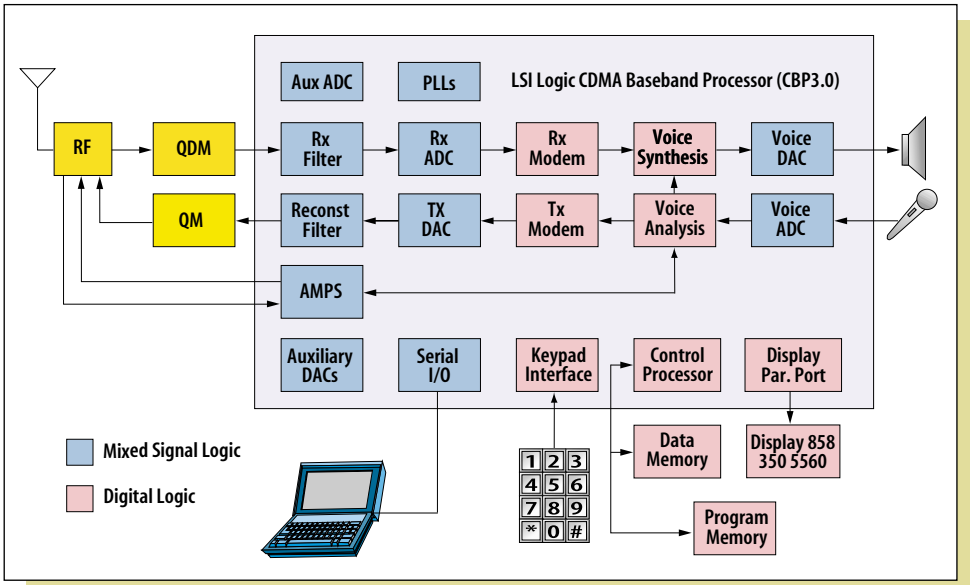
Overview

The LSI Logic CBP3.0 chip is the most highly-integrated CDMA processing solution available today for wireless handset designers. Thanks in large part to the company's leading-edge G11™ CMOS process technology, which features 0.18-micron (Leff) gate length devices, system designers can pack more performance and functionality into an ever-smaller footprint, supported by leading-edge packaging capabilities. Phone manufacturers can use this integration to reduce overall product size and power consumption while increasing reliability.

The CBP3.0 integrates voice coding–including mixed-signal analog and digital capabilities–with a seamless interface to baseband modem, speaker, microphone and IF/RF devices. The specific CDMA blocks include:

- Two standard CDMA vocoders (EVRC and QCELP13)
- AMPS capability
- Receive filter
- Transmit filter
- Receive analog-to-digital converter (ADC)
- Transmit digital-to-analog converter (DAC)
- Receive and transmit modems,
- Phase-locked loops (PLL)
- Auxiliary DACs
- Voice codec

The chip also includes an on-chip ARM7TDMI™ control processor with on-chip RAM, two OakDSPCore® digital signal processors (DSPs), DSP program RAM/ROM, data RAM, digital logic for most modem functions, accelerators and glue logic.



Simplified Block Diagram - CDMA Baseband Processor

Features

- An ARM7TDMI™ control processor (CP). The CP performs all control functions, including protocol stack, user interface, and hardware interface
- Two OakDSPCore® Digital Signal Processors. One DSP assists the modem hardware. The other performs vocoder operations for QCELP-13 and EVRC
- Mixed signal logic for the Rx ADC, Rx Filter, Tx Filter, Tx DAC, PLL, voice codec, and auxiliary digital-to-analog (DAC) and analog-to-digital (ADC) functions
- Special purpose logic providing signal processing, modulation, demodulation, hardware accelerators, and interfaces for keypad and display

Benefits

- Low power consumption: Unique design consumes less than 1mW during paging and standby modes
- Slotted-Paging Implementation: Increases standby over conventional implementations
- Small size: The CBP at 16mm x 16mm with 0.8mm pitch, featuring LSI Logic's 280-pin Chip Scale Package (CSP) mounting technology is unmatched in its size-to-performance ratio
- Cost: Single chip integration of both digital and mixed signal functions greatly reduces manufacturing and material costs, optimizing end-product value
- Performance: The CDMA Baseband Processor meets IS-95B requirements including support for 64Kbps data rate on the forward link
- Time to Market: The CBP's powerful combination of the ARM7TDMI processor and dual OakDSPCore® DSPs implementing IS-95B functions lets product designers focus on production issues rather than CDMA integration

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Expanding the Feature Set, Reducing Costs and Power Consumption

As with so many other SoC applications in the communications and networking arena, LSI Logic's unique CoreWare® design methodology and library of building blocks provides system designers with unsurpassed flexibility. CDMA cellular and PCS vendors can take advantage of CoreWare technology to add value and specific features to the single CDMA chip for dramatic product differentiation–all while accelerating time to market by shortening the product development cycle and paving a smooth technology migration path into the future. Potential value-added functionality may include a customized display interface; a DSP dedicated to voice processing that can be used for voice recognition purposes; and support for various Flash/RAM types, sizes, and speeds.

The single-chip integration helps reduce power consumption because the signals pass between the on-chip functions blocks rather than between multiple chips at the I/O drive level. Additionally, the single chip's digital circuitry operates at only 1.8 volts, significantly reducing power consumption. Working in conjunction with on-chip 3.3-volt mixed-signal circuitry (which includes a phase-locked loop, voice codec, receive and transmit paths, and auxiliary ADC and DAC units), the chip's digital 1.8-volt operation and sophisticated power-saving capabilities pave the way for battery life increase.

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