GENERAL DESCRIPTION

The BW1251X is a CMOS 3.3V 12-bit analog-to- digital converter (ADC). It converts the analog input signal into 12-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5MHz clock.

The device is a recycling type monolithic ADC with an on-chip sample-and-hold function. The ADC has power down mode.

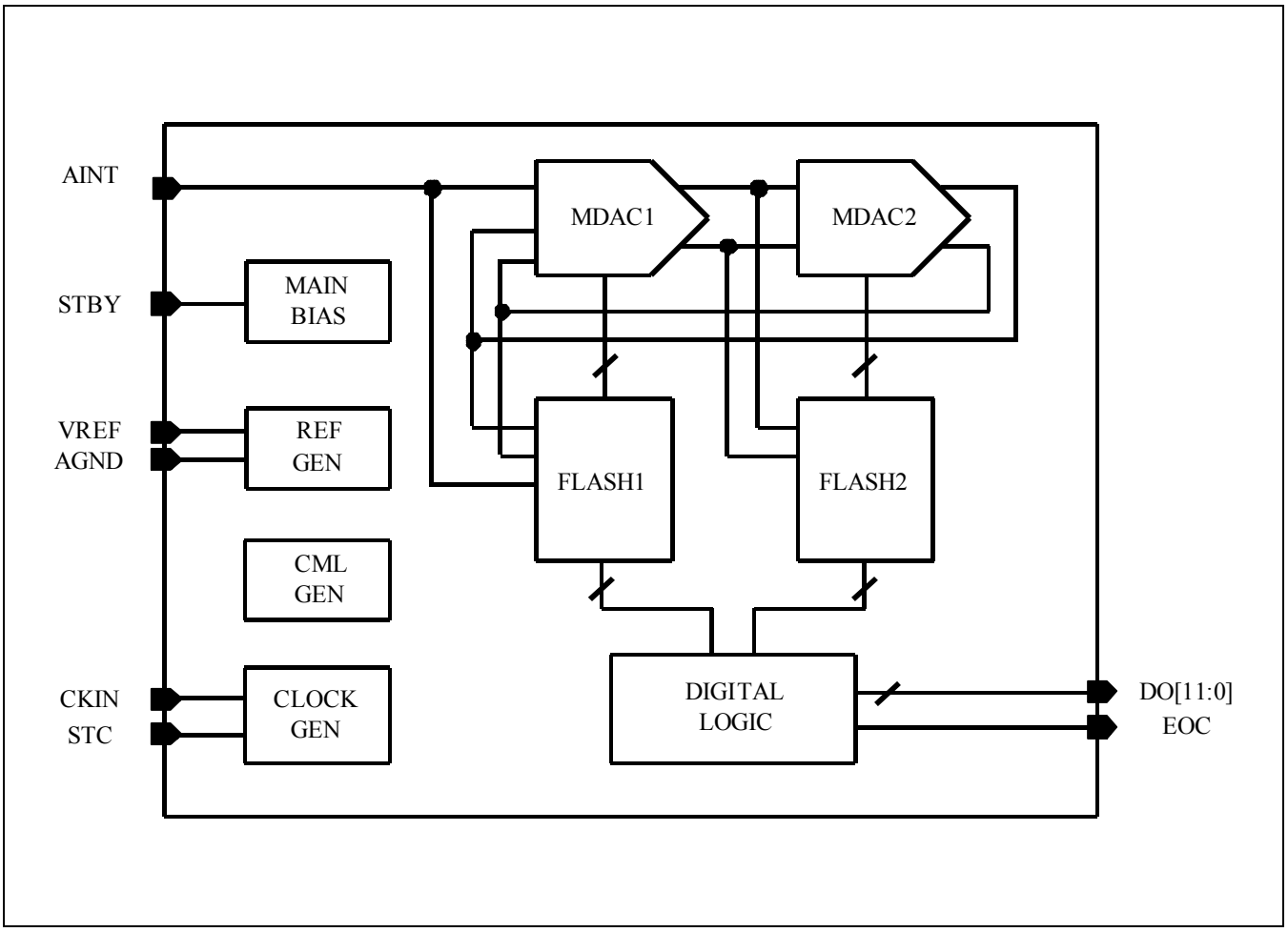
TYPICAL APPLICATIONS

— MICOM Interface
— Portable Equipment
— Low-Voltage Low-Power Application

FEATURES

— Resolution: 12-bit
— Maximum Conversion Rate : 500KSPS
— Main Clock: 2.5MHz
— Power Supply: 3.3V ±0.3V
— Total Current: 20uA (Standby Mode)
2.2mA (Normal Operation)
— Input Range: 0.0V ~ 3.3V ($3.3V_{P-P}$)
— Differential Linearity Error: ±0.7 LSB
— Integral Linearity Error: ±0.8 LSB
— Signal to Noise & Distortion Ratio: 70dB
— Digital Output: CMOS Level
— Operating Temperature Range: 0 °C ~ 70 °C

FUNCTIONAL BLOCK DIAGRAM



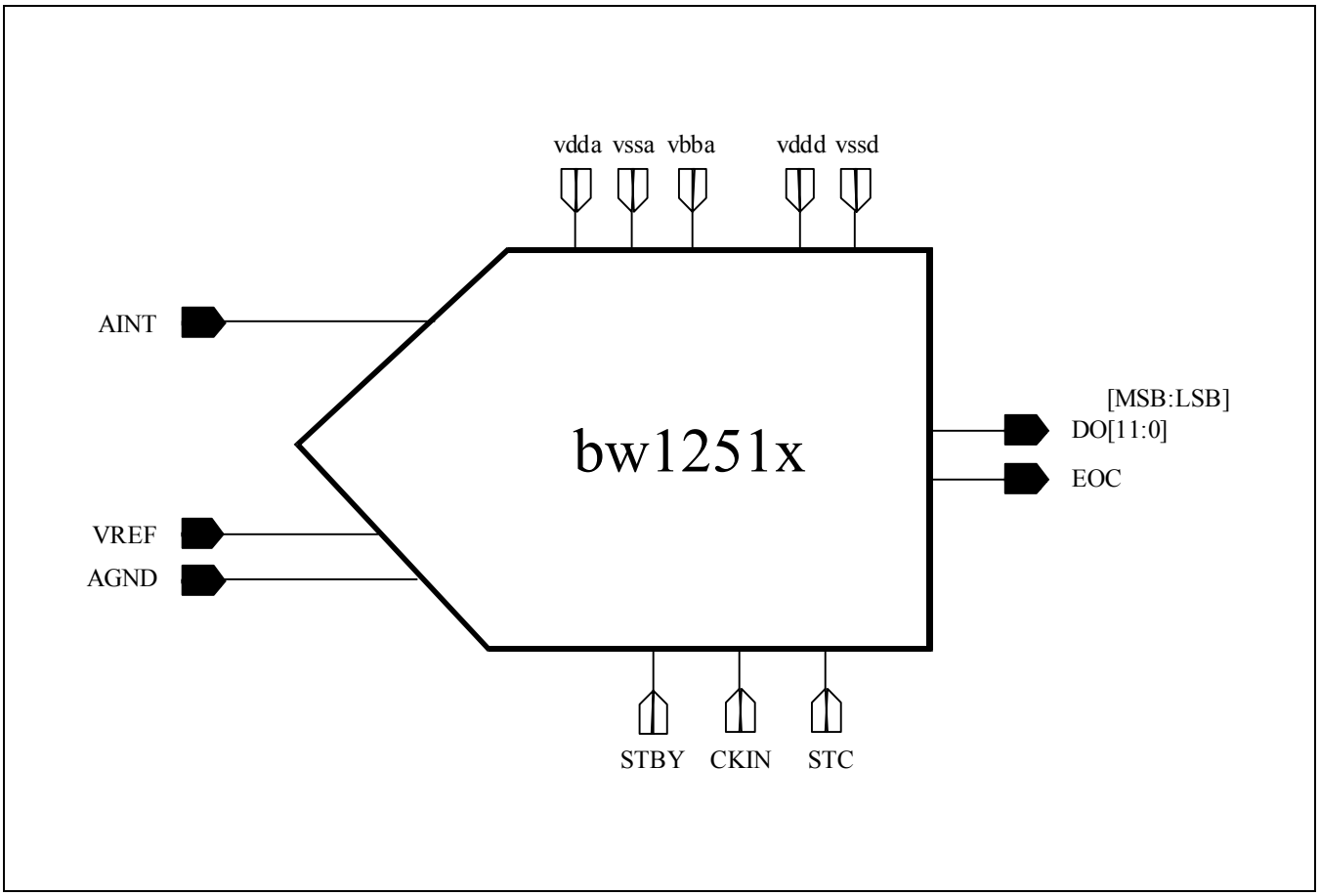
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VREF	AI	pia_bb	Reference Top (3.3V)
AGND	AI	pia_bb	Reference Bottom (0.0V)
VDDA	AP	vdda	Analog Power (3.3V)
VBBA	AG	vbba	Analog Sub Bias (0.0V)
VSSA	AG	vssa	Analog Ground (0.0V)
AINT	AI	piar50_bb	Analog Input (Input Range: 0.0V ~ 3.3V)
STBY	DI	picc_bb	VDD = power saving (standby), GND = normal
CKIN	DI	picc_bb	Sampling Clock Input
D[11:0]	DO	pot4_bb	Digital Output
EOC	DO	pot4_bb	End of Conversion Signal
STC	DI	picc_bb	Start of Conversion Signal
VSSD	DG	vssd	Digital GND (0.0V)
VDDD	DP	vddd	Digital Power (3.3V)

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground
— AB: Analog Bidirectional
— DB: Digital Bidirectional

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	4.5	V
Analog Input Voltage	AINT	VSS to VDD	V
Digital Input Voltage	CKIN	VSS to VDD	V
Reference Voltage	VREF / AGND	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTE:

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDD VDDA	3.0	3.3	3.6	V
Reference Input Voltage	VREF AGND	2.0 0.0	3.3 0.0	3.6 0.0	V
Analog Input Voltage	AINT	0.0	VREF	-	V
Operating Temperature	Toper	0	-	70	°C

NOTE: It is strongly recommended that all the supply pins (VDDA, VDDD) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Differential Nonlinearity	DNL	–	0.7	±1	LSB	VREF=3.3V AGND=0.0V
Integral Nonlinearity	INL	–	0.8	±2	LSB	VREF=3.3V AGND=0.0V
Offset Voltage	OFF	–	10	16	LSB	VREF=3.3V AGND=0.0V

NOTE: Converter Specifications : VDDA=VDDD=3.3V, VSSA=VSSD=0V, Toper=25 °C, VREF=3.3V, AGND=0.0V unless otherwise specified

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Maximum Conversion Rate	fc	–	–	500	KSPS	f_{CKIN} = 2.5MHz
Standby Supply Current		–	20	40	uA	STBY = VDD
Dynamic Supply Current	IVDD	–	1.8	2.4	mA	f_{CKIN} = 2.5MHz (without system load)
Reference Current	IREF	–	0.4	0.6	mA	V_{REF} = 3.3V
Total Harmonic Distortion	THD	–	-82	-68	dB	f_{CKIN} = 2.5MHz AINT=100kHz
Signal-to-Noise & Distortion Ratio	SNDR	60	70	–	dB	f_{CKIN} = 2.5MHz AINT=100kHz

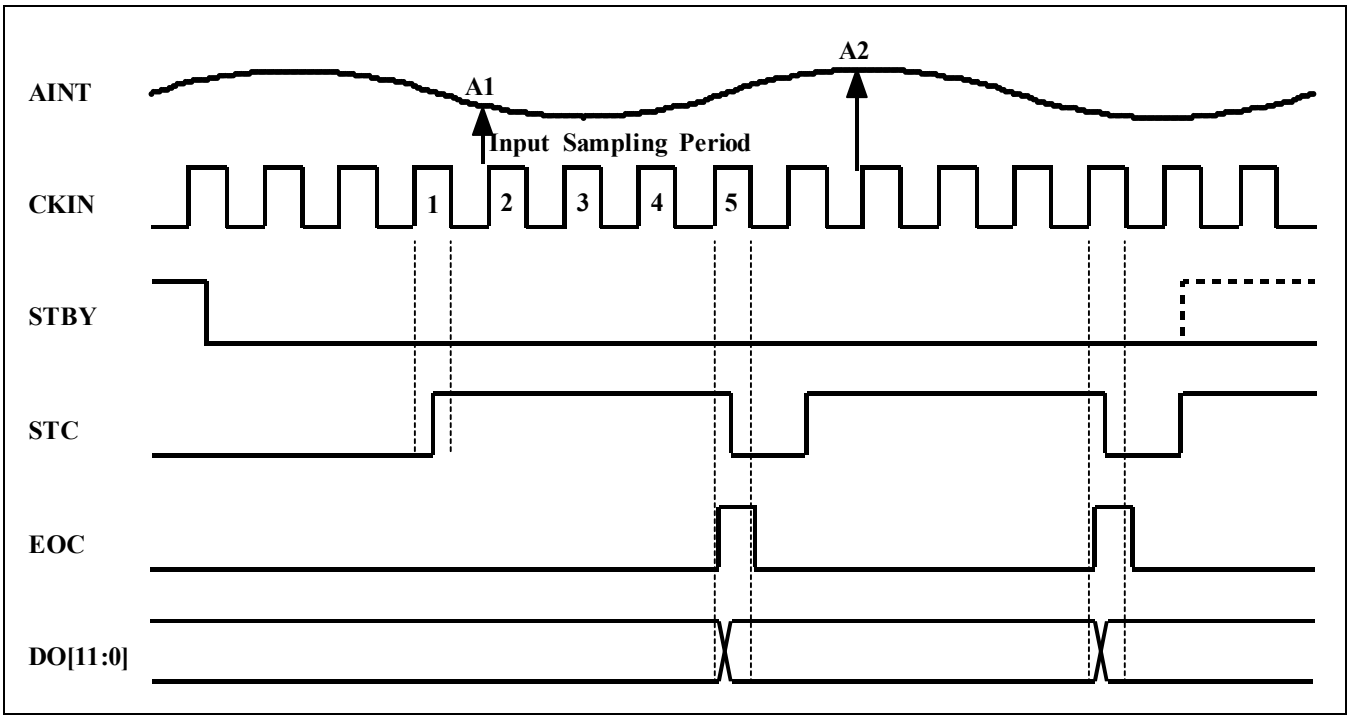
NOTE: Converter Specifications : VDDA=VDDD=3.3V, VSSA=VSSD=0V, Toper=25 °C, VREF=3.3V, AGND=0.0V unless otherwise specified

I/O CHART

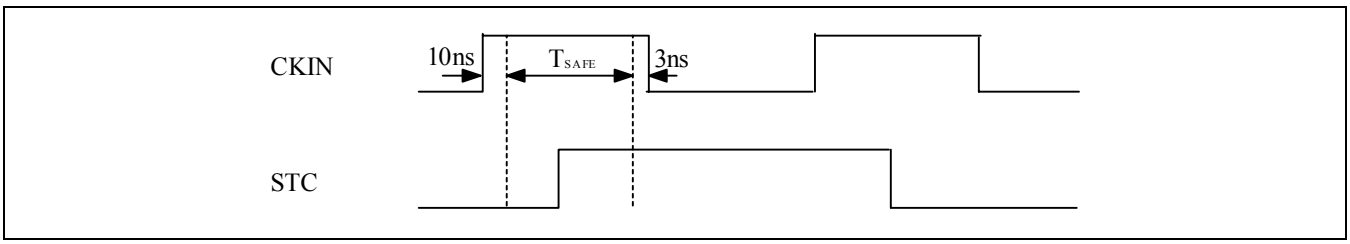
Index	AINT Input (V)	Digital Output	
0	~ 0.00081	0000 0000 0000	1LSB=0.806mV
1	0.00081 ~ 0.00161	0000 0000 0001	VREF=3.3V
2	0.00161 ~ 0.00242	0000 0000 0010	AGND=0.0V
~	~	~	
2047	1.64919 ~ 1.65000	0111 1111 1111	
2048	1.65000 ~ 1.65081	1000 0000 0000	
2049	1.65081 ~ 1.65161	1000 0000 0001	
~	~	~	
4093	3.29758 ~ 3.29839	1111 1111 1101	
4094	3.29839 ~ 3.29919	1111 1111 1110	
4095	3.29919 ~	1111 1111 1111	

TIMING DIAGRAM

1. Main Waveform



2. STC & CKIN CONDITION



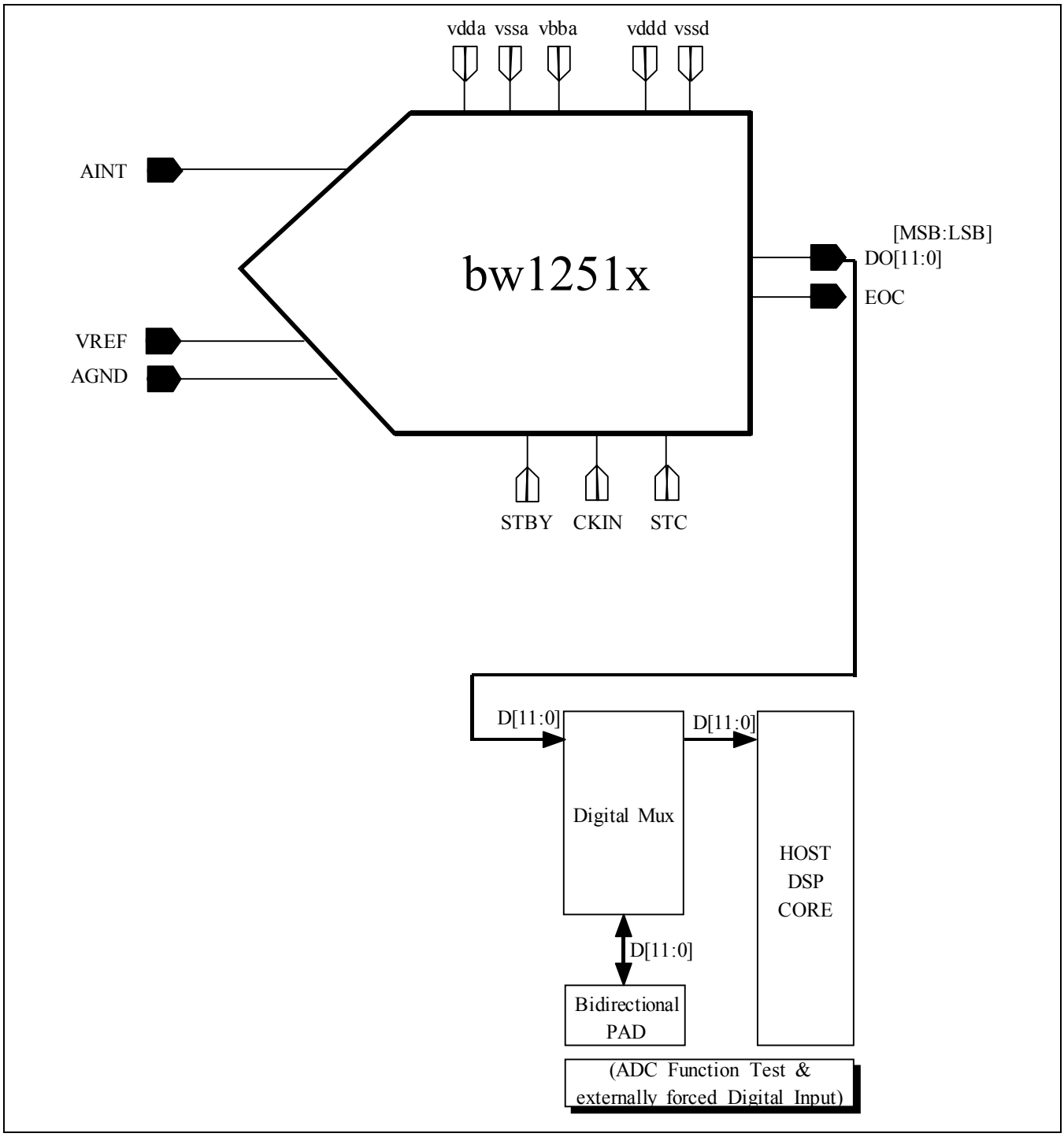
The A/D Converter operates data conversion when STC (Start Conversion) signal is just "HIGH". Otherwise, output data (DO[11:0]) keep the current states. The STC signal should be changed during "T_{SAFE}" with the "HIGH" level of the clock to operation as shown in the main waveform.

ADC External Interface Signal

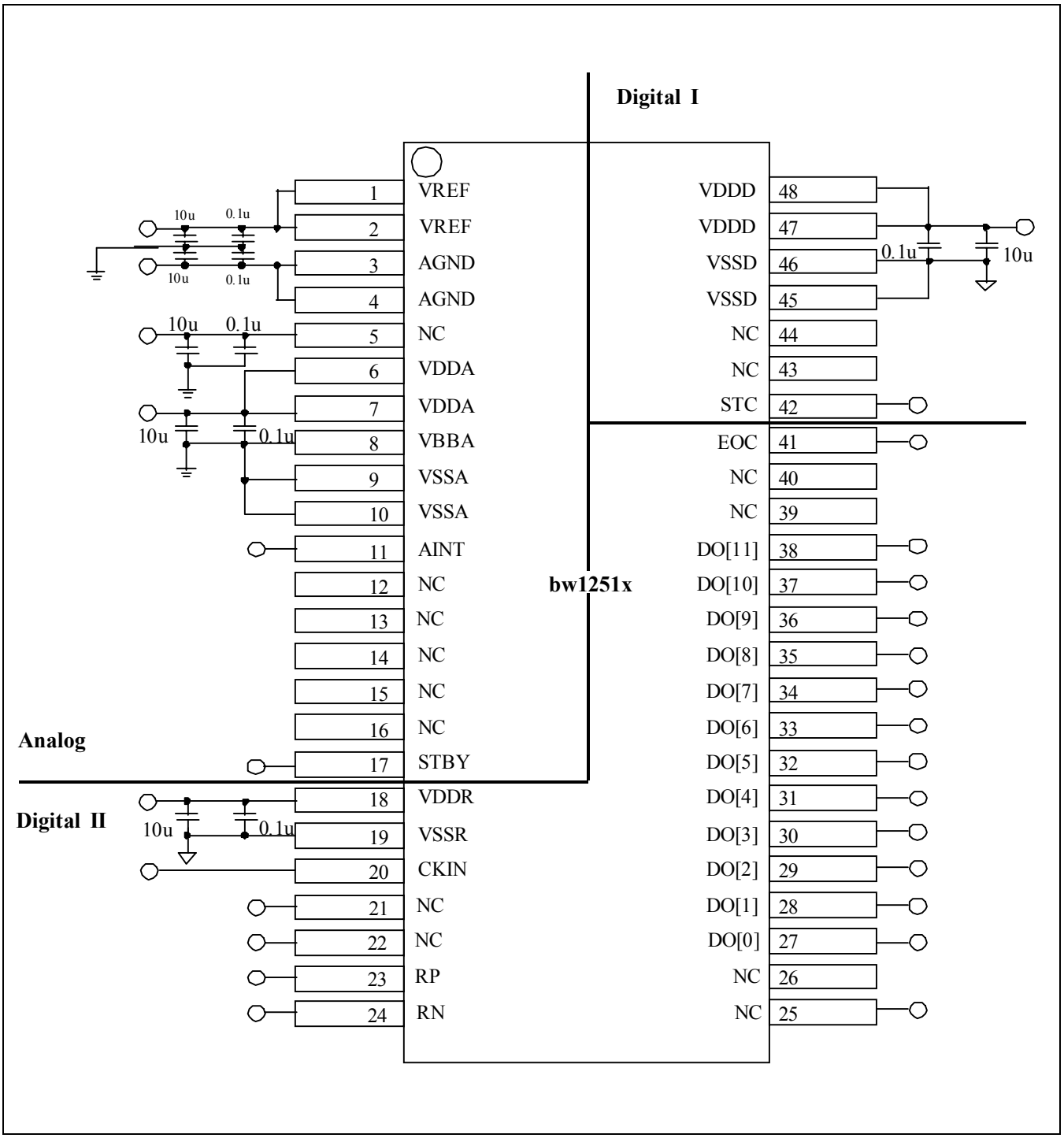
- AINT: Analog Input Signal (Input)
  Input Range : VREF ~ AGND
- STBY: Stand-by Signal, Power Save Mode (Input)
- CKIN: ADC Main Clock, fCKIN = 2.5MHz, 1 Clock Period = 400ns (Input)
- STC: Start of Conversion Signal (Input)
- EOC: End of Conversion Signal (Output)
- DO[11:0]: Digital Output Signal (Output)

CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased internally through resistor divider.



PACKAGE CONFIGURATION



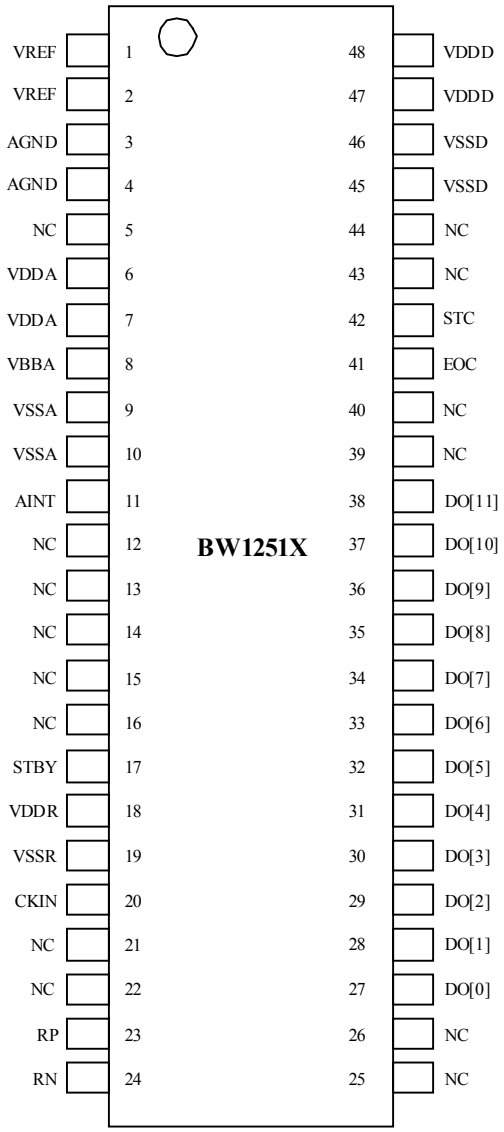
NOTE: NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

Pin No.	Name	I/O Type	Pin Description
1,2	VREF	AI	Reference Voltage (3.3V)
3,4	AGND	AI	Analog Ground (0.0V)
6, 7	VDDA	AP	Analog Power (3.3V)
8	VBBA	AG	Analog Sub Bias
9, 10	VSSA	AG	Analog Ground
11	AINT	AI	Analog Input
17	STBY	DI	VDD=Power saving (Standby), GND=Normal
18	VDDR	PP	PAD Power (3.3V)
19	VSSR	PG	PAD Ground
20	CKIN	DI	Clock Input (f_{CKIN} = 2.5MHz)
23	RP	AO	Test Pin1
24	RN	AO	Test Pin2
27	DO[0]	DO	Digital Output (LSB)
28~37	DO[1:10]	DO	Digital Output
38	DO[11]	DO	Digital Output (MSB)
41	EOC	DO	End of Conversion Signal
42	STC	DI	Start of Conversion Signal
45, 46	VSSD	DG	Digital GND
47, 48	VDDD	DP	Digital Power (3.3V)

PACKAGE PIN DESCRIPTION (Continued)

Configuration



SAMSUNG ELECTRONICS

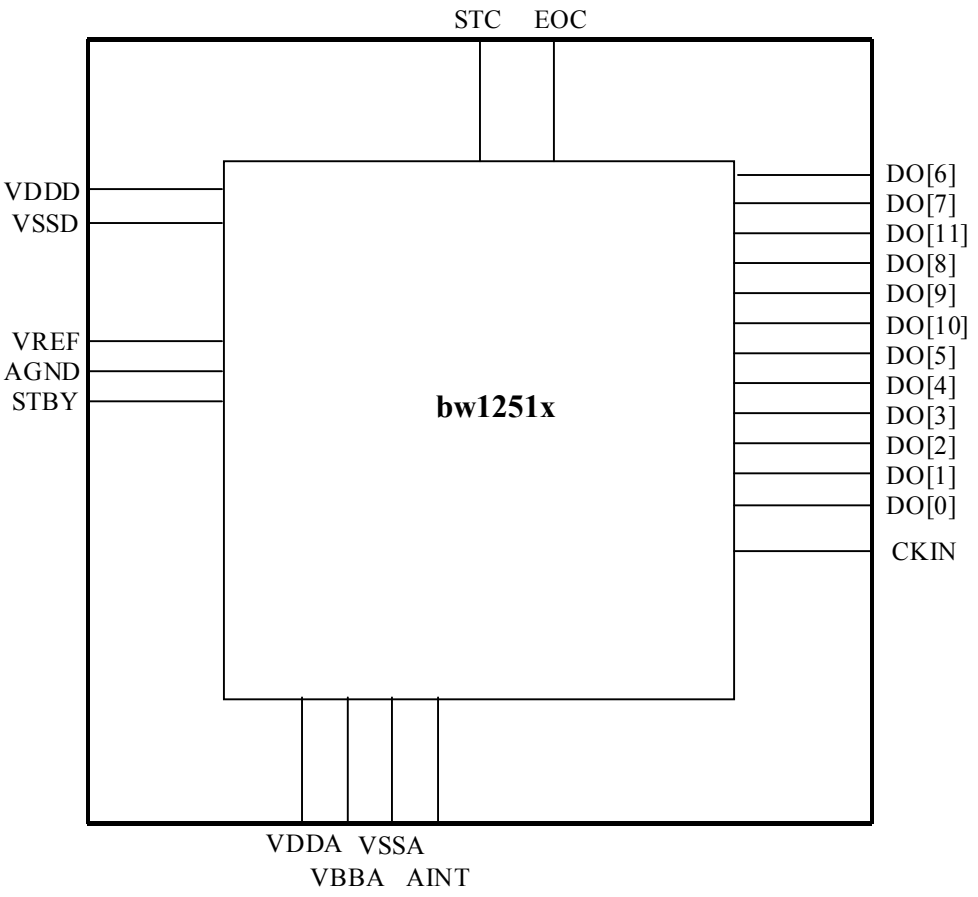
USER GUIDE

1. Input Range

— The analog input is single-ended type and the range is from VREF to AGND. This AINT voltage follows reference voltage range fundamentally. So, if you want to alter into the another input range, you should change the voltage value of VREF.

— You can use the AINT voltage whose minimum range is 2.0V. In this case, the VREF is 2.0V.

PHANTOM CELL INFORMATION



PHANTOM CELL INFORMATION (Continued)

Name	I/O Type	Pin Usage	Pin Description
AINT	AI	Internal/External	AINT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
STBY	DI	Internal/External	
CKIN	DI	Internal/External	
D[11:0]	DO	Internal/External	
EOC	DO	Internal/External	
STC	DI	Internal/External	
VREF	AI	External	Voltage reference lines (VREF and AGND) must be wide metal to reduce voltage drop of metal lines.
AGND	AI	External	
VDDA	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
VBBA	AG	External	
VSSA	AG	External	
VSSD	DG	External	
VDDD	DP	External	

FEEDBACK REQUEST

ADC SPECIFICATION

Parameter	Min	Typ	Max	Unit	Remarks
Supply voltage				V	
Reference Input voltage				V	
Analog Input voltage				Vpp	
Operating temperature				°C	
Integral non-linearity error				LSB	
Differential non-linearity error				LSB	
Offset voltage error (Bottom)				mV	
Offset voltage error (Top)				mV	
Maximum conversion rate				MSPS	
Dynamic supply current				mA	
Power dissipation				mW	
Signal-to-noise ratio				dB	
Digital output format (Provide detailed description & timing diagram)					

- What do you want to choose as power supply voltages? For example, the analog VDD needs to be 5V. the digital VDD can be 3.3V/5V.
- What resolution do you need for ADC?
- How about conversion speed (data in ® data out)?
- How many cycles do exist during the latency of ADC (pipelined delay)?
- What's the input range? And then what do you need between single input and differential input?
- Can the bus interface be compatible with TTL?
- Could you explain external/internal pin configurations as required?

Specially requested function list :

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0		Original version published (preliminary)	
ver 1.1	1999.06	Release the formal datasheet	
ver 1.2	02.04.29	Add the pin information to the phantom cell information	