GENERAL DESCRIPTION

The BW1238X is a CMOS 6-Bit A/D converter for a digital video disk (DVD) partial-response maximum likelihood (PRML) system. It is a flash type A/D converter which consists of input buffer, comparator array, digital backend encoder, and output buffer. The maximum conversion rate of BW1238X is over 250MSPS and supply voltage is 3.3V single.

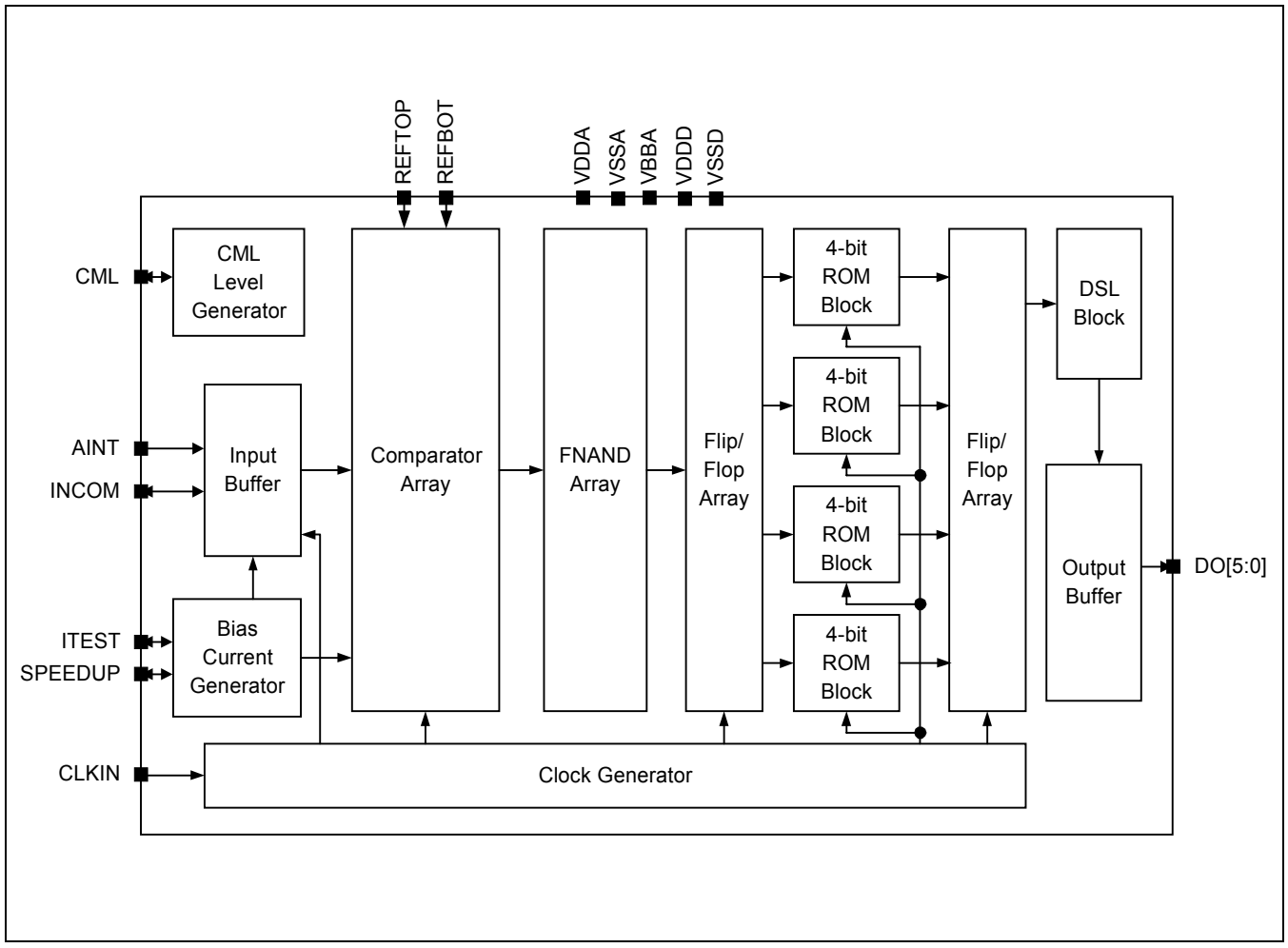
TYPICAL APPLICATIONS

— Multi-media applications
— Digital video disk (DVD) system
— Digital broadcast satellite (DBS) receiver
— Quadrature phase shift keying (QPSK) demodulator
— Video applications

FEATURES

— Resolution : 6Bit
— Differential Linearity Error : ±1.0 LSB
— Integral Linearity Error : ±1.0 LSB
— Maximum Conversion Rate : 250MSPS
— Digital Output : CMOS Level
— Power Consumption : 260mW
— Power Supply : 3.3V Single

FUNCTIONAL BLOCK DIAGRAM



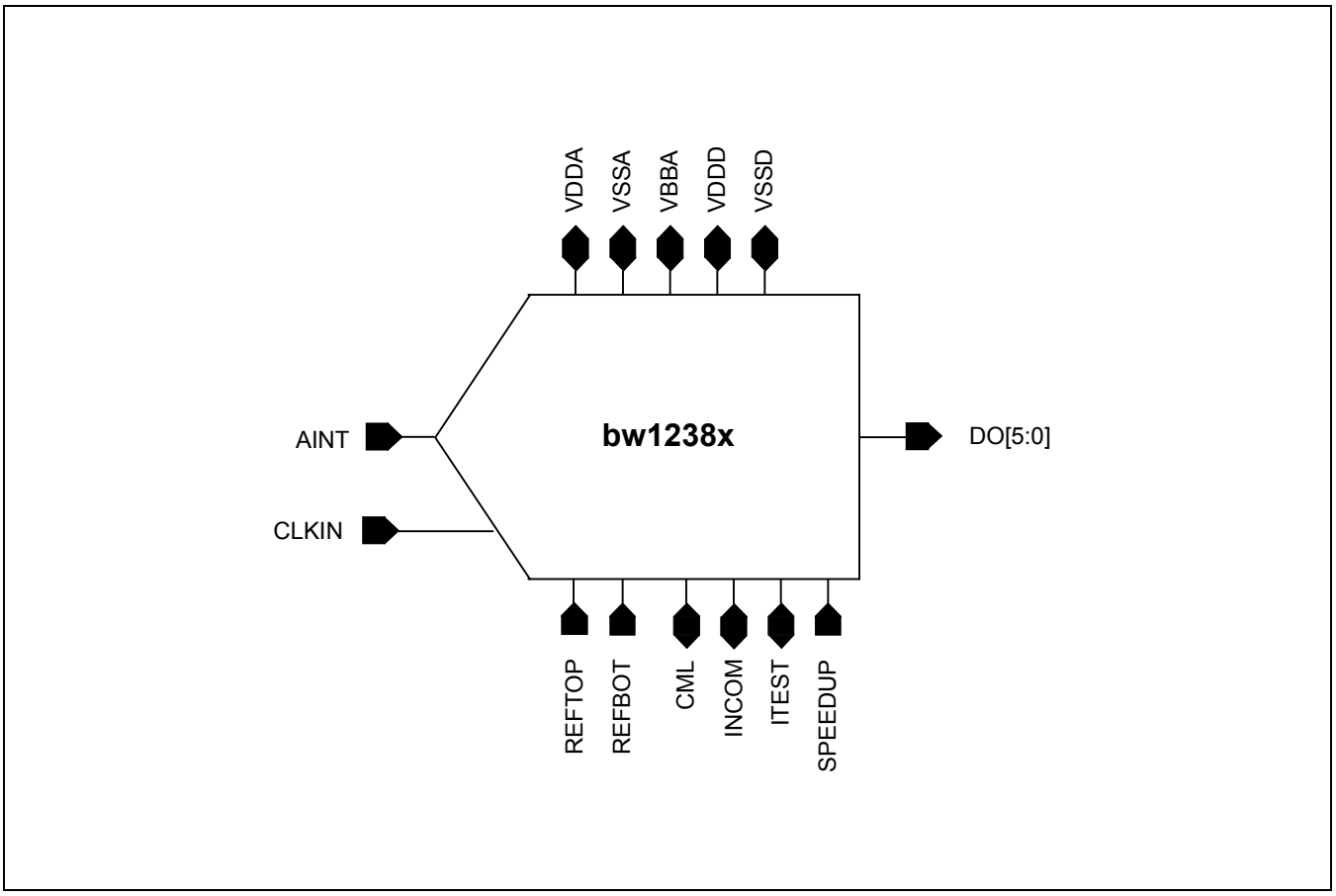
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
REFTOP	AI	pia_bb	Reference Top Bias (2.0V)
REFBOT	AI	pia_bb	Reference Bottom Bias (1.0V)
CML	AB	pia_bb	Internal Bias Point (open=use internal bias circuit)
VDDA	AP	vdda	Analog Power (3.3V)
VBBA	AG	vbba	Analog Sub Bias
VSSA	AG	vssa	Analog Ground
AINT	AI	piar10_bb	Analog Input Input Span : 0.5~2.5 V
INCOM	AB	pia_bb	Internal Bias Point (open=use internal bias circuit)
SPEEDUP	DI	piar10_bb	Speed test pin (normally, VDDA)
ITEST	AB	piar10_bb	Internal Bias Point (open=use internal bias circuit)
CLKIN	DI	piar50_bb	Clock Input
DO[5:0]	DO	poa_bb	Digital Output
VSSD	DG	vssd	Digital Ground
VDDD	DP	vddd	Digital Power (3.3V)

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	4.5	V
Analog Input Voltage	AINT	VSS to VDD	V
Digital Input Voltage	CLKIN	VSS to VDD	V
Digital Output Voltage	V_{OH}, V_{OL}	VSS to VDD	V
Reference Voltage	REFTOP/REFBOT	2.0/1.0	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTE:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5KW resistor (Human body model).

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA - VSSA VDDD - VSSD	3.15	3.3	3.45	V
Supply Voltage Difference	VDDA - VDDD	-0.1	0.0	0.1	V
Reference Input Voltage	REFTOP REFBOT	– –	2.0 1.0	– –	V
Analog Input Voltage	AINT	0.5	–	2.5	V
Digital Input 'L' Voltage Digital Input 'H' Voltage	V_{IL} V_{IH}	– 3.0	– –	0.3 –	V
Operating Temperature	Topr	0	–	70	°C

NOTE: It is strongly recommended that all the supply pins (VDDA, VDDD, VDDO) be powered from the same source to avoid power latch-up.

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	–	–	6	–	Bits	–
Reference Current	IREF	0.80	0.91	1.00	mA	REFTOP: 2.0V REFBOT: 1.0V
Differential Linearity Error	DLE	-1.00	0.29	1.00	LSB	AINT : 0.5V - 2.5V (Ramp Input) Fs : 250MHz
Integral Linearity Error	ILE	-1.00	0.42	1.00	LSB	
Offset Error Voltage	OFF	-1	0.24	1	LSB	
Gain Error Voltage	GAIN	-2	-1.83	2	LSB	

NOTES:

1. Converter Specifications (unless otherwise specified)
   VDDA=3.3V VDDD=3.3V VBBA=0.0V
   VSSA=0.0V VSSD=0.0V
   REFTOP=2.0V REFBOT=1.0V
   Ta=25°C
2. TBD : To Be Determined

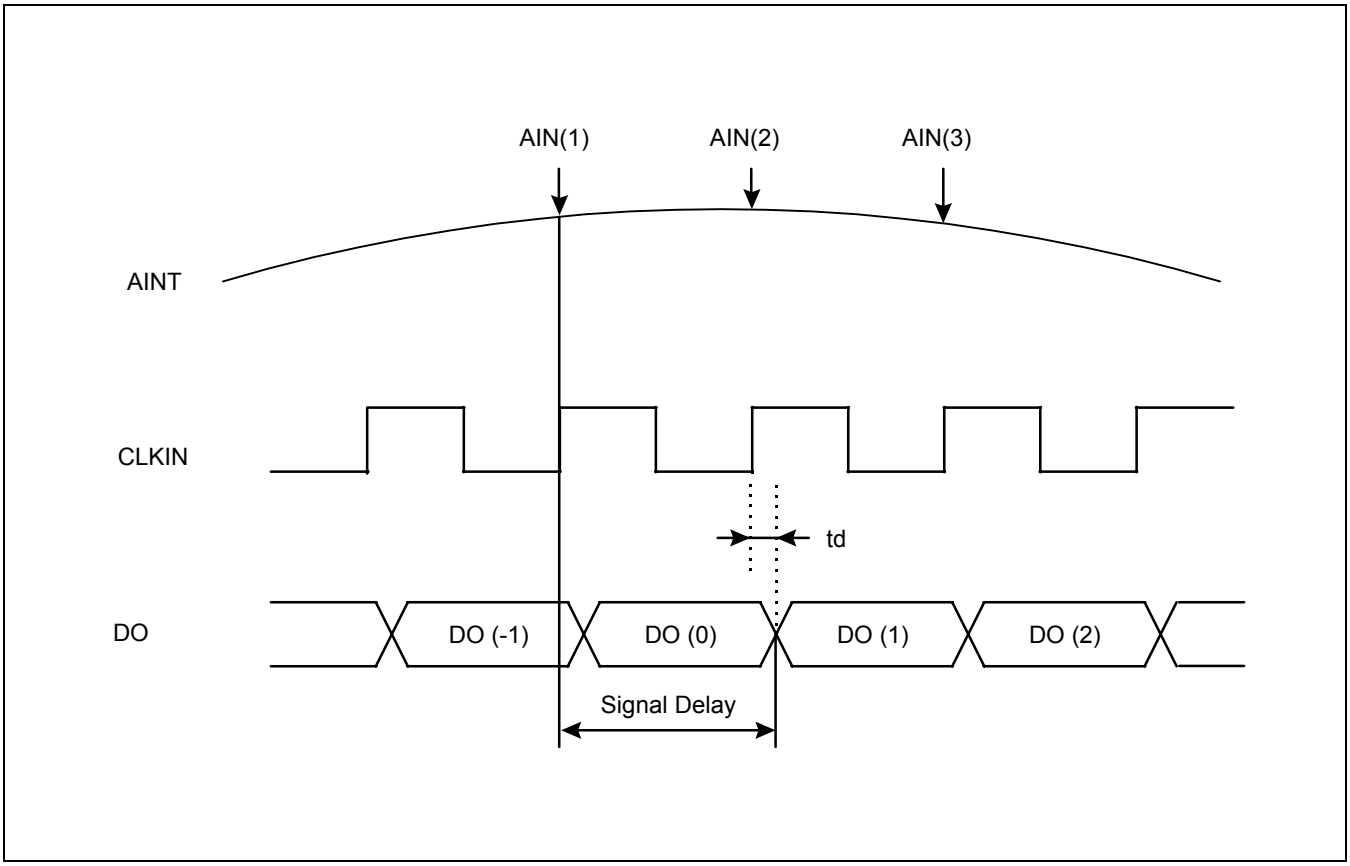
AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Conversion Rate	Fs	–	–	250	MSPS	
Clock Low Time	Tpwl	–	4.0	–	ns	
Conversion Rate	Fs	–	120	–	MSPS	
Dynamic Supply Current	Is	69.0	72.6	76.0	mA	Is = I(VDDA) + I(VDDD) Fs : 250MHz
Digital Output Data Delay	td	1.0	1.1	1.2	ns	See "DELAY TIMING DIAGRAM"
Signal to Noise and Distortion Ratio	SNDR	31.6	34.8	37.2	dB	AINT : 40MHz (Sine Input) Fs : 250MHz

I/O CHART

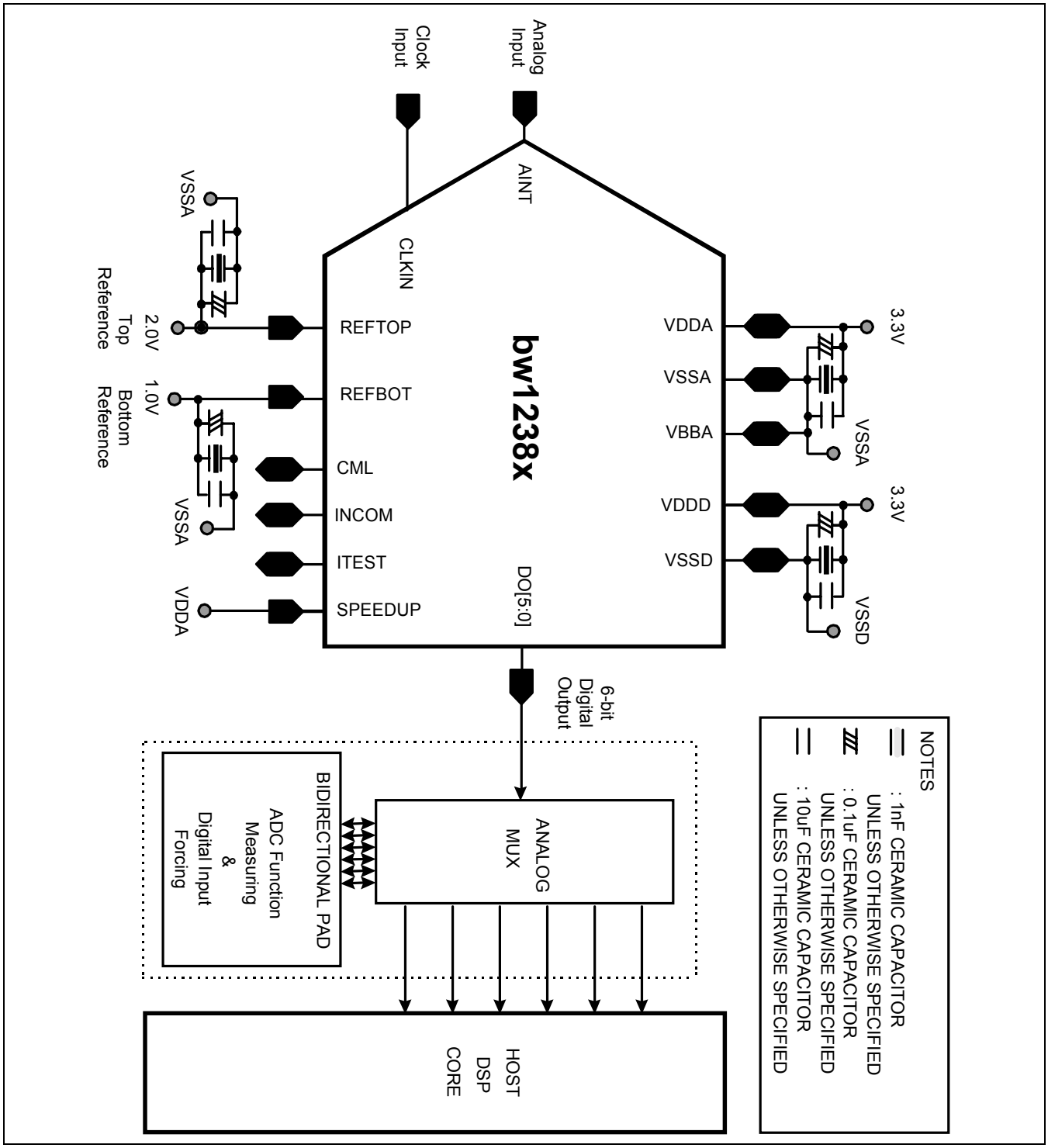
Index	AINT Input (V)	Digital Output	
0	0.50000 ~ 0.53125	000000	1LSB=31.25mV
1	0.53125 ~ 0.56250	000001	for single input
2	0.56250 ~ 0.59375	000010	REFTOP=2.5V
. . .	. . .	. . .	REFBOT=0.5V
511	1.46875 ~ 1.50000	011111	
512	1.50000 ~ 1.53125	100000	
513	1.53125 ~ 1.56250	100001	
. . .	. . .	. . .	
61	2.40625 ~ 2.43750	111101	
62	2.43750 ~ 2.46875	111110	
63	2.46875 ~ 2.50000	111111	

DELAY TIMING DIAGRAM

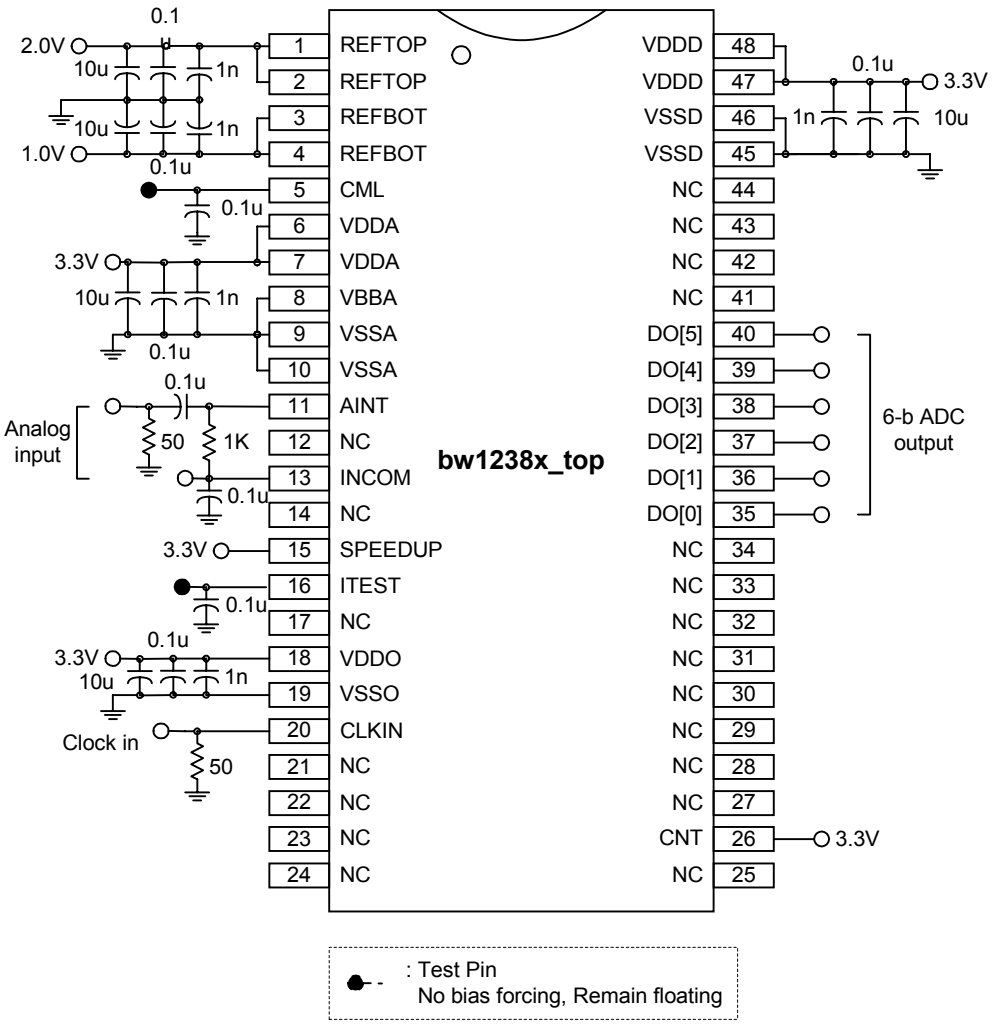


CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages should be biased externally through REFTOP and REFBOT pins.



PACKAGE CONFIGURATION



NOTE: NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

Name	Pin No.	I/O Type	Pin Description
REFTOP	1,2	AI	Reference Top (2.0V)
REFBOT	3,4	AI	Reference Bottom (1.0V)
CML	5	AB	Internal Bias Point (Open=use internal bias circuit)
VDDA	6, 7	AP	Analog Power (3.3V)
VBBA	8	AG	Analog Sub Bias
VSSA	9, 10	AG	Analog Ground
AINT	11	AI	Analog Input +
INCOM	13	AB	Analog Input - (Open=use internal bias circuit)
SPEEDUP	15	DI	Speed test pin. Tie to VDDA (3.3V)
ITEST	16	AB	Internal Bias Point (Open=use internal bias circuit)
VDDO	18	PP	Output Driving Power (3.3V)
VSSO	19	PG	Output Driving Ground
CLKIN	20	DI	Clock Input
CNT	26	DI	Output buffer test pin. Tie to VDDD (3.3V)
DO[5:0]	35~40	DO	Digital Output
VSSD	45,46	DG	Digital Ground
VDDD	47,48	DP	Digital Power (3.3V)

NOTES:

1. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.
2. INCOM is the other pin of differential input, which is fixed to 1.5 V internally.
3. CML is the bias pin, which is fixed to 1.5 V internally.
4. ITEST is the test pin of bias generator. When initial bias function is working normally the pin is fixed to 0.9 V.
5. VDDO and VSSO are output driving power pads.

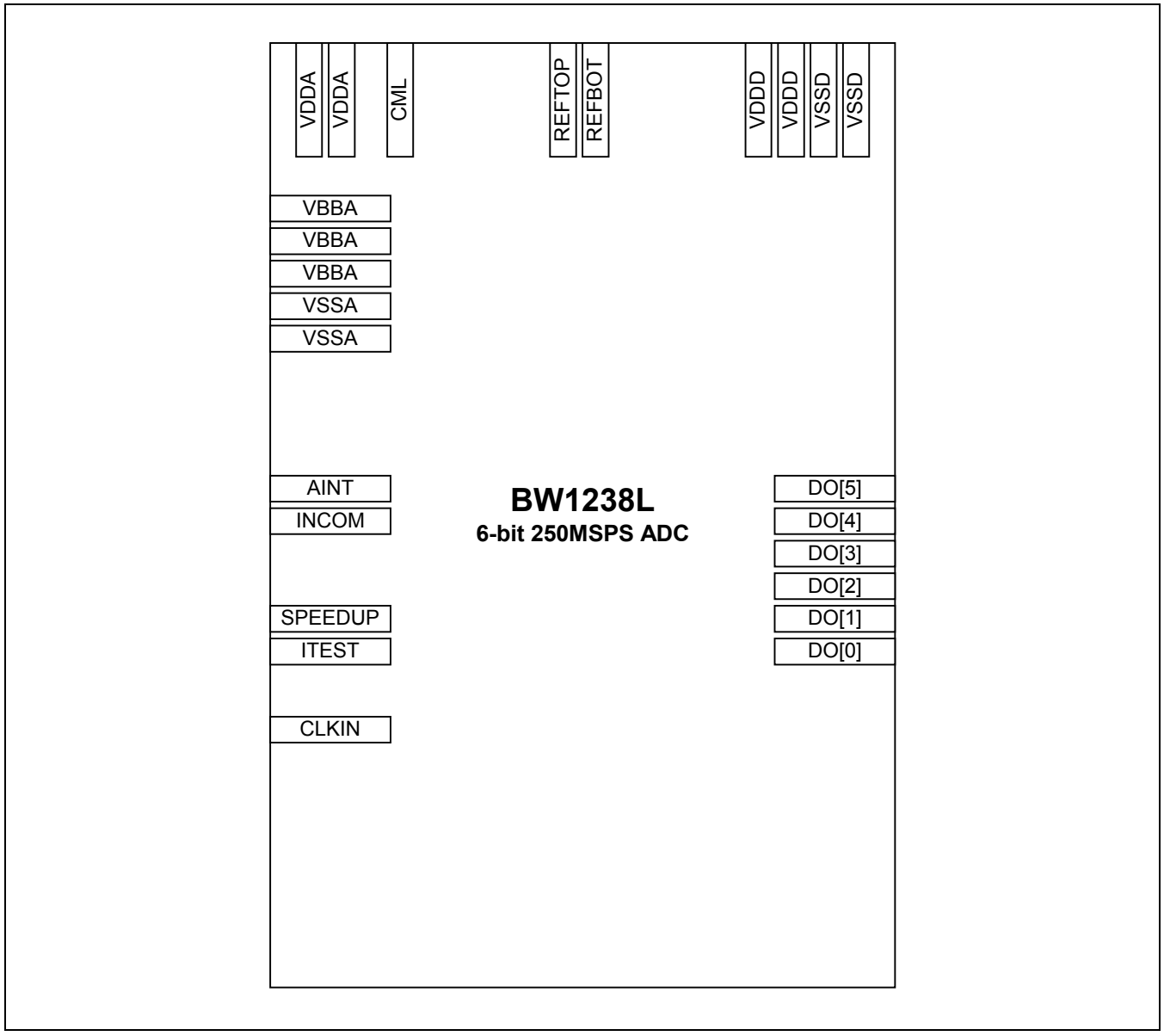
USER GUIDE

1. Input signal type

The ADC was designed to use only single mode input from AINT. To use this ADC as the differential mode inputs, contact to SEC.

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



PHANTOM CELL INFORMATION (Continued)

Pin Name	Pin Usage	Pin Layout Guide
VDDA	External	- Maintain the large width of lines as far as the pads. - place the port positions to minimize the length of power lines. - Do not merge the analog powers with anoter power from other blocks. - Use good power and ground source on board.
VSSA	External	
VBBA	External	
VDDD	External	
VSSD	External	
AINT	External/Internal	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
CLKIN	External/Internal	- Separate from all other analog signals
REFTOP	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFBOT	External/Internal	
CML	External/Internal	
ITEST	External/Internal	
INCOM	External/Internal	
SPEEDUP	External/Internal	
DO[5]	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
DO[4]	External/Internal	
DO[3]	External/Internal	
DO[2]	External/Internal	
DO[1]	External/Internal	
DO[0]	External/Internal	

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

Characteristics	Min	Typ	Max	Unit	Remarks
Analog power supply voltage				V	
Digital power supply voltage				V	
Bit resolution				Bit	
Reference input voltage				V	
Analog input voltage				Vpp	
Analog input bandwidth (Maximum input frequency)				MHz	
Operating temperature				°C	
Integral non-linearity error				LSB	
Differential non-linearity error				LSB	
Bottom offset voltage error				mV	
Top offset voltage error				mV	
Maximum conversion rate				MSPS	
Dynamic supply current				mA	
Power dissipation				mW	
Signal-to-noise ratio				dB	
Pipeline delay				CLK	
Output loading capacitance				pF	
Digital output format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?
2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.
3. Freely list those functions you want to be implemented in our ADC, if you have any.

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	99.3.20	Original version published	
ver 1.1	99.12.13	1. Upgrade to the released version 2. Insert the History Card Section	
ver 2.0	02.3.10	Add I/O CHART, USER GUIDE, and PHANTOM CELL INFORMATION	

NOTES