10BIT 80MSPS DUAL DAC BW1221L

GENERAL DESCRIPTION

The BW1221L is a CMOS Dual 10Bit D/A converter for general & video applications. Its maximum conversion rate is 80MSPS (typical 50MSPS) and supply voltage is 3.3V single. An external 1.0V voltage reference(VREF) and a single resistor (RSET) control the full_scale output current.

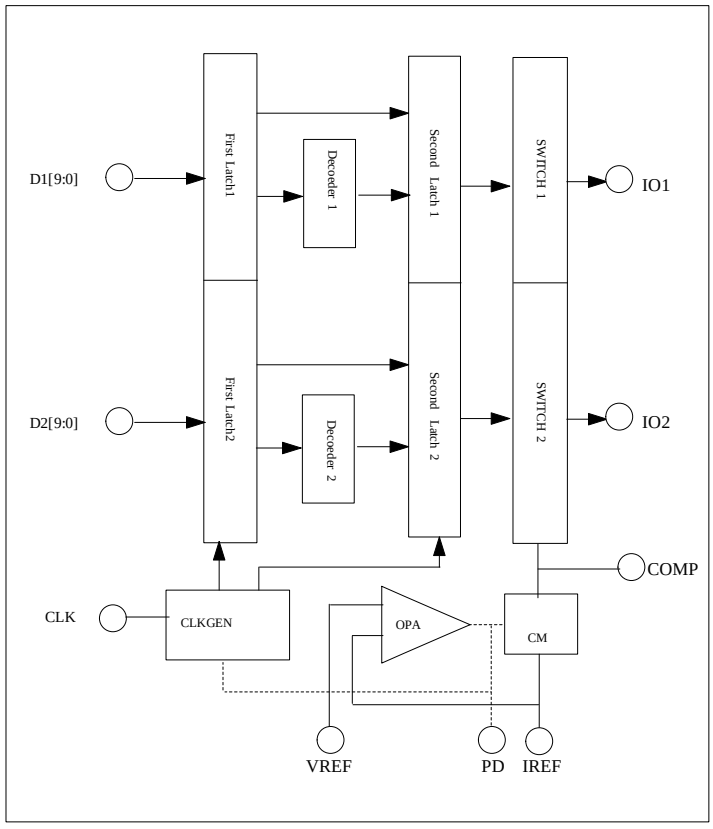
TYPICAL APPLICATIONS

- High Definition Television(DTV,HDTV)
- High Resolution Color Graphics
- Hard Disk Driver(HDD)
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Conventional Digital to Analog Conversion

FEATURES

- 80MSPS 1CLK pipeline delay operation
- +3.3V CMOS monolothic construction
- ±0.4LSB differential linearity error(Typ)
- ±1.5LSB integral linearity error(Typ)
- External voltage reference
- Dual Channel DAC
- 10-Bit voltage parallel input per channel
- High impedance single current output
- Bineary coding input
- High impedance analog output current source

FUNCTIONAL BLOCK DIAGRAM



Ver 1.1 (Dec. 1998)

CORE CONFIGURATION

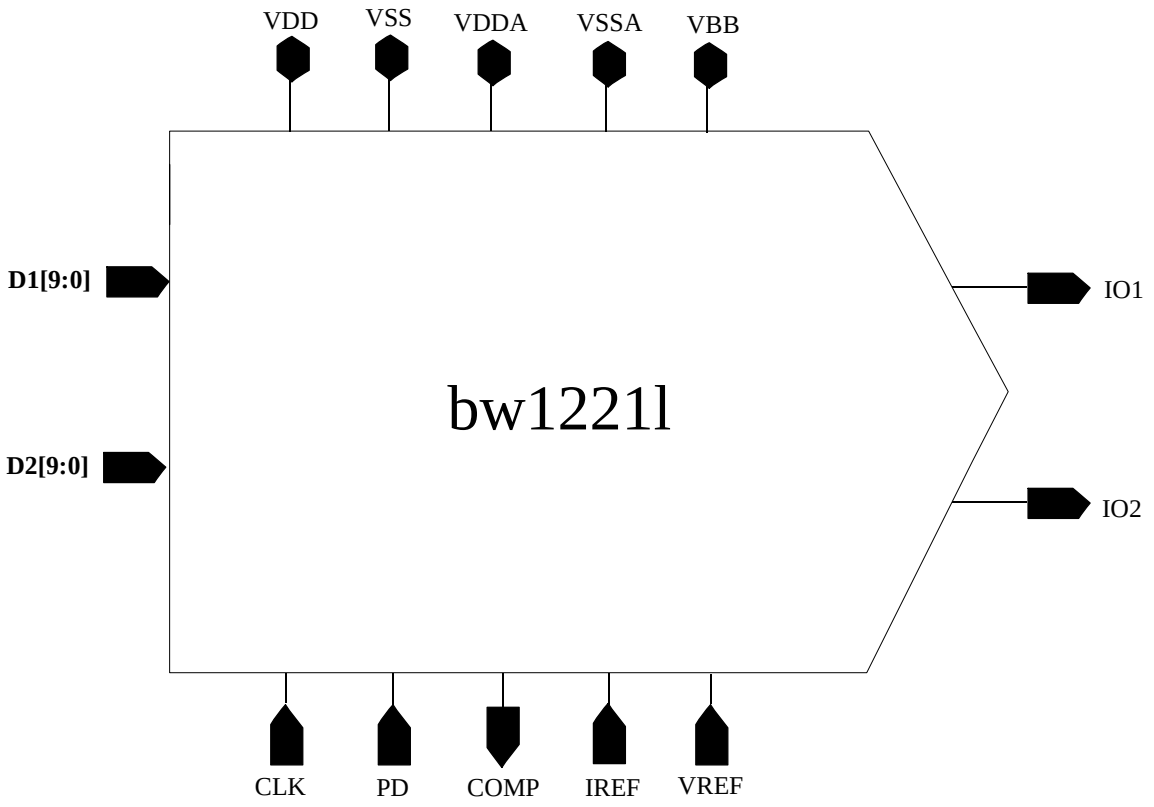
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
D1[9:0]	DI	picc_bb	1st Channel Digital input
D2[9:0]	DI	picc_bb	2nd Channel Digital input
IO1	AO	poa_bb	1st Channel Current Output
IO2	AO	poa_bb	2nd Channel Current Output
CLK	DI	picc_bb	Clock Input
VREF	AI	pia_bb	Reference voltage input
COMP	AI	pia_bb	External capacitance connection
PD	DI	picc_bb	Power-Down High Enable
IREF	AI	pia_bb	external resistor connection
VDDA	AP	vdda	Analog Power
VDDD	DP	vddd	Digital Power
VSSA	AG	vssa	Analog Ground
VSSD	DG	vssd	Digital Ground
VBB	AG	vbba	Bulk Bias

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

- AB : Analog Bidirection
- DB : Digital Bidirection



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	VALUES	UNIT
Supply Voltage	VDDA VDDD	5	V
Voltage on any Digital Voltage	Vin	VSSD-0.3 to VDDD+0.3	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTE:

* It is strongly recommended that to avoid power latch-up all the supply Pins(VDDA,VDDD) be driven from the same source, and all ground Pins(VSSA,VSSD,VBB) be driven from the same source.
* Absolute Maximum Rating values should be applied individually while all other parameters are within specified operating conditions. Function operation under any of these conditions is not implied.
* Applied voltage must be limited to specified range.
* Absolute Maximum Ratings are values beyond which the device may be damaged permanently. Normal operation is not guaranteed.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Operating Supply Voltage	VDDA,VDDD	3.15	3.3	3.45	V
Digital input Voltage HIGH LOW	V_{IH} V_{IL}	0.7VDDD -	3.3 0.0	- 0.3VDDD	V
Operating Temperature Range	T_{opr}	0	25	70	°C
Output Load(effective)	R_L	-	37.5	-	Ω
Data Input Setup Time	T_S	-	2	-	ns
Data Input Hold Time	T_H	-	2	-	ns
Clock Cycle Time	t_{CLK}	12.6	20	-	ns
Clock Pulse Width High	t_{PWH}	6	10	-	ns
Clock Pulse Width Low	t_{PWL}	6	10	-	ns
IREF Current	I_{REF}	1.5	1.77	2.0	mA
Zero_level Voltage	V_{OZ}	-5.0	-1.2	5.0	mV
External Reference Voltage	V_{REF}	-	1.0	-	V

NOTE:

• It is strongly recommended that all the supply pins(VDDA,VDDD) should be driven from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Resolution	-	-	10	-	Bits
Differential Linearity Error	DLE	-	±0.4	±1.0	LSB
Integral Linearity Error	ILE	-	±1.5	±2.0	LSB
Full Scale Current per Channel	I_{fs}	23	25	28	mA
Monotonicity	-	-	Guaranteed	-	-
LSB Size	-	23	25	28	uA
Maximum Output Compliance	V_{oc}	-0.5	0.0	0.2	V
Exteranl Refence Voltage	-	-	1.0	-	V
Power Supply Current	I_s	50	54	60	mA

NOTES

* Converter Specifications (unless otherwise specified)
  VDDA=3.3V VDDD=3.3V VSSA=VSSD=VBB=GND
  Ta=25°C R_{L1}=R_{L2}=37.5Ω , V_{REF}=1.0V, R_{set} = 564Ω
* TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Conversion Speed	f_{MAX}	-	50	80	MHz
Analog Output Delay	T_d	-	11	20	ns
Analog Output Rising Time	T_r	-	15	25	ns
Analog Output Falling Time	T_f	-	19	30	ns
Analog Output Settling Time	T_{set}	-	100	150	ns
Glitch Impulse	GI	-	±120	±200	pVsec
Pipeline Delay	T_{op}	-	1	-	Clock
Power Supply Rejection Ratio (f=1KHz, COMP=0.1uF)	PSS	-	0.0	0.5	%
Feedthrough	fdth	-	-33	-28	dB
Power_Down On Time	T_{pn}	-	4	6	ms
Power_Down Off Time	T_{pf}	-	0.1	0.3	ms

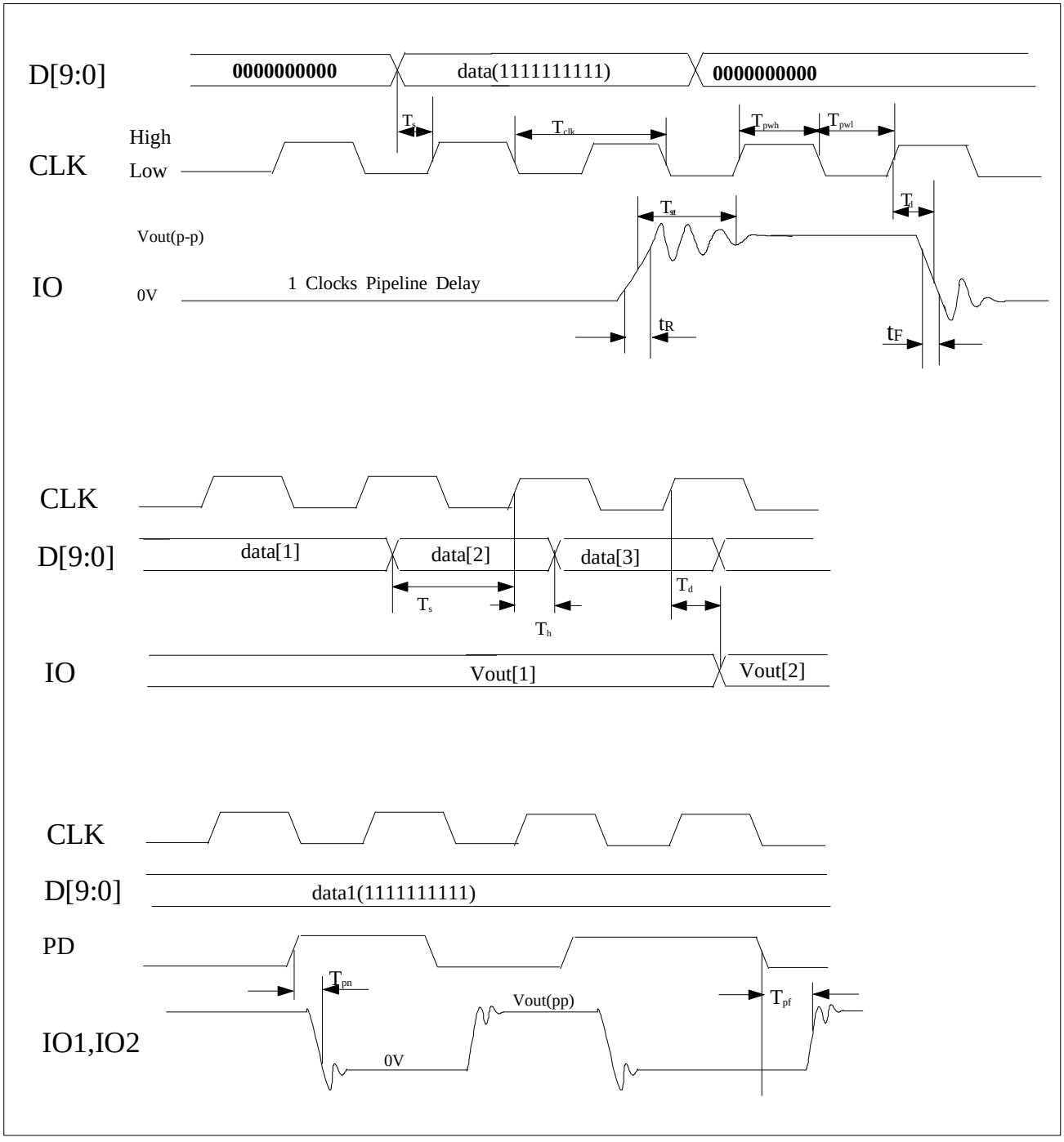
NOTE:

- The above pararameters are not tested through the temperature range.
- Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Settling time does not include clock and data feedthrough. Glitch impulse include clock and data feedthrough.

FUNCTIONAL DESCRIPTION

This is dual 10bit 80MSPS digital to analog data converter and uses segment architecture for 5bits of MSB sides and binerary-weighted architecture for 5bits of LSB side. It contains of 1st latch block, decoder block, 2nd latch block, OPA block, CM(current mirror)block and analog switch block. This core uses reference current to decide the 1LSB current size by dividing the reference current by 68times. So the reference current must be constant and the reference curretn of CM can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of the matching characteristic on analog switch and CM block. And more than 80% of supply current is dissipated at analog switch block and OPA block. And it uses samsung(SEC) standard cell as all digital cell of latch,decoder and buffer. And to adjust full current output, you must decide the "Rset" resistor value(connected to IREF pin) and "Vbias" voltage value(connected to VREF pin). Its voltage output can be obtained by connecting R_{L1}(connected to IO1 pin) and R_{L2}(connected to IO2 pin). Its maximum output voltage limit is 1.2V. So you must decide the R_{L1}, R_{L2}, Vbias and Rset carefully not Vout(p-p) to exceed 1.2V. It contains PD pin for power-save but regretfuly it isn't complete. If you want more complete power-save mode, call back us(SEC). We can provide you more complete power-save mode control scheme.

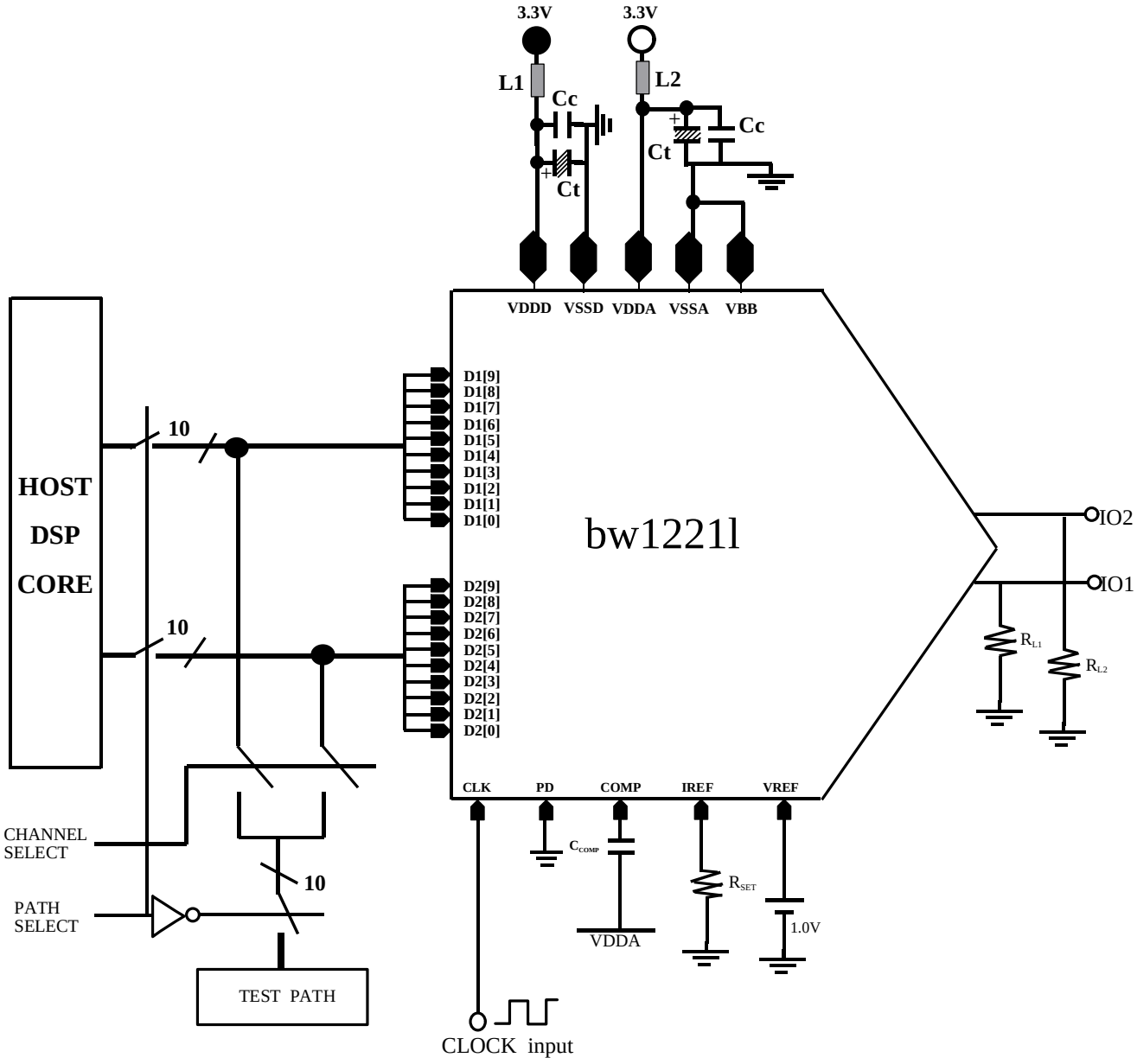
TIMING DIAGRAM



NOTES:

- The Behavioral Modeling is provided by Verilog HDL modeling file which includes the spec of pipeline delay, setup_time, hold_time, rising time, falling time, and clock frequency, and so on.
- Output delay(T_d) measured from the 50% point of the rising edge of CLK to the full scale trasition
- Settling time(T_{set}) measured from the 50% point of full scale transition to the output remaining within ±1LSB.
- Output rising(T_r)/falling(T_f) time measured between the 10% and 90% points of full scale transition.
- Power_down doesn't need clock signal.

CORE EVALUATION GUIDE



LOCATION	DESCRIPTION
C_{COMP},Cc	0.1μF CERAMIC CAPACITOR
Ct	10μFTANTALUM CAPACITOR
R_{SET}	564Ω
R_{L1}	37.5Ω
R_{L2}	37.5Ω
V_{REF}	1.0V DC Voltage Supply

*** How to change the resolution**

If it is needed to change the resolution, you can use as many as more significant bits, and the rest (less significant bits) can be grounded or supplied by VDDD power. That is, if you need only 8bits, you have to use MSB 8bit digital input pin, and the LSB 2 digital input pin have to be grounded or supplied by VDDD power.

*** How to change the output range**

You can change the output swing using the following equation:

$$\mathbf{Vout = \{ V_{ref} / (R_{set}*68) \} * 1023 * R_L}$$

This equation implies that you can determine the output swing by changing the value of Vref, R_{set}, and R_L where the output swing is limited up to 1.2V.

1. ABOUT TESTABILITY

If you want to test it over full spec via all channel in main chip(that is, when it is used as a block of main chip) you must add many pins(for 20pins of digital inputs, 2pins of analog outputs, etc) at the main chip to test this DAC block. But usually it is nearly impossble 'cause the total number of pins at main chip is limited. So more efficient method for testing this DAC block is needed. We offer two efficient ways of testing here as a reference. But remember that this is not the best way. You can test it by your own testing method.

2. FIRST METHOD OF TESTABILITY

The first way is adding only extra 10PADs for 10bit parallel digital inputs and 2PADs for channel selecting and path selecting. You can check two channels one by one, that is you can test only one channel at one time. Therefore you can test all two channels by turn but cannot check all channels at one time. And this method needs extra analog MUX and switch blocks for testing. Furthermore we cna assure all channels by testing only one channel because the two channels have same architecture and share the same analog reference block(OPA, CM). This characteristic makes it simple to test this DAC block(when it is embedded in main chip) by adding another 10PADs and selecting 2PADs for selecting one channel analog switch block of DAC out of two chab\nnels.

3. SECOND METHOD OF TESTABILITY

If above extra 12PADs are burden on you, then you can test it by this second method to reduce the extra PADs for testing. What is different from above method is that this way needs only 2 extra PADs(one for 1bit input and the other for clock signal), but you must insert extra serial to parallel converter block for converting 1bit 10times speedy digital input to 10bit parallel digital inputs. And this block needs considerable area. Further this method also needs extra 2PADs for channel selecting and path selecting.

4 ANALYSIS

The voltage applied to VREF is measured at IREF node . And the voltage value is proportioned to the reference current value of resistor which is connected to IREF node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPA. For reference, as VREF applied to VREF node is given at IREF node, the current flowing through RSET is given as VREF/RSET.

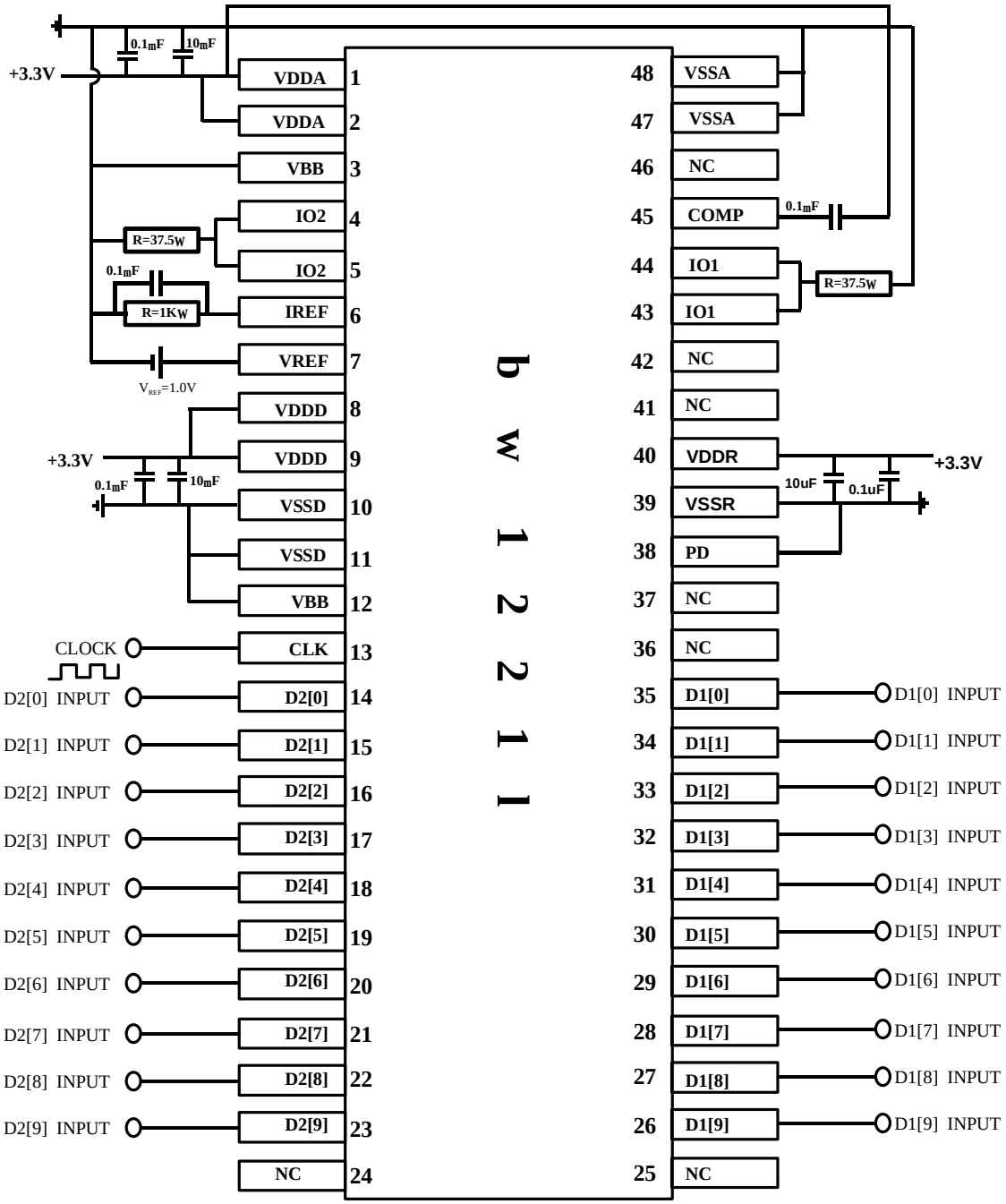
If the voltage applied to VREF node is not same with IREF node, you can say "This DAC chip does not work properly", because the internal OPAMP block makes the two node voltage(IFEF pin, VREF pin) equal.And you have to check the COMP node to see the desired voltage on it. If the desired voltage is not measured, you can check the DAC output by appling a voltage to the node directly.

CORE LAYOUT GUIDE

Layout DAC core replacement

- It is recommended that you use thick analog power metal. When connecting to PAD, the path should be kept as short as possible, and use branch metal to connect to the center of analog switch block.
- It is recommended that you use thick analog output metal(at least more than 50um) when connecting to PAD, and also the path length should be kept as short as possible. If the metal width is less than 50um, you should use double or triple PADs.
- Digital power and analog power are separately used.
- When it is connected to other blocks, it must be double shielded using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
- Bulk power is used to reduce the influence of substrate noise.
- You must use more than two pins for VDDA because it requires much current dissipation.

PACKAGE CONFIGURATION



NOTE

*Analog and digital supplies should be separated and decoupled.

*Supplies are not connected internally

*All ground pins must be connected. One ground plane is preferred although it depends on the application

PACKAGE PIN DESCRIPTION

PIN NAME	NO	I/O TYPE	DESCRIPTION
VDDA	1,2	AP	Analog Power
VBB	3,12	AG	Bulk Bias
VSSA	47,48	AG	Analog Ground
VSSR	39	PG	PAD Cell Ground
VDDR	40	PP	PAD Cell Power
D2[9:0]	14~23	DI	2nd Channel Digital Input(10bit parallel)
D1[9:0]	26~35	DI	1st Channel Digital Input(10bit parallel)
PD	38	DI	Power-Down Control (High Enable)
VDDD	8,9	DP	Digital Power
VSSD	10,11	DG	Digital Ground
CLK	13	DI	Clock Input (Input Data is latched at the rising edge of CLK)
IO1	43,44	AO	1st Analog Current Output (needs termination resistor:37.5Ω)
IO2	4,5	AO	2nd Analog Current Output (needs termination resistor:37.5Ω)
VREF	7	AI	External Reference DC Voltage Input(1.0V)
IREF	6	AI	RSET resistor(564Ω) connection to adjust full scale current output with VREF
COMP	45	AI	Compensation Capacitor. This pin should be connected to VDDA through bypass capacitor. The COMP capacitor must be as close to the device as possible to keep lead length to an absolute minimun.

NOTES

1.I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

FEEDBACK REQUEST

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				μF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ω	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Interal Reference Voltage(BGR)?
- Which do you want to Serial Input TYPE or parallel Input TYPE?
- Do you need 3.3v and 5v power supply in your system?
- How many channels do you need(BW1221L is dual channel DAC)?

PC BOARD LAYOUT CONSIDERATIONS

♦ PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of vdd (vdda,vddd) pins short as possible so as to minimize inductive ringing.

♦ Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1μF ceramic capacitor is used in parallel with a 10μF tantalum capacitor. The digital power plane(VDDD) and analog power plane(VDDA) are connected through a ferrite bead, and also the digital ground plane(VSSD) and the analog ground plane(VSSA). This ferrite bead should be located within 3inches of the BW1221L. The analog power plane supplies power to the BW1221L of the analog output pin and related devices.

♦Analog Signal Interconnect

To minimized noise pickup and reflections due to impedance mismatch, the BW1221L should be located as close as possible to the output connector.
The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used. By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.