GENERAL DESCRIPTION

The BW0406XB is Sigma-Delta ADC for speech and telephony applications. The product contains both digital IIR and FIR filter. The normal output channels have with 70dB signal to distortion ratio. The output of this device is 14bit linear. An on-chip voltage reference circuit is included to allow the single supply operation.

FEATURES

— Single chip voice line ADC

— Oversampled Sigma Delta modulator

— Output format : linear 14bit
  - When serial interface mode, the 14bit linear data has 16bit format with two don't care bits from LSB
  - 2's complement format

— 256X Oversampling

— On chip Decimation Filter

— Single ended Input

— Sampling Rate of 8~11KHz

— On chip voltage reference circuitry

— Single +3.3V Power Supply

— 2Vpp Input signal swing

— Power Consumption
  - Operating Mode : 6mW Typ(3.3V)
  - Powerdown Mode : 33mW Typ(3.3V)

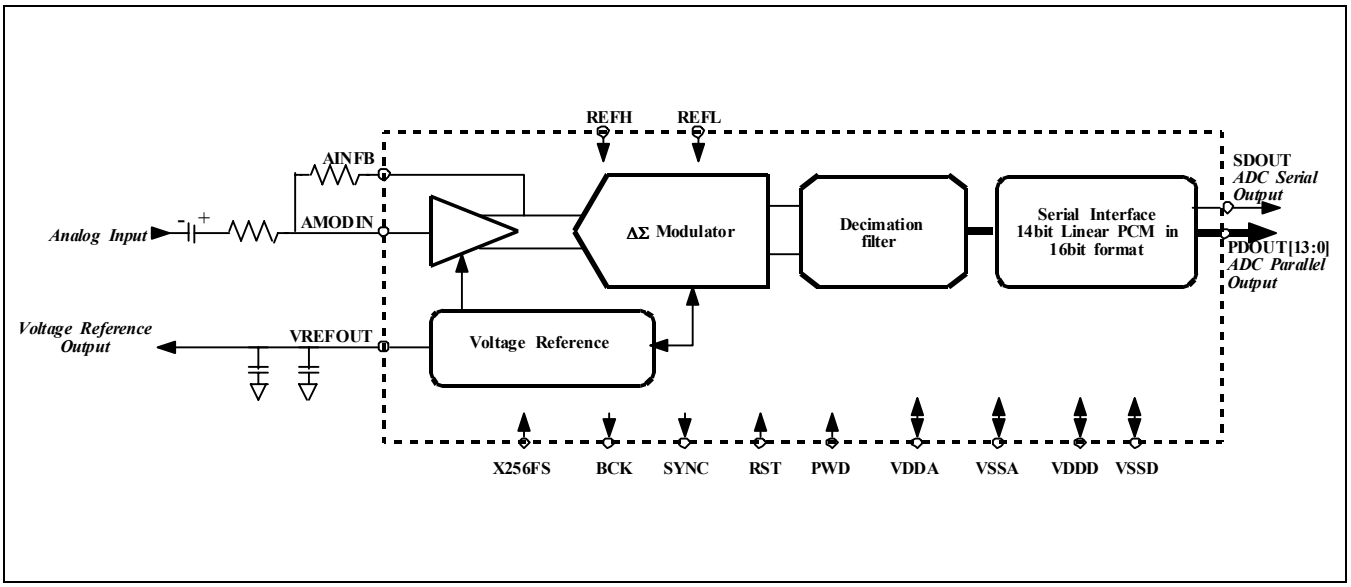
TYPICAL APPLICATIONS

— Speech Processing (Recognition, Synthesis, Compression etc.)

— Telephony

— Modem

BLOCK DIAGRAM WITH INPUT/OUPUT APPLICATION



CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VDDA	AP	vdda	Analog Power (+3.3V)
VSSA	AG	vssa	Analog Ground (0.0V)
REFH	AP	piar50_bb	Analog Reference Power(+3.3V)
REFL	AG	piar50_bb	Analog Reference Ground (0.0V)
AMODIN	AI	piar50_bb	ADC Analog input
VREFOUT	AO	poar50_bb	Vref output
AINFB	AI	piar50_bb	Analog Input Gain control
PWD	DI	picc_bb	Power Down (High active)
RST	DI	picc_bb	Digital Reset (High active)
X256FS	DI	picc_bb	256*Sampling Freq.(FS) Clock
SYNC	DO	pot2_bb	Sampling Freq.(FS) Clock
BCK	DO	pot2_bb	Bit Clock
SDOUT	DO	pot2_bb	Serial Data Output
PDOUT[13:0]	DO	pot2_bb	Parallel Data Output [14bit]
VSSD	DG	vssd	Digital Ground
VDDD	DP	vddd	Digital Power Supply

NOTES:

1. The Power pin(VDDA,VDDD) must be connected by DIODE_SLOT2.
2. The Ground pin (VSSA, VSSD) must be connected bye DIODE_SLOT2.

I/O Type Abbr.

— AI: Analog Input

— DI: Digital Input

— AO: Analog Output

— DO: Digital Output

— AB: Analog Bidirectional

— DB: Digital Bidirectional

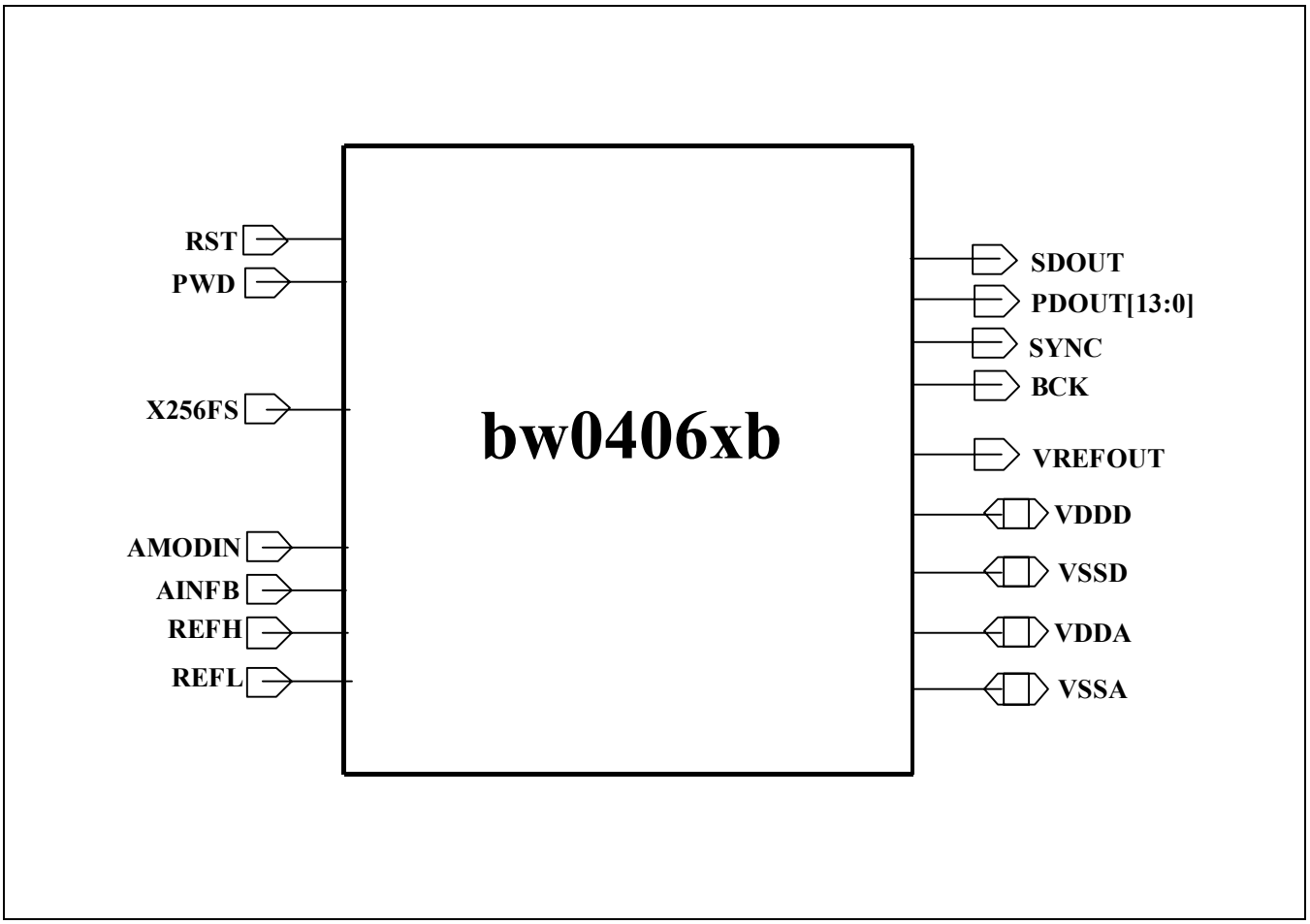
— AP: Analog Power

— DP: Digital Power

— AG: Analog Ground

— DG: Digital Ground

CORE CONFIGURTION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDDD	-0.3 to 3.8	V
Digital Input Voltage	D_{IN}	-0.3 to 3.8	V
Storage Temperature Range	Tstg	-40 to 125	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operations under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(VSSA or VSSD) unless otherwise specified.

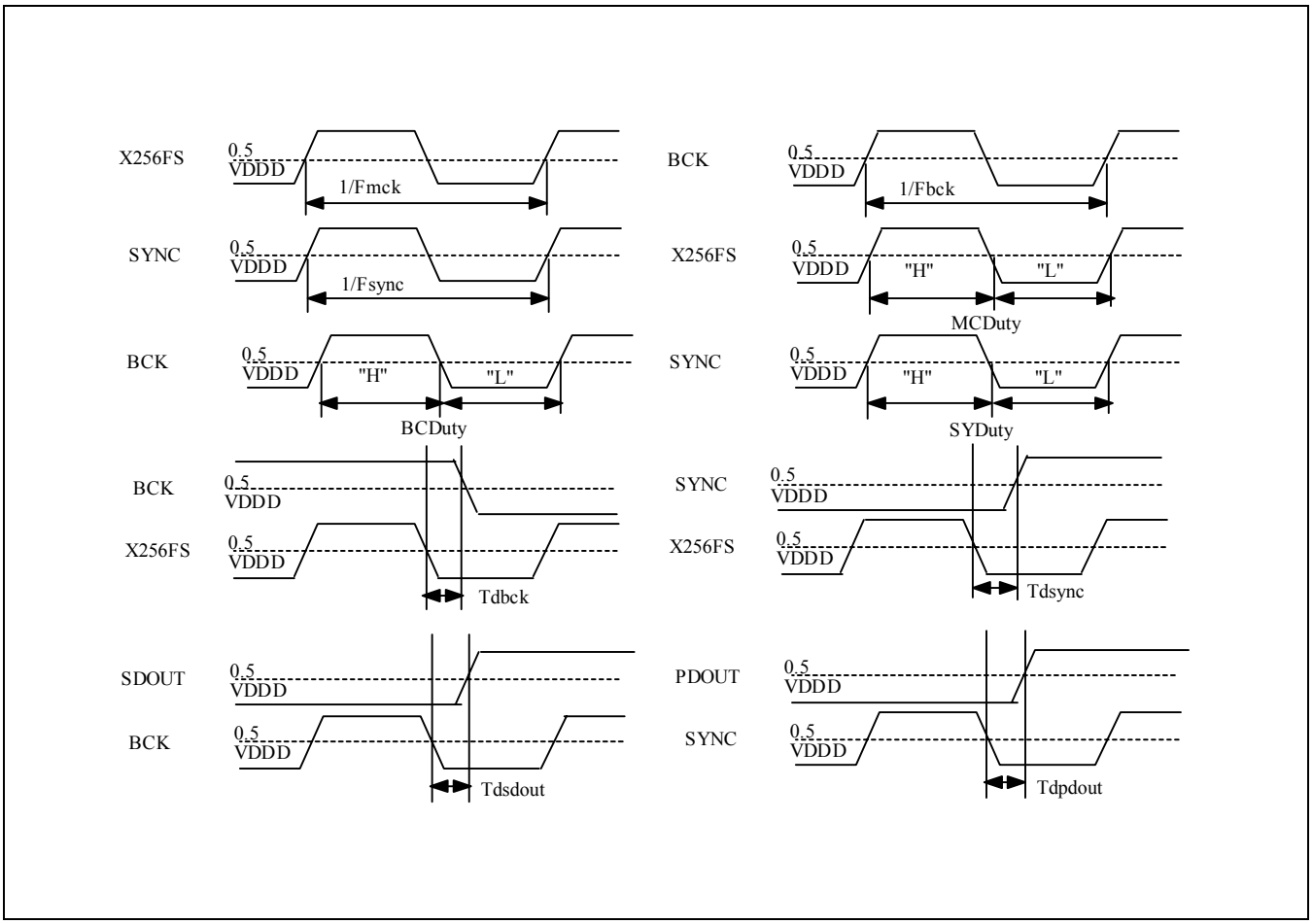
RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA • VSSA VDDD • VSSD	3.15	3.3	3.45	V
Supply Voltage Difference	VDDA • VDDD	0.1	0.0	0.1	V
Digital Input Voltage Range		2.7	3.3	3.6	V
Analog Input Voltage Range		–	2	–	Vpp

NOTE: It is strongly recommended that all the supply pins (VDDA, VDDD) be powered from the same source to avoid power latch up.

CONTROL CLOCK CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
X256FS Frequency	Fmck	-	2.048	-	MHz
BCK Frequency	Fbck	-	128	-	KHz
SYNC Frequency	Fsync	-	8	-	KHz
X256FS Duty cycle (H:L)	MCDuty	40:60	50:50	60:40	%
BCK Duty cycle (H:L)	BCDuty	-	50:50	-	%
SYNC Duty cycle (H:L)	SYDuty	-	50:50	-	%
X256FS Falling and BCK Edge Delay	Tdbck	3	5	7	ns
X256FS Falling and SYNC Edge Delay	Tdsync	3	5	7	ns
BCK Falling and SDOUT Delay	Tdsdout	3	5	7	ns
SYNC Falling and PDOUT Delay	Tdpdout	3	5	7	ns



AC ELECTRICAL CHARACTERISTICS

(Measurement Bandwidth is 20Hz-4KHz. Full scale input sine wave 1KHz, FS=8KHz, @VDDA=3.3V, Ta=25°C, Unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		–	14	–	Bits	
Sampling rate		–	8	–	KHz	–
Analog Input Characteristics						
* Signal to Distortion Ratio		67	70	–	dB	0dB Input : Linear
Offset Error		–	–	±20	mV	–
Input Voltage Range		–	2	–	Vpp	–
Power Supply						
Power comsumption (3.3v Operating Mode) Analog Digital		–	– 1.5 0.25	–	mA	–
Power comsumption (3.3v Powerdown Mode)		–	33	–	mA	

CORE EVALUATION GUIDE

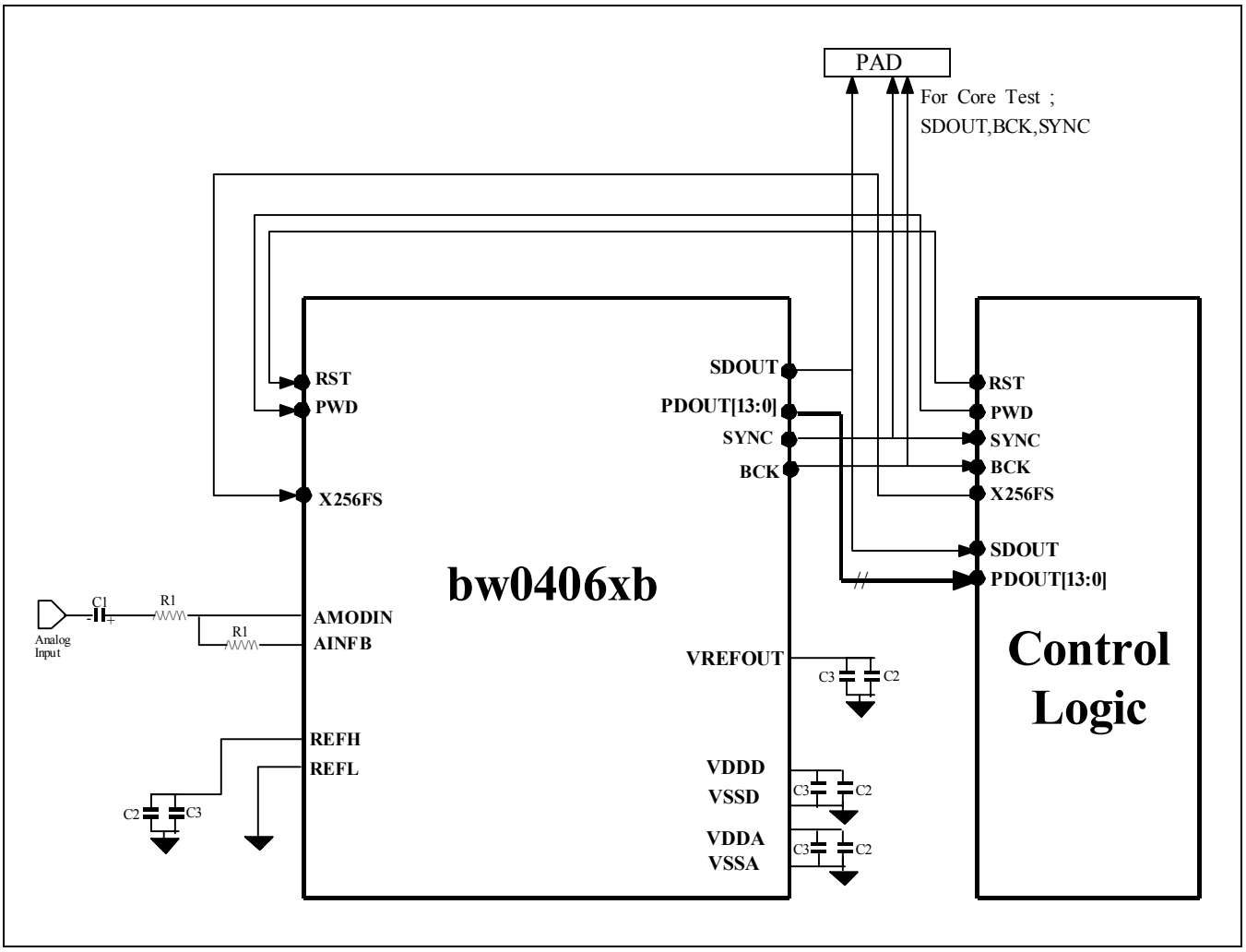


Table 1. The Connection User Guide Line for Embedded Core Test

Location	Description
C3	0.1mF TANTALUM CAPACITOR
C2	10mF CERAMIC CAPACITOR
C1	0.33mF TANTALUM CAPACITOR
R1	50kΩ RESISTOR

NOTES:

1. The analog power/ground must be separated from digital power/ground.
2. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.
3. Power typical value:
   VDDA = VDDD = 3.3V, VSSA = VSSD = 0.0V

TIMING DIAGRAM

The frame of sync clock(SYNC) transitions determine the start of the serial data.

Output data

— All serial output data are clocked out by the falling edge of BCK.

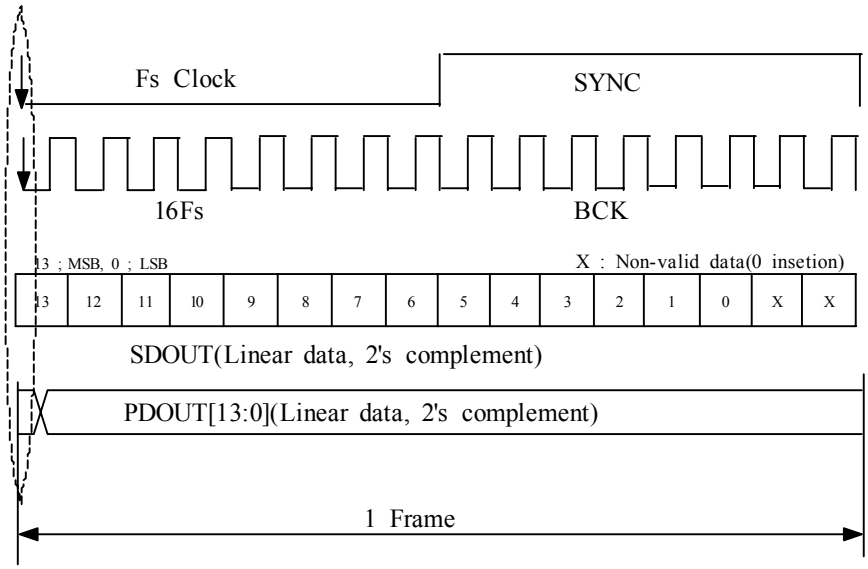
— All parallel output data are clocked out by the falling edge of SYNC.

— 14bit linear PCM

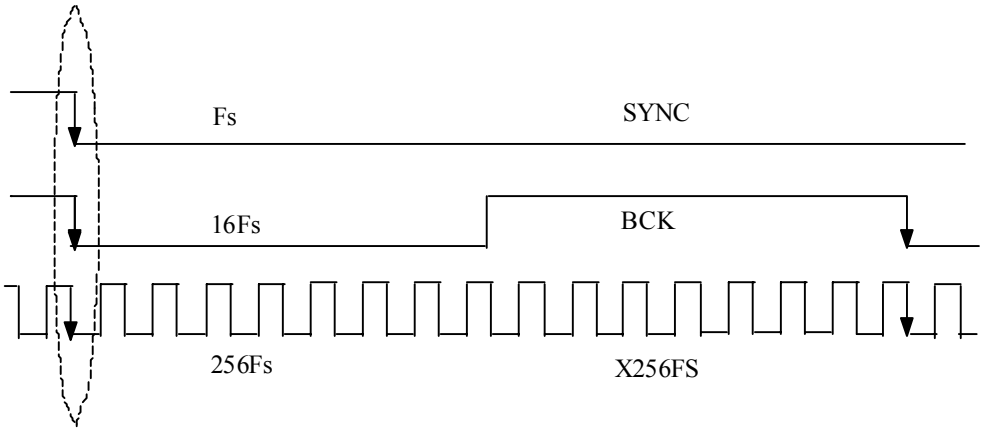
NOTES:

1. SYNC clock is at sampling frequency, Fs
2. 14bit linear data has 16bit serial data format, this is accomplished by 16FS (= Fs clock x 16) and two don't care bits are added from LSB, to fit into 16bit format.

Digital data output interface timing diagram

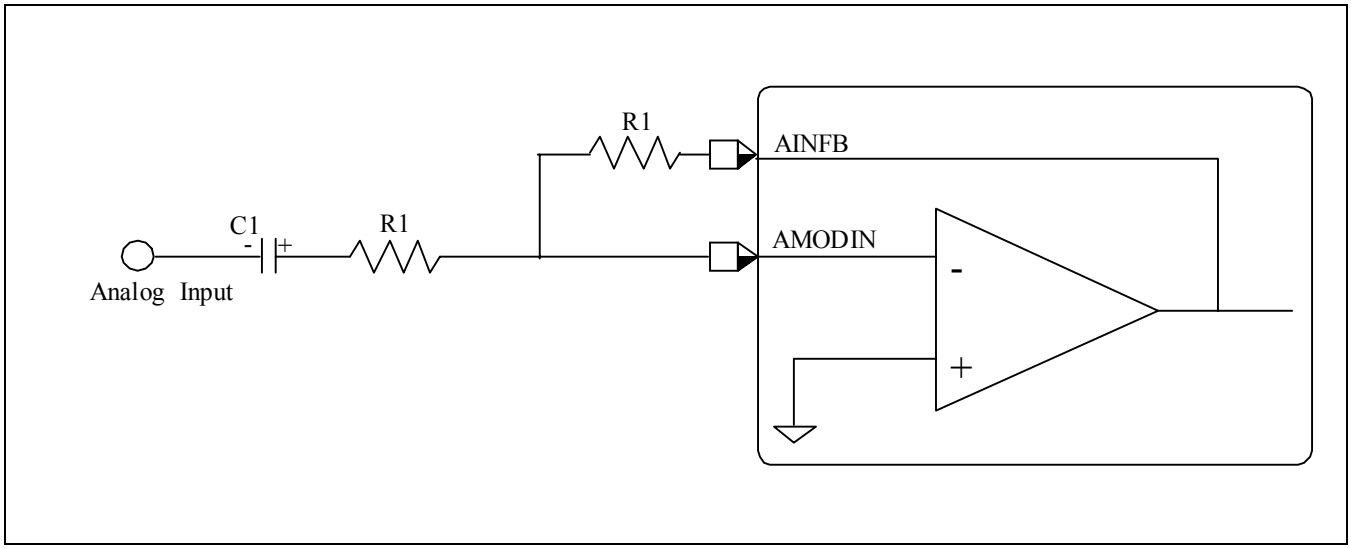


Digital clock interface timing diagram



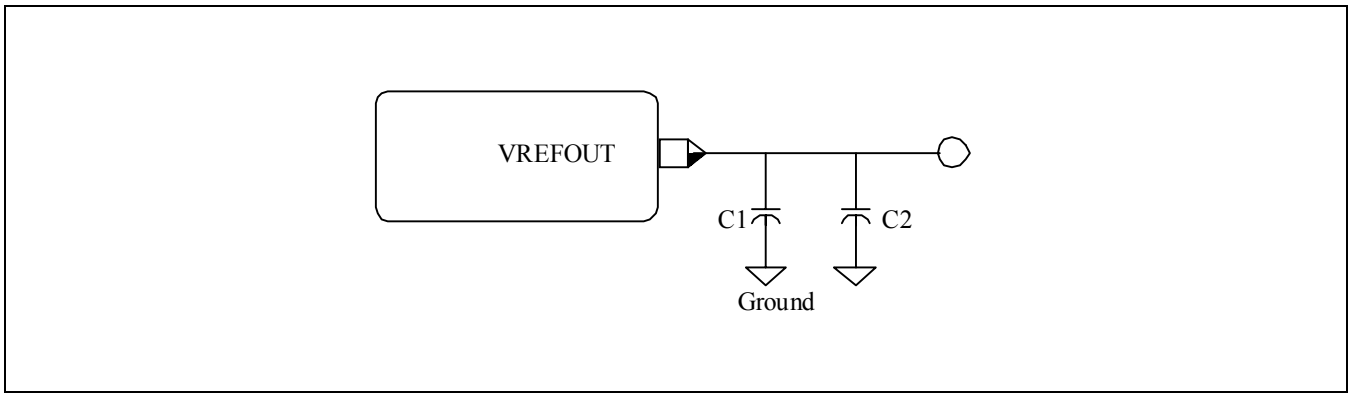
INPUT APPLICATION GUIDE

1. Input stage application guide



Typical value of R1 and C1
R1 > 50KΩ
C1 = 0.33mF

2. VREFOUT port application guide



C1 = 0.1mF, C2 = 10mF
Note: The user should dispose the C1 and C2 as the order shown above and dispose the capacitors to VREFOUT pin as close as possibe.

FEEDBACK REQUEST

It should be quite helpful to our CODEC core development if you specify your system requirements on CODEC in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

— Could you explain external/internal pin configurations as required?

Specially requested function list :

1. What is your signal band to use, 3.6KHz? 4KHz? or 4.8KHz?
2. What is your analog in/output signal voltage swing? and what kind of format do your want as analog signal in/ouput: single or differential format? If you can, Please let us know, what is your exact in/output signal spec.
3. What is your minimum S/N+D spec?
4. Do you want linear phase characteristic or you don't care on digital filter spec?
5. Could you give us exact design spec of speech adc?