

Clock generator for DVD players

BU2363FV

BU2363FV is a clock generator IC that generates necessary clocks for DVD players by standard clock. Video clock can realize high C/N necessary for high-quality vision (PM) by MULTI-PLL Technology. Frequency can be changed by the internal dividing control.

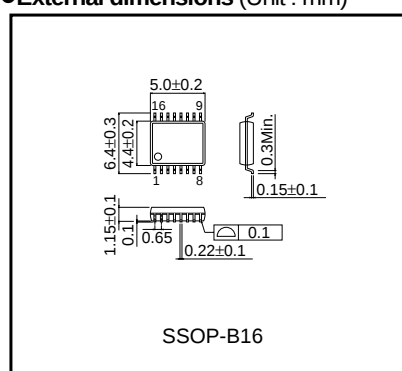
●Applications

DVD player

●Features

- 1) Clock signals are generated when connecting a crystal oscillator.
- 2) SSOP-B16 package
- 3) 3.3V single power supply
- 4) No need additional components (BU2363FV have PLL loopfilter inside)

●External dimensions (Unit : mm)



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V _{DD}	−0.5 to +7.0	V
Input voltage	V _{IN}	−0.5 to V _{DD} +0.5	V
Storage temperature range	T _{stg}	−30 to +125	°C
Power dissipation	P _d	450	mW

*An operation is not guaranteed.

*In case it is used at Ta=25°C or more, 4.5mW is reduced at every 1°C.

*Radiation resistance design is not used.

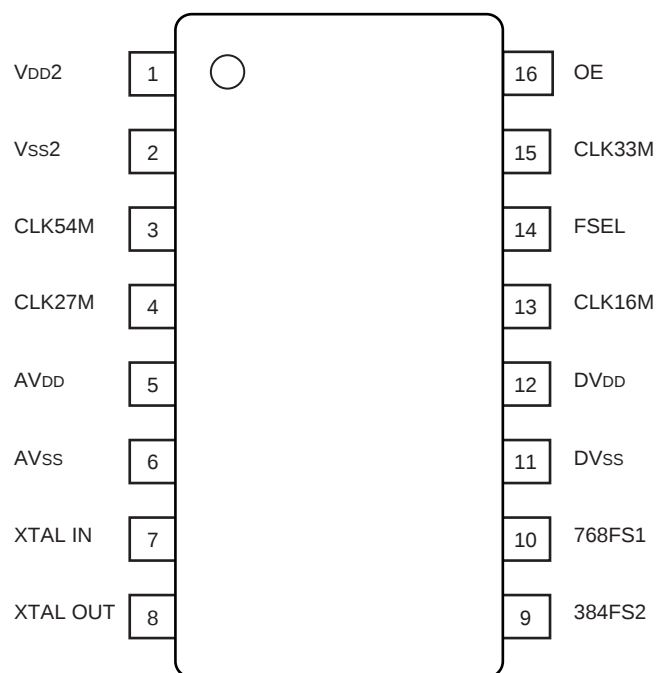
*Power dissipation is measured when BU2363FV is placed on the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	3.0	–	3.6	V
Input "H" voltage range	V _{IH}	0.8V _{DD}	–	V _{DD}	V
Input "L" voltage range	V _{IL}	0	–	0.2V _{DD}	V
Operating temperature range	T _{opr}	−10	–	+70	°C
Output maximum load	C _L	–	–	15	pF

Multimedia ICs

●Block diagram



●Pin descriptions

Pin No.	Pin name	Functions
1	VDD2	27,54MHz VDD
2	VSS2	27,54MHz GND
3	CLK54M	54MHz clock output
4	CLK27M	27MHz clock output
5	AVDD	Analog VDD
6	AVSS	Analog GND
7	XTAL _{IN}	Standard crystal input
8	XTAL _{OUT}	Standard crystal output
9	384FS2	FSEL=OPEN : 18.432MHz, FSEL=LOW : 16.9344MHz
10	768FS1	FSEL=OPEN : 36.864MHz, FSEL=LOW : 33.8688MHz
11	DVSS	Digital GND
12	DVDD	Digital VDD
13	CLK16M	16.9344MHz clock output
14	FSEL	Pin9, 10 output select with pull-up OPEN : 18.432MHz (Pin9), 36.864MHz (Pin10) L : 16.9344MHz (Pin9), 33.8688MHz (Pin10)
15	CLK33M	33.8688MHz clock output
16	OE	output enable(OPEN : enable, LOW : disable) with pull-up

Multimedia ICs

●Input output circuits

Pin No.	Equivalent circuit
Input Pin 14, 16 with pull-up (about 250kΩ)	
Output Pin 3, 4, 9, 10, 13, 15	
Crystal Pin 7, 8	

Multimedia ICs

●Electrical characteristics (Unless specified otherwise Ta=25°C, VDD=3.3V, crystal frequency=36.864MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output 'L' voltage	V _{OL}	–	–	0.4	V	I _{OL} =4.0mA
Output 'H' voltage	V _{OH}	2.4	–	–	V	I _{OH} =–4.0mA
Power supply current	I _{DD}	–	30	50	mA	No load
CLK54M	CLK54M	–	54	–	MHz	XTAL×375/64/4
CLK27M	CLK27M	–	27	–	MHz	XTAL×375/64/8
CLK33M	CLK33M	–	33.8688	–	MHz	XTAL×147/40/4
CLK16M	CLK16M	–	16.9344	–	MHz	XTAL×147/40/8
CLK768FS1	CLK768_H	–	36.864	–	MHz	FSEL=OPEN : XTAL output
	CLK768_L	–	33.8688	–	MHz	FSEL=L : XTAL×147/40/4
CLK384FS2	CLK384_H	–	18.432	–	MHz	FSEL=OPEN : XTAL/2 output
	CLK384_L	–	16.9344	–	MHz	FSEL=L : XTAL×147/40/8

The following is guaranteed by design

Duty	Duty	45	50	55	%	Measured at 1/2 V _{DD}
Jitter 1	Jstd1	–	50	–	psec	Jitter 1 sigma (Maximum load)
Jitter 2	Jstd2	–	300	–	psec	MIN-MAX level (Maximum load)
Rise time	t _r	–	2.5	–	nsec	Time between 0.2V _{DD} to 0.8V _{DD}
Fall time	t _f	–	2.5	–	nsec	Time between 0.8V _{DD} to 0.2V _{DD}
Output Lock time	t _{Lock}	–	–	1	msec	*1
S / N 54M	S / N 54M	65	80	–	dB	Maximum load *2
S / N 33M	S / N 33M	50	60	–	dB	Maximum load *2

Note) When input frequency is 36.864MHz, output frequency is above rated value.

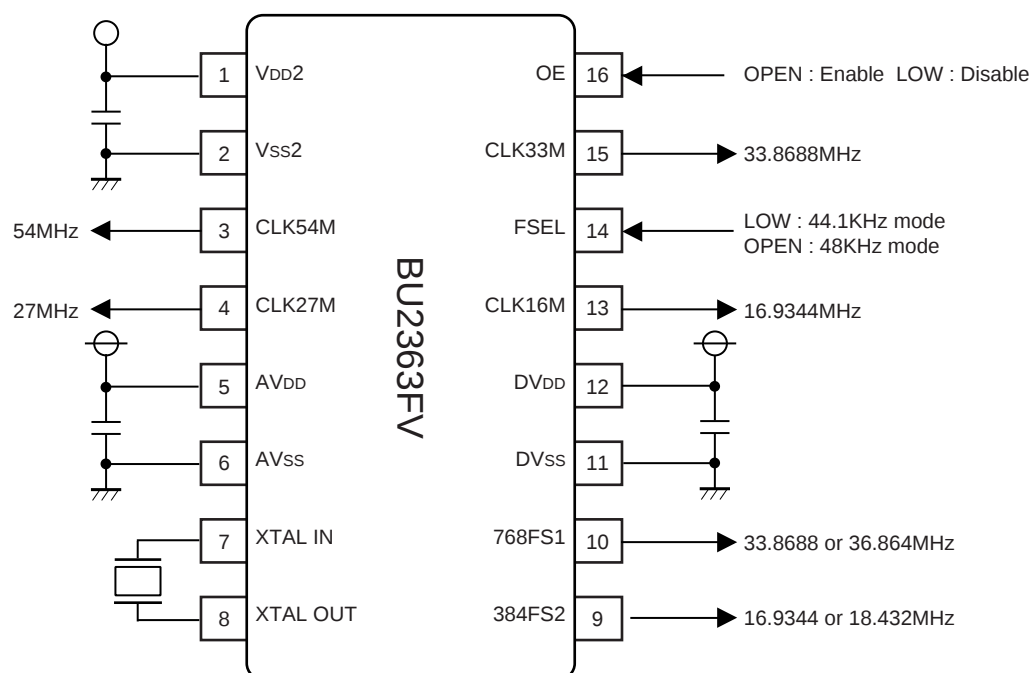
Jitter is mean value when using Time Interval Analyzer with 10,000 sampling.

*1 Time between voltage supply leads to 3.0V and output clock gets stable.

*2 Measuring condition is as following SPAN : 100kHz, RBW : 1kHz VBW : 100Hz.

Measuring point is the middle point of noise. (27MHz±20KHz) (33.8688MHz±20KHz)

●Application example



Note) The BU2363FV is basically placed on the board.

Decoupling capacitor (0.1μF) needs to be placed between Pin1 (VDD2) and Pin2 (VSS2), Pin5 (AVDD) and Pin6 (AVSS), Pin11 (DVSS) and Pin12 (DVDD).

Decoupling capacitor also needs to be placed as near to BU2363FV as possible.

To obtain accurate frequency, capacitor (–pF) needs to be placed between Pin8 (XTAL IN) and Pin6 (AVSS), Pin7 (XTAL OUT) and Pin6 (AVSS).

Electrolytic capacitor needs to be placed between VDD and GND according to the condition of the board.

Ferrite beads needs to be placed on beginning point of VDD against EMI.

Moreover, selected bypass capacitor ($\leq 1\Omega$ at problem high frequency) may need to be placed between VDD and GND.