Clock generator for DVD

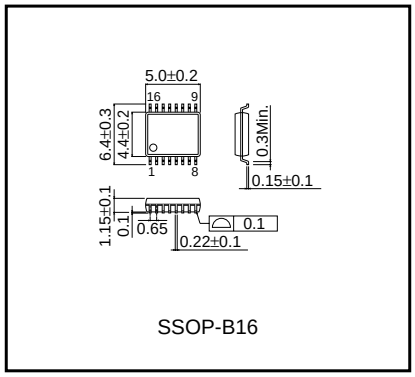
BU2362FV

BU2362FV is a high-performance 2-channel PLL integrated Circuit. PLL circuit generates necessary clocks by inputting standard clocks of crystal oscillator from outside. Frequency can be changed by the internal dividing control.

●Applications

DVD-P, DVD-R, DVD-R/W, DVC
DVD car navigation (Expanded operating temperature range for car navigation : (-25°C to 85°C)
DVD camcoder (Low power operation (3.0V±0.3V) for portable appliances)

●External dimensions (Unit : mm)



SSOP-B16

●Features

1) Generate Sound clock (44.1k, 48k) from basic video clock
2) No external element required for PLL
3) 3.3V single power supply (2.7V~3.6V operation)
4) -25°C~85°C operation
5) SSOP-B16 package

●Absolute maximum ratings (Ta=25°C)

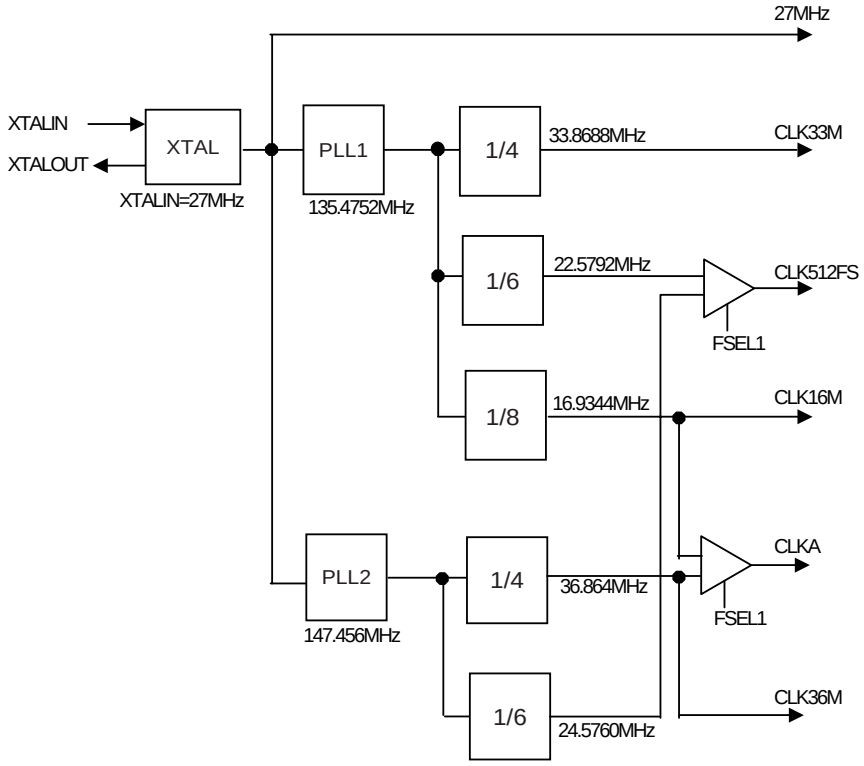
Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{DD}+0.5	V
Storage temperature range	Tstg	−30 to +125	°C
Power dissipation	Pd	450	mW

∗An operation is not guaranteed.
∗In case it is used at Ta=25°C or more, 4.5mW is reduced at every 1°C.
∗Radiation resistance design is not used.
∗Power dissipation is measured when BU2362FV is placed on the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.7	–	3.6	V
Input "H" voltage range	V_{IH}	0.8V_{DD}	–	V_{DD}	V
Input "L" voltage range	V_{IL}	0	–	0.2V_{DD}	V
Operating temperature range	Topr	−25	–	+85	°C
Output maximum load	C_L	–	–	15	pF

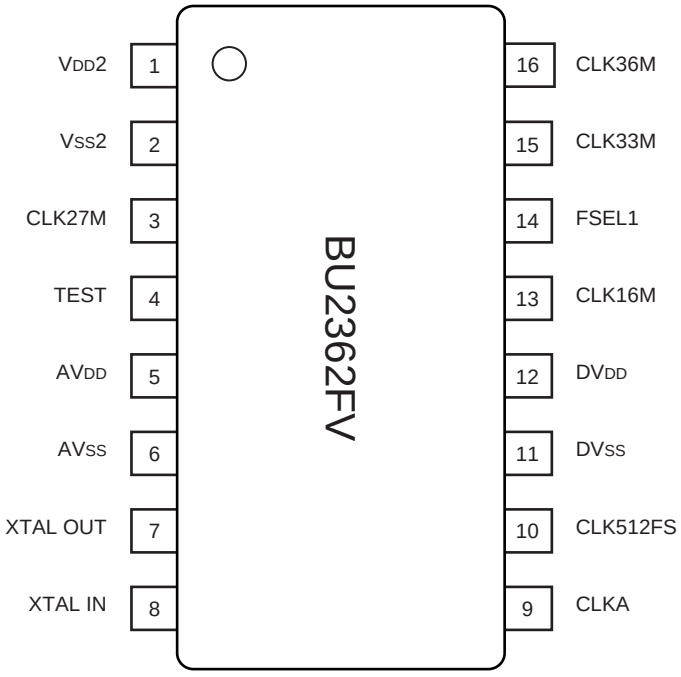
●**Block diagram**



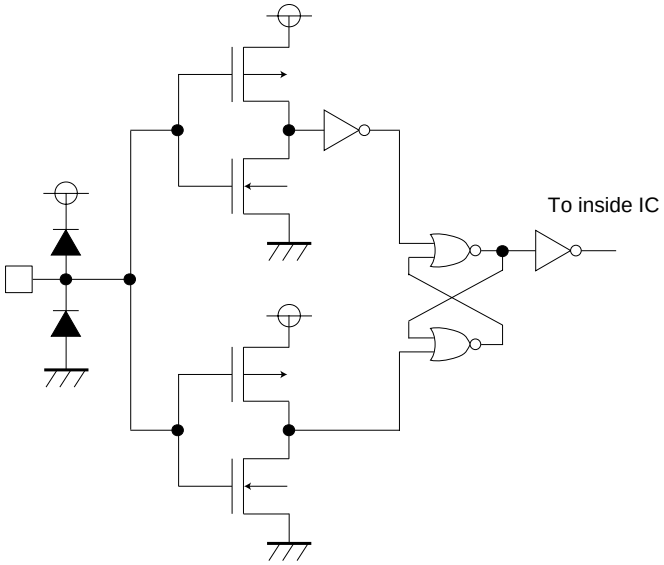
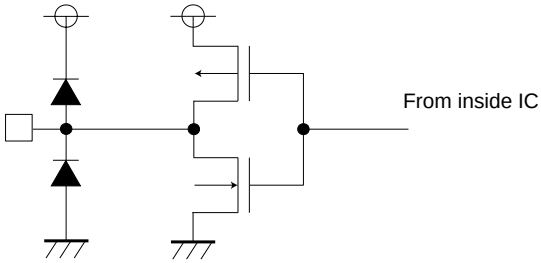
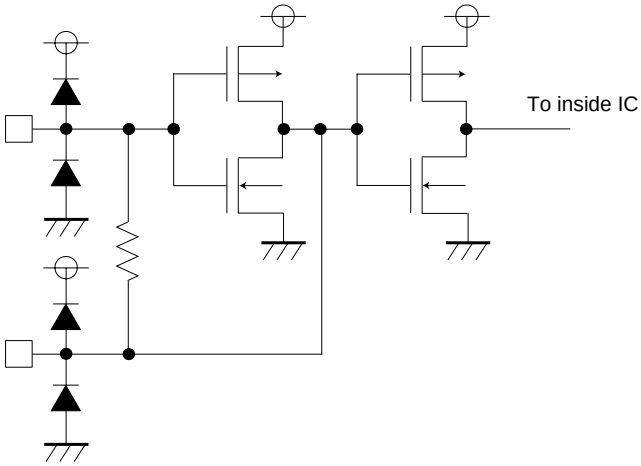
FSEL1	CLK512FS	CLKA
OPEN	22.5792MHz	16.9344MHz
L	24.5760MHz	36.8640MHz

●**Pin descriptions**

Pin No.	Pin name	Functions
1	$V_{DD}2$	V_{DD} for CLK27M, CLK36M
2	$V_{SS}2$	CLK27M. V_{DD} for CLK36M
3	CLK27M	27MHz clock output
4	TEST	Input for test with pull-down Normally, use by open or the 'L' fix.
5	AV_{DD}	Analog V_{DD}
6	AV_{SS}	Analog GND
7	$XTAL_{OUT}$	Standard crystal output
8	$XTAL_{IN}$	Standard crystal input
9	CLKA	16.9344MHz/ 36.8640MHz switch clock output
10	CLK512FS	22.5792MHz/ 24.5760MHz switch clock output
11	DV_{SS}	Digital GND
12	DV_{DD}	Digital V_{DD}
13	CLK16M	16.9344MHz clock output
14	FSEL1	CLKA, CLK512FS output select pin with pull-up
15	CLK33M	33.8688MHz clock output
16	CLK36M	36.8640MHz clock output



●**Input output circuits**

Pin No.	Equivalent circuit
Input Pin 4, 14 (Pin14: with pull-up resistance. Pin4 : with pull-down resistance.)	
Output Pin 3, 9, 10, 13, 15, 16	
Crystal Pin 7, 8	

●**Electrical characteristics** (Unless specified otherwise Ta=25°C, VDD=3.3V, crystal frequency=27MHz)

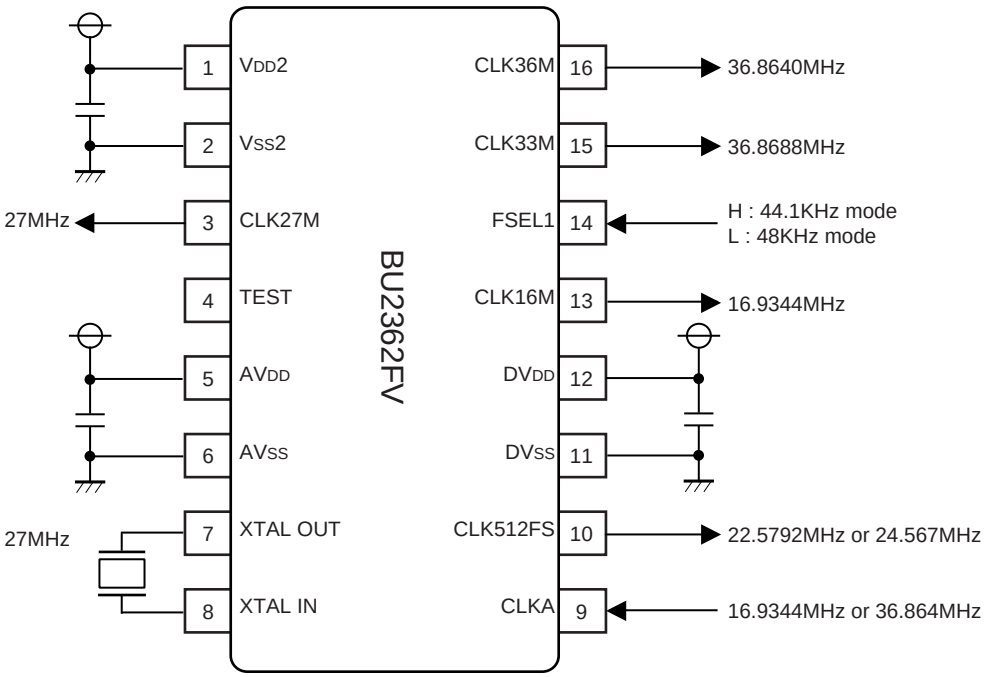
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	V_{OH}	2.4	–	–	V	I_{OH}=4.0mA
Output L voltage	V_{OL}	–	–	0.4	V	I_{OL}=4.0mA
Power supply current	I_{DD}	–	35	45	mA	No load
CLK512FS	CLK512-A	–	22.5792	–	MHz	FSEL 1=OPEN, XTAL ∗ 3136/625/6
	CLK512-B	–	24.5760	–	MHz	FSEL 1=L, XTAL ∗ 2048/375/6
CLKA	CLKA-A	–	16.9344	–	MHz	FSEL 1=OPEN, XTAL ∗ 3136/625/8
	CLKA-B	–	36.8640	–	MHz	FSEL 1=L, XTAL ∗ 2048/375/8
CLK36M	CLK36M	–	36.8640	–	MHz	XTAL ∗ 2048/375/4
CLK33M	CLK33M	–	33.8688	–	MHz	XTAL ∗ 3136/625/4
CLK16M	CLK16M	–	16.9344	–	MHz	XTAL ∗ 3136/625/8
CLK27M	CLK27M	–	27.0000	–	MHz	XTAL

The following is guaranteed by design.

Duty	Duty	45	50	55	%	Measured at 1/2 V_{DD}
Jitter 1σ	JsSD	–	70	–	psec	Jitter 1 sigma
Jitter MIN-MAX	JsABS	–	420	–	psec	MIN-MAX level
Rise time	tr	–	2.5	–	nsec	Time between 0.2V_{DD} to 0.8V_{DD}
Fall time	tf	–	2.5	–	nsec	Time between 0.8V_{DD} to 0.2V_{DD}
Output Lock time	tlock	–	–	1	msec	∗

Jitter is mean value when using Time Analyzer with 10,000 sampling.
∗ Time between voltage supply leads to 3.0V and output clock gets stable.
Whatever rising the power supply does, output locks at above time.

●**Application example**



Note) The BU2362FV is basically placed on the board.
Decoupling capacitance (0.1μF) need to be placed between Pin5 (AV_{DD}) and Pin6 (AV_{SS}).
Also decoupling capacitance (0.1μF) need to be placed between Pin1 ($V_{DD}2$) and Pin6 ($V_{SS}2$), Pin (DV_{SS}) and Pin12 (DV_{DD}).
To obtain accurate frequency, capacitance (pF) need to be placed between Pin8 (XTAL IN) and Pin6 (AV_{SS}). Pin7 (XTAL OUT) and Pin6 (AV_{SS}).
Tantalum capacitance (10 to 100μF), ferrite beads may need to be placed to prevent power supply drop in certain boards case.
To reduce high frequency noise, selected bypass capacitors (≤1Ω at problem high frequency) maybe used for power pin as close to BU2362FV as possible.