

Picture cell driver for STN (LCD driver) for low voltage power supplies

BU9718KV

The BU9718KV is a driver IC designed for the character-type STN liquid crystal panels which ideal for applications such as portable devices. The number of display segments includes 32 output segments and 3 common outputs, enabling drive of up to 96 segments. A compact 48-pin QFP package with a pitch of 0.5mm is used, enabling compact size for the set as a whole.

●Applications

Portable terminals (POS, ECR, PDA, and others), movie projectors, cameras, telephones (cordless hand held telephone units), and others Los-voltage power supply sets.

●Features

- 1) Operates on 3V power supply.
- 2) Low current dissipation. (0.1μA in low power mode (actual value))
- 3) Compact package. (molded section is 7.0mm²)
- 4) Up to 32 segment output pins and 3 common output pins are provided, enabling a total display of up to 96 segments.
- 5) 1/3 duty display.
- 6) Either 1/2 or 1/3 bias can be selected for power supply for LCD display.

●Absolute maximum ratings (Ta=25°C, V_{SS}=0V)

Parameter	Symbol	Pin	Limits	Unit
Power supply voltage ^{*1}	V _{DD}	V _{DD}	-0.3 to +7.0	V
Input voltage ^{*1}	V _{IN}	OSC, CS, CK, DI, RES	-0.3 to V _{DD} +0.3	V
Output voltage ^{*1}	V _{OUT}	OSC	-0.3 to V _{DD} +0.3	V
Output current	I _{SO}	S ₁ ~ S ₃₂	300	μA
	I _{CO}	COM ₁ ~ COM ₃	3	mA
Power dissipation	P _d	—	400 ^{*2}	mW
Storage temperature	T _{stg}	—	-55 to +125	°C

^{*1} Max. voltage that can be applide with a V_{SS} pin

^{*2} Reduced by 4.0mW for each increase in Ta=1°C over 25°C.

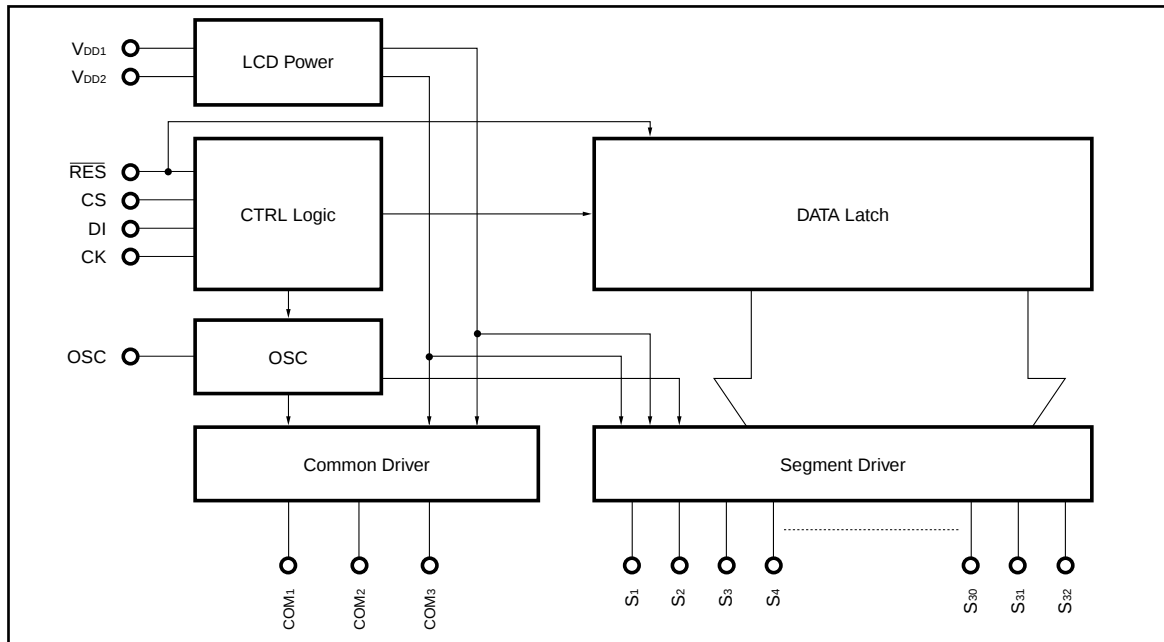
●Recommended operating conditions (Ta=25°C, V_{SS}=0V)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit
Power supply voltage [*]	V _{DD}	V _{DD}	2.7	—	3.5	V
Input voltage [*]	V _{DD1}	V _{DD1}	0	2/3 V _{DD}	V _{DD}	V
	V _{DD2}	V _{DD2}	0	1/3 V _{DD}	V _{DD}	V
Oscillation freq., with external input	f _{OSC}	OSC	—	38	100	kHz
External resistance	R	OSC	—	47	—	kΩ
External capacitance	C	OSC	—	1000	—	pF
Operating temperature	T _{opr}	—	-40	—	85	°C

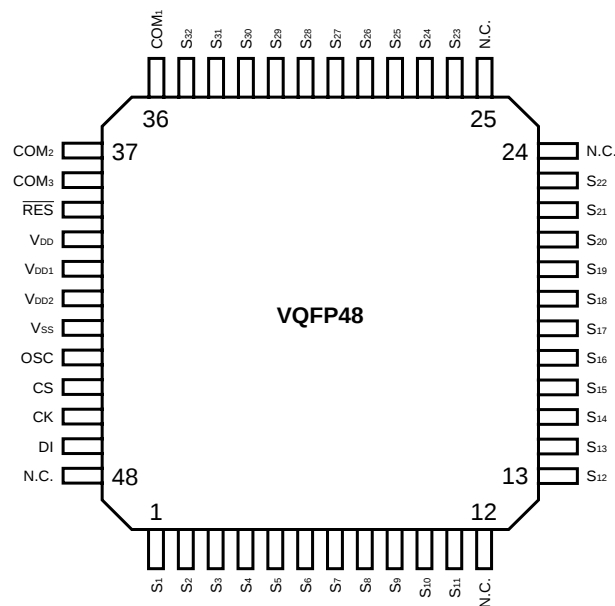
^{*} Indicates the max. voltage that can be applied with a V_{SS} pin.

Display Driver ICs

●Block diagram



●Pin assignments



Display Driver ICs

●Pin descriptions

Pin No.	Pin name	I/O	Function	Processing when not in use
1 – 11 13 – 23 26 – 35	S ₁ – S ₁₁ S ₁₂ – S ₂₂ S ₂₃ – S ₃₂	O	Segment data output pin; outputs LCD drive voltage that matches CMOS ₁ – CMOS ₃ compatible data	OPEN
36 37 38	COM ₁ COM ₂ COM ₃	O	Common drive output; frame freq. $f_c = (f_{osc} / 384)$ Hz	V _{SS}
39	$\overline{RES}$	I	Reset input; when $\overline{RES}=L$, resets internal data (include. control data)	V _{DD}
44	OSC	—	Oscillation pin (for common, segment alternation waves)	V _{SS}
45	CS	I	Chip segment input; when CS=H, data can be transferred	V _{SS}
46	CK	I	Synchronous clock input for serial data transfer	V _{SS}
47	DI	I	Serial data input	V _{SS}
41	V _{DD1}	—	internal standard voltage for liquid-crystal drive; when using 1/2 bias mode, connects to V _{DD2}	OPEN
42	V _{DD2}	—	Internal standard voltage for liquid-crystal drive; when using 1/2 bias mode, connects to V _{DD1}	OPEN

●Electrical characteristics (Unless otherwise noted, Ta=25°C, V_{DD}=2.7V to 3.5V, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Input high level voltage	V _{IH}	0.8 V _{DD}	—	V _{DD}	V	—	CS, CK, DI, $\overline{RES}$
Input low level voltage	V _{IL}	0	—	0.2 V _{DD}	V	—	CS, CK, DI, $\overline{RES}$
Input high level current	I _{IH}	0	—	6.0	μA	V _I =V _{DD}	CS, CK, DI, $\overline{RES}$
Input low level current	I _{IL}	0	—	6.0	μA	V _I =V _{SS}	CS, CK, DI, $\overline{RES}$
Output high level voltage	V _{SOH}	—	V _{DD} -1.0	—	V	I _O =-20μA	S ₁ ~ S ₃₂
	V _{COH}	—	V _{DD} -1.0	—	V	I _O =-100μA	COM ₁ ~ COM ₃
Output low level voltage	V _{SOL}	—	1.0	—	V	I _O =20μA	S ₁ ~ S ₃₂
	V _{COL}	—	1.0	—	V	I _O =100μA	COM ₁ ~ COM ₃
Output medium level voltage	V _{CM1}	—	$\frac{1}{2} V_{DD} \pm 1.0$	—	V	1/2bias	COM ₁ ~ COM ₃
	V _{SM1}	—	$\frac{2}{3} V_{DD} \pm 1.0$	—	V	1/3bias	S ₁ ~ S ₃₂
	V _{CM2}	—	$\frac{2}{3} V_{DD} \pm 1.0$	—	V	1/3bias	COM ₁ ~ COM ₃
	V _{SM2}	—	$\frac{1}{3} V_{DD} \pm 1.0$	—	V	1/3bias	S ₁ ~ S ₃₂
	V _{CM3}	—	$\frac{1}{3} V_{DD} \pm 1.0$	—	V	1/3bias	COM ₁ ~ COM ₃
Power supply current	I _Q	—	0.1	30	μA	Low-power mode	—
	I _{DD}	—	100	300	μA	f _{osc} =38kHz	—

Display Driver ICs

●AC characteristics (Unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$ to 3.5V , $V_{SS} = 0\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Guaranteed oscillation range	f_{osc}	10	38	80	kHz	$C=1000\text{pF}$ $R=47\text{k}\Omega$	OSC
Operating frequency	f_{osc}	—	—	100	kHz	External input	OSC
Data set-up time	t_{DS}	200	—	—	ns	—	CK, DI
Data hold time	t_{DH}	200	—	—	ns	—	CK, DI
CS set-up time	t_{CS}	200	—	—	ns	—	CS, CK
CS hole time	t_{CH}	200	—	—	ns	—	CS, CK
CK "H" level pulse width	t_{CKH}	200	—	—	ns	—	CK
CK "L" level pulse width	t_{CKL}	200	—	—	ns	—	CK
Rise time	t_r	—	—	100	ns	—	CS, CK, DI
Fall time	t_f	—	—	100	ns	—	CS, CK, DI

AC timing waveform

(1) When CK is stopped at "L"

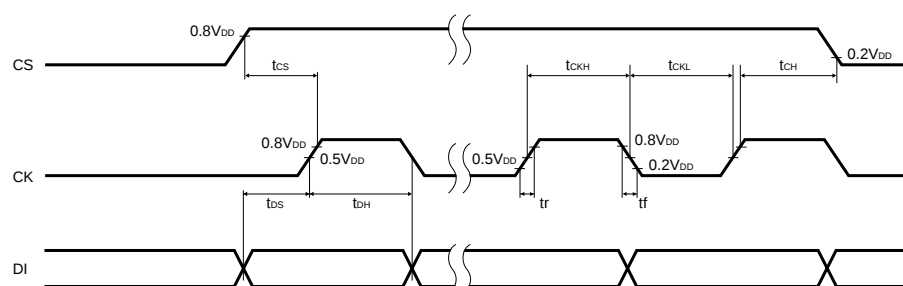


Fig.1

(2) When CK is stopped at "H"

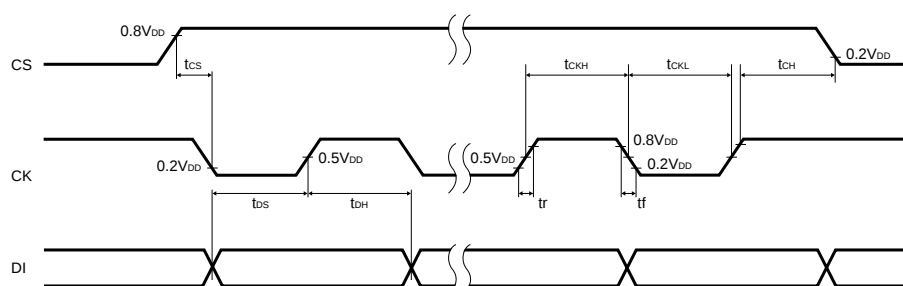


Fig.2

Display Driver ICs

Timing charts

(1) When CK is stopped at "L"

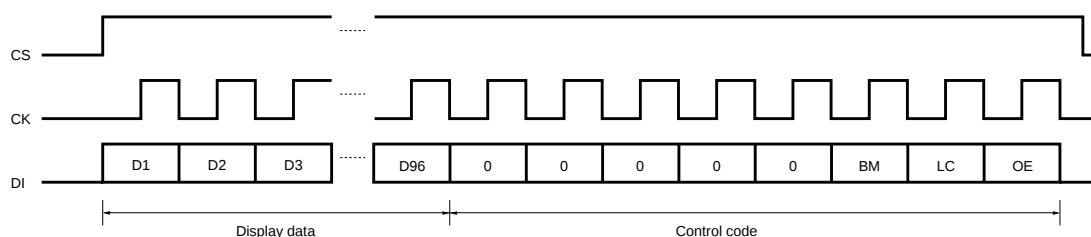


Fig.3

When CS is HIGH, data can be transferred. Data is sent to the shift register at the rising edge of CK. After all the DI data has been transferred, CS should be set to LOW. The voltage corresponding to the display transferred at the falling edge of CS is output.

(2) When CK is stopped at "H"

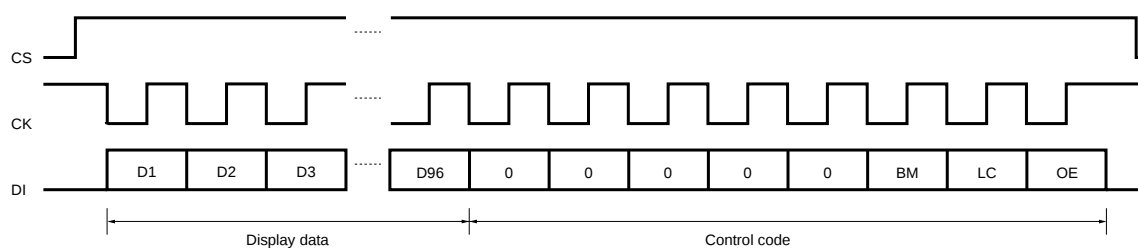


Fig.4

Control code table

OE	Output enable control
0	Normal operation
1	No display; all display data=0(internal oscillation circuit is operating)
LC	Low-poert mode control
0	Normal operation
1	Loe-power mode=internal oscillation circuit has stopped; segment and common output=0
BM	Bias mode control
0	1/3 bias
1	1/2 bias

Display Driver ICs

Correspondence between display data input and segments

Segment	COM3	COM2	COM1
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96

Display Driver ICs

●Output waveforms

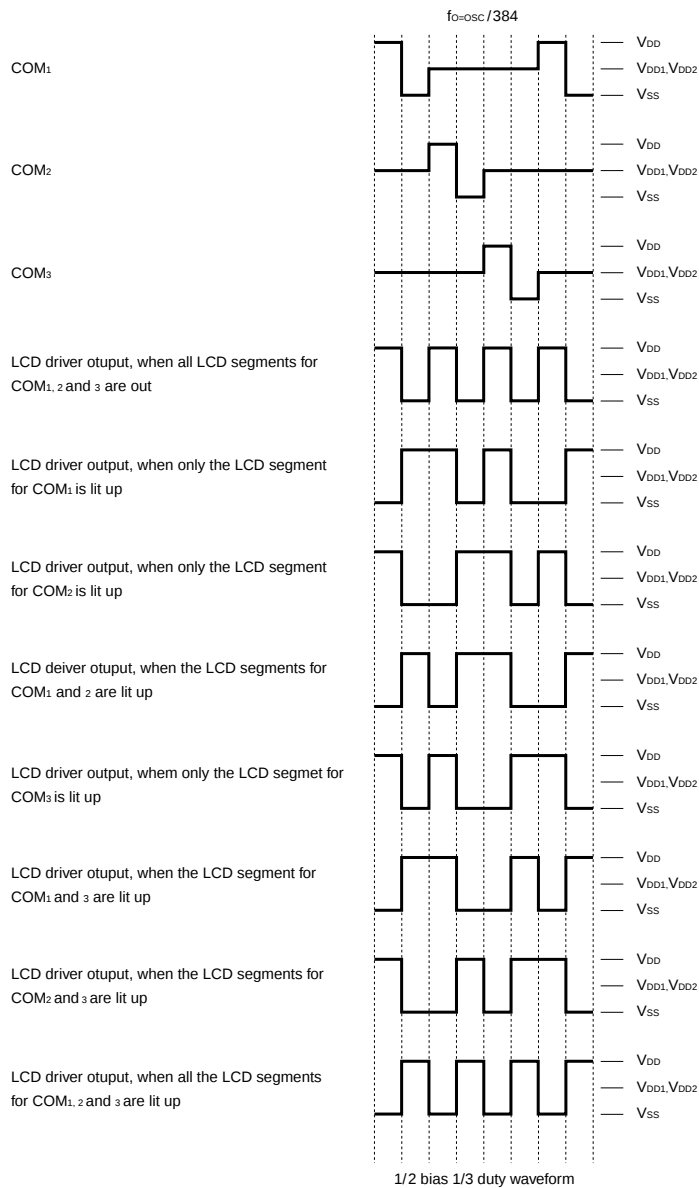


Fig.5

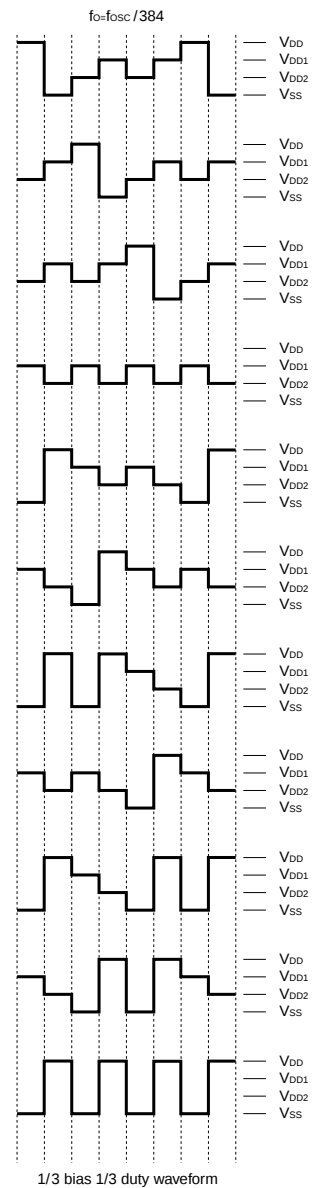
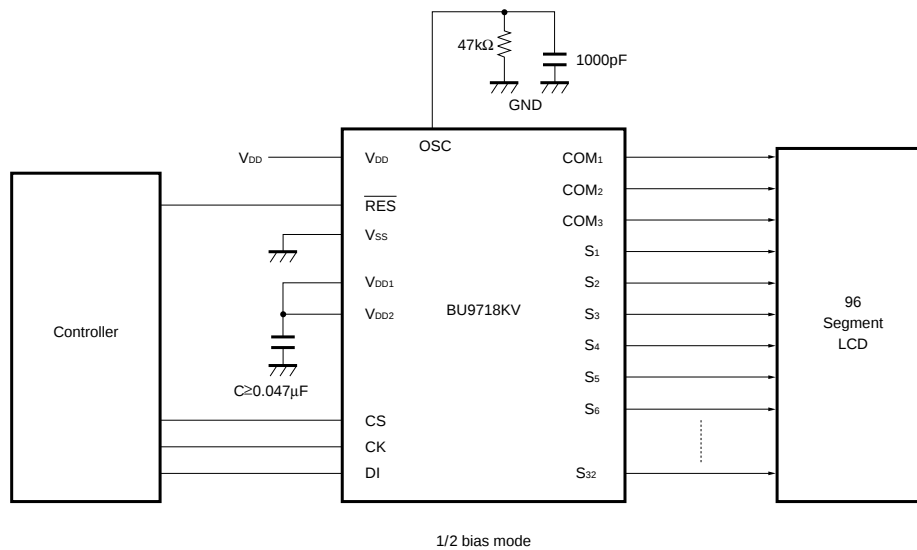


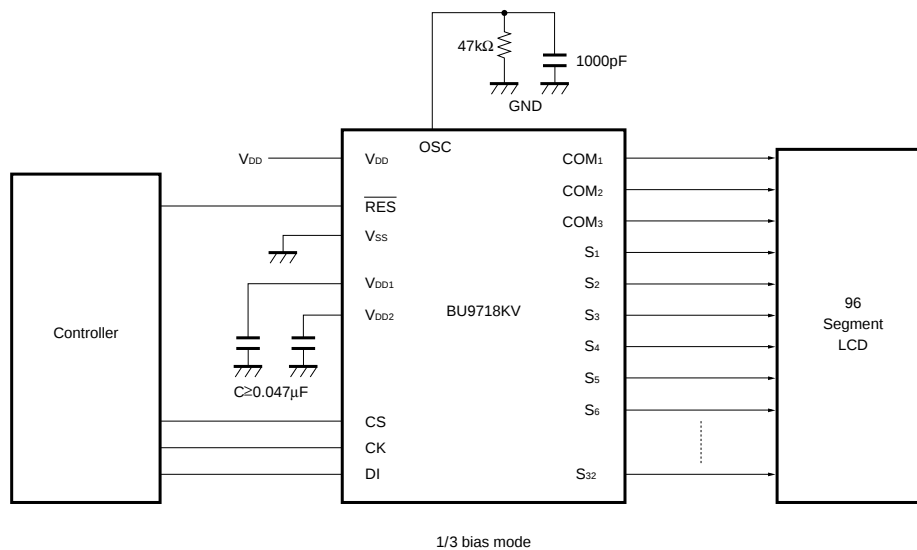
Fig.6

●Application example 1



1/2 bias mode

Fig.7



1/3 bias mode

Fig.8

Display Driver ICs

●Application example 2

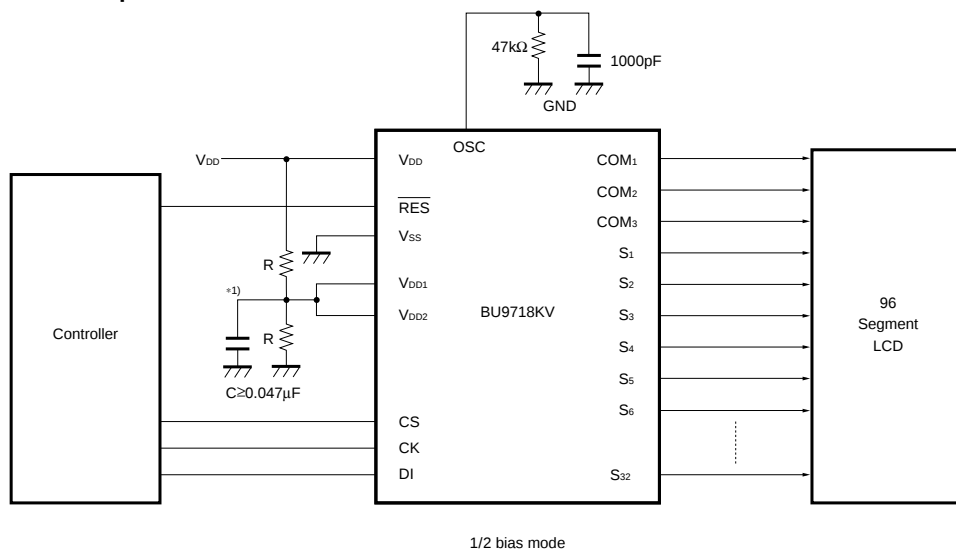


Fig.9

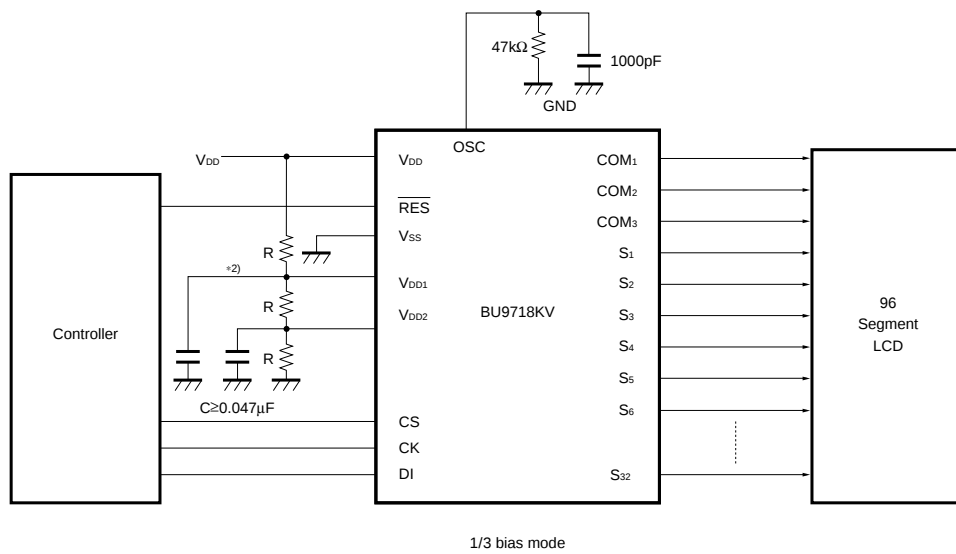


Fig.10

Note: The resistance values and capacitance for *1 and *2 should be set to match the LCD panel, and should be checked sing test operation.

- When using the external reset terminal, make $\overline{\text{RST}} = \text{"L"}$ at 1 ms or more with V_{DD} at 2.7V or more.
- When not using the external reset terminal, V_{DD} has to satisfy the following conditions.

