Device Datasheet
Version 1.0 - July 2001

Utopia Level 3 to Level 2

Slave/Slave Bridge

Datasheet

CONTENTS

1 Introduction

1.1 Utopia Overview

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (segmentation and Re-assembly) devices.

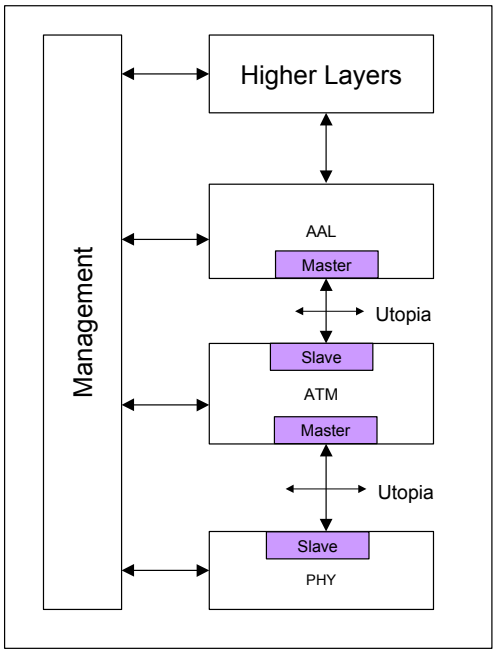

Figure 1: Utopia Reference Model

The Utopia Standard defines a full duplex bus interface with a Master/Slave paradigm. The Slave interface responds to the requests from the Master. The Master performs PHY arbitration and initiates data transfers to and from the Slave device.

The ATM forum has standardized the Utopia Levels 1 (L1) to 3 (L3). Each level extends the maximum supported interface speed from OC3, 155Mbps (L1) over OC12, 622Mbps (L2) to 3.2Gbit/s (L3).

The following Table 1 gives an overview of the main differences in these three levels.

Table 1: Utopia Level Differences

Utopia Level	Interface Width	Max. Interface Speed	Theoretic (typical) Throughput
1	8 bit	25 MHz	200Mbps (typ. OC3 155Mbps)
2	8 bit, 16 bit	50 MHz	800Mbps (typ. OC12 622MBps)
3	8 bit, 32 bit	104MHz	3.2Gbps (typ. OC 48 2.5GBps)

Utopia Level 1 implements an 8-bit interface running at up to 25MHz. Level 2 adds a 16 Bit interface and increases the speed to 50MHz. Level 3 extends the interface further by a 32 Bit word-size and speeds up to 104MHz providing rates up to 3.2 Gbit/s over the interface.

In addition to the differences in throughput, Utopia Level 2 uses a shared bus offering to physically share a single interface bus between one master and up to 31 slave devices (Multi-PHY or MPHY operation). This allows the implementation of aggregation units that multiplex several slave devices to a single Master device. The Level 1 and Level 3 are point-to-point only, whereas Level 1 has no notion of multiple slaves. Level 3 still has the notion of multiple slaves, but they must be implemented in a single physical device connected to the Utopia Interface.

2 Utopia Slave/Slave Bridge Application

As it is not possible to connect two Master devices together, the Slave/Slave Bridge provides the necessary interfaces to convey between two Master devices as shown in Figure 2.

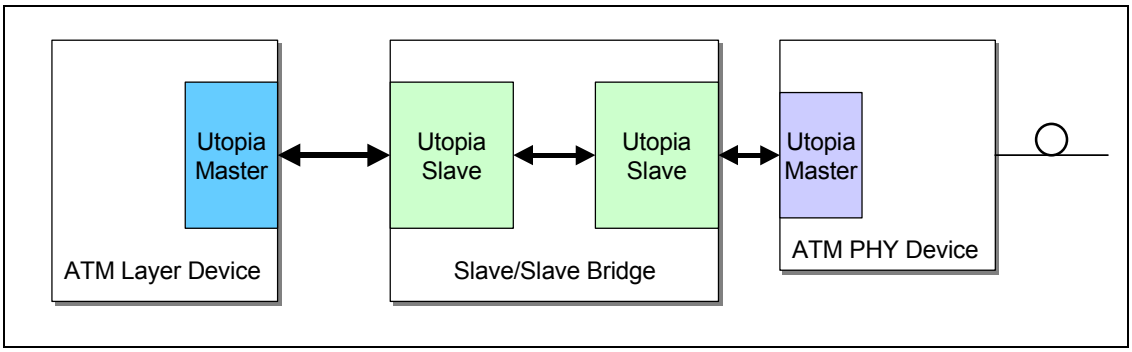

Figure 2: Utopia Slave Bridge

The Bridge automatically transfers data as soon as it becomes available from one side to the other. Internal asynchronous FIFOs enable independent clock domains for each interface.

3 Utopia Level 3 to Level 2 Slave Bridge Core Features

- Implements one Utopia Level 3 Slave and one Utopia Level 2 Slave providing a solution to bridge Utopia Master devices of differing Levels
- Compliant with ATM-Forum af-phy-0039.000 (L2) and af-phy-0136.000 (L3) specification
- Single chip solution for improved system integration
- Supports 16 Bit busses on both interfaces, single PHY
- Support for cell level transfer mode
- Cell and clock rate decoupling with on chip FIFOs
- Meets 104MHz performance on Level 3 interface and 50MHz performance on Level 2 interface offering up to 800Mbps cell rate transfers
- Up to 1.5 KByte of on chip FIFO per data direction
- Integrated management interface and built-in errored cell discard
- ATM Cell size programmable via external pins from 16 to 128 bytes
- Optional Utopia parity generation/checking enable/disable via external pin
- Built in JTAG port (IEEE1149 compliant)
- Simulation model available for system level verification (Contact Quicklogic or MorethanIP for details)
- Solution also available as flexible Soft-IP core, delivered with a full device modelization and verification testbenches.

4 Application

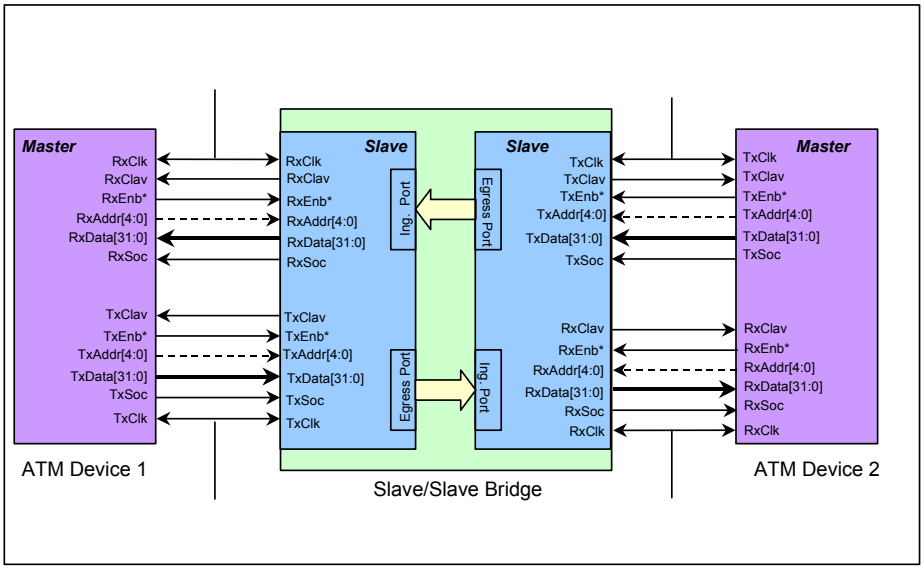

Figure 3: Slave/Slave Bridge connecting two Master Devices

Data flows from the Bridge's TX Ports to the corresponding RX Ports on the other side of the bridge.

5 Core Pinout

On the Utopia interfaces, the Core implements all the required Utopia signals and provides all the Utopia optional signals (Indicated by an 'O' in the following tables). The optional Utopia signals are activated during the Core configuration and inactive Utopia signals should be left unconnected (Outputs) or tied to a zero logic level (inputs) as specified in the following Tables.

In addition to the Utopia Interface signals, error indication signals are available for error monitoring or statistics. An error indication always shows that a cell has been discarded by the bridge. Possible errors are parity or cell-length errors on the receive interface of the corresponding Utopia Interfaces.

All Utopia interfaces work in the same transfer mode (cell level). A mix is not possible.

To identify the sides of the core the notion "WEST" and "EAST" for the corresponding interfaces will be used.

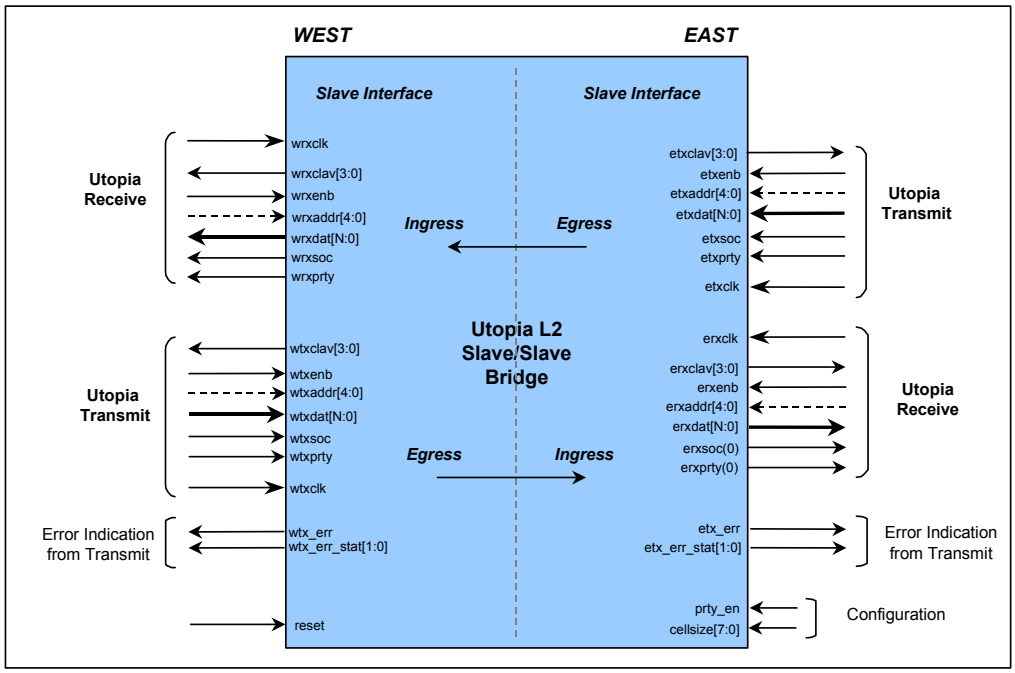

Figure 4: Utopia Level 3 Slave/Slave Bridge Top Entity

5.1 Signal descriptions

Table 2: Global Signal

Pin	Mode	Description
reset	In	Active high chip reset.

Table 3: Device Management Interface

Pin	Mode	Description
wtx_err	Out	Transmit error indication on west interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the west interface and is discarded.
wtx_err_stat(1:0)	Out	Transmit error status information for west interface. When wtx_err is driven, indicates the error status of the discarded cell: • wtx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • wtx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of `ut_tx_soc` on the Utopia interface within less than a complete cell time).
etx_err	Out	Transmit error indication on east interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the east interface side.
etx_err_stat(1:0)	Out	Transmit error status information for east receive interface. When etx_err is driven, indicates the error status of the discarded cell: • etx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • etx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of `ut_tx_soc` on the Utopia interface within less than a complete cell time).

Note: wtx_.. signals are sampled with west transmit clock (wtxclk). etx_.. signals are sampled with west receive clock (wrxclk).

Table 4: West Utopia Level 3 Slave Transmit Interface

Pin	Mode	Description
wtxclk	In	104MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
wtxdata[N:0]	In	Transmit data bus. The width of the data bus can be 8 or 16 bit. Bit N is the MSB.

wtxprty	In	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be tied to '0'.
wtxsoc	In	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
wtxenb	In	Active low transmit data transfer enable.
wtxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
wtxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wtxaddr[4:0]	In	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Note: (O) indicates optional signals.

Table 5: West Utopia Level 3 Slave Receive Interface

Pin	Mode	Description
wrxclk	In	104MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
wrxdata[N:0]	Out	Receive data bus. The width of the data bus can be 8,16 or 32 bit. Bit N is the MSB.
wrxprty (O)	Out	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
wrxsoc	Out	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
wrxenb	In	Active low transmit data transfer enable.
wrxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
wrxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals

		is limited to four.
wrxaddr(4:0)	In	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 6: East Utopia Level 2 Slave Transmit Interface

Pin	Mode	Description
etxclk	In	50MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
etxdata[N:0]	In	Transmit data bus. The width of the data bus is user programmable and can be set to 8 or 16 or 32 bit. Bit N is the MSB.
etxprty	In	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
etxsoc	In	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
etxenb	In	Active low transmit data transfer enable.
etxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
etxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
etxaddr[4:0]	In	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Note: (O) indicates optional signals.

Table 7: East Utopia Level 2 Slave Receive Interface

Pin	Mode	Description
erxclk	In	50MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.

erxdata[N:0]	Out	Receive data bus. The width of the data bus can be 8,16 or 32 bit. Bit N is the MSB.
erxprty (O)	Out	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
erxsoc	Out	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
erxenb	In	Active low transmit data transfer enable.
erxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
rxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
erxaddr(4:0)	In	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. taddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 8: Device Configuration Pins

Pin	Mode	Description
prty_en	In	Enable parity checking on the Utopia interface. If disabled (tied to 0), the wrx_err_stat(0) signal can be ignored and left open and the rx parity input should be tied to 0. Also the tx parity pins can be left open.
cellsize[7:0]	In	Define cellsize: sets the size in bytes of a cell. Binary value to be set usually by board wiring. For 16 bit implementations the size must be a multiple of 2 and cellsize[0] becomes a "not connected" and should be left open.

The configuration pins are not intended for change during operation. They are usually board wired to configure the device for operation.

6 Global Signal Distribution

The externally provided Utopia Transmit and Receive clocks are connected to global resources to provide low skew and fast chip level distribution. In both data directions, the two corresponding Utopia Interfaces are decoupled by asynchronous FIFOs.

Therefore each interface runs completely independently each at its own *tx* and *rx* clocks which typically are up to 104 MHz on the Level 3 interface (west) and up to 50 MHz on the Level 2 interface (east).

The Error indications of the two receive interfaces are always sampled within the west clock domains. The errors of the east tx (receiving) interface is available on the etx_err signal, which is handled using the west clock domain (wrxclk). The west tx (receiving) error is directly derived from the west tx block (wtxclk).

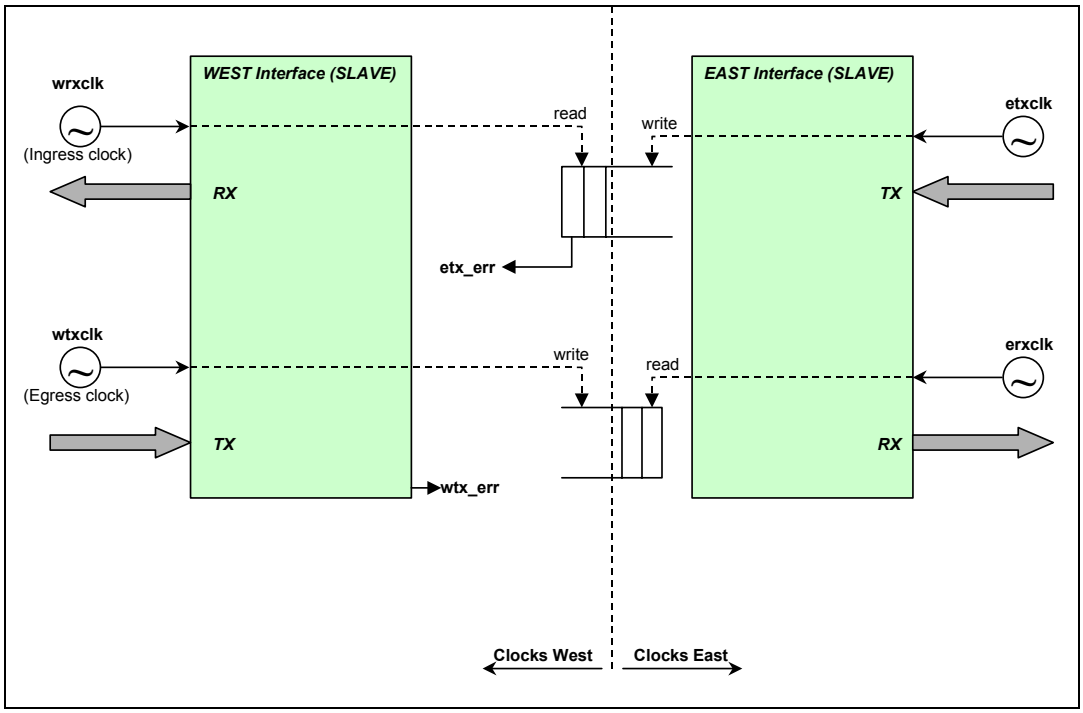

Figure 5: Slave/Slave Bridge Clock Distribution

7 Functional Description – Utopia Interface

The Utopia Bridge operates in single PHY mode. Therefore no address bus and only a single status pin (clav[0]) per direction is used on the interfaces.

7.1 Utopia Level 2 Interface Single PHY Transmit Interface

The Transmit interface is controlled by the Master.

The transmit interface has data flowing in the same direction as the ATM enable `ut_tx_enb`. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the Master to Slave via the following procedure. The Slave indicates it can accept data using the `ut_txclav` signal, then the Master drives data onto `ut_txdat` and asserts `ut_txenb`. The Slave controls the flow of data via the `ut_txclav` signal.

Cell Level Transfer – Single Cell

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Master asserts `ut_txenb` (Low) to indicates that it drives valid data to the Slave **2**. Together with the first octet of a cell, the Master device asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the Master does not cause transmit overrun, the Slave deasserts `ut_txclav` at least 4 cycles before the end of a cell if it cannot accept the immediate transfer of the subsequent cell **4**.

The Master can pause the cell transfer by de-asserting `ut_txenb` **5**. To complete the transfer to the Slave, the Master de-asserts `ut_tx_enb` **6**.

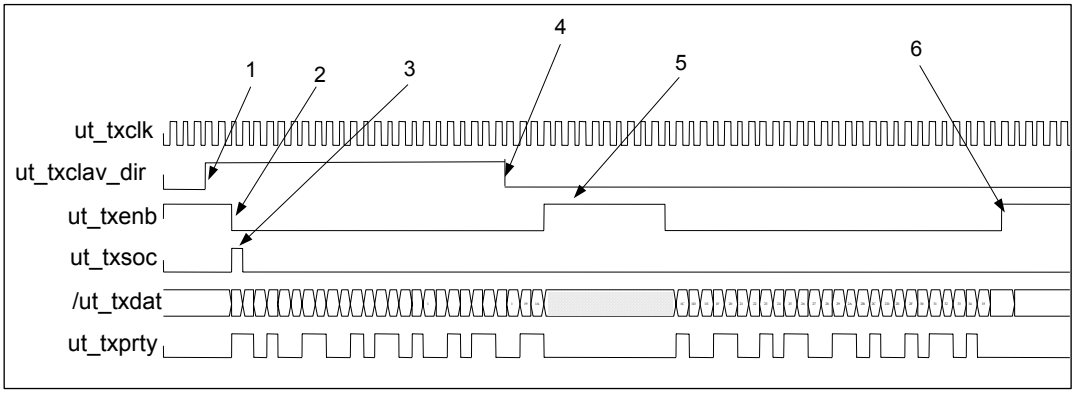

Figure 6: Single Cell Transfer – Cell Level Transfer

Cell Level Transfer – Back to Back Cells

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Master can keep `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last octet of the previous cell **2**.

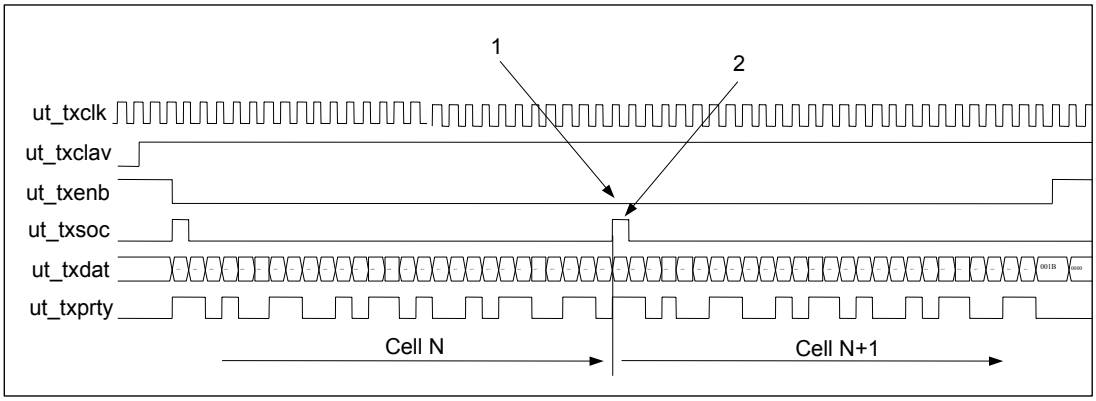

Figure 7: Back to Back Cell Transfer – Cell Level Transfer

7.2 Utopia Level 2 Interface Single PHY Receive Interface

The Receive interface is controlled by the Master. The receive interface has data flowing in the opposite direction to the Master enable `ut_rxenb`.

Receive data is transferred from the Slave to Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Slave indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

Cell Level Transfer – Single Cell

The Slave asserts `ut_rx_clav` when it is ready to send a complete cell to the Master device **1**. The Master interface asserts `ut_rxenb` to start the cell transfer. The Slave samples `ut_rxenb` and starts driving data **2**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **3**.

The Master can pause a transfer by de-asserting `ut_rxenb` **4**. The Slave samples high `ut_rxenb` and stops driving data **5**. To resume the transfer, the Master re-asserts `ut_rxenb` **6**. The Slave samples low `ut_rxenb` and starts driving valid data **7**.

The Master drives `ut_txenb` high one before the expected end of the current cell if the Slave has no more cell to transfer **8**. The Slave de-asserts ut_rxclav to indicate that no new cell is available **9**.

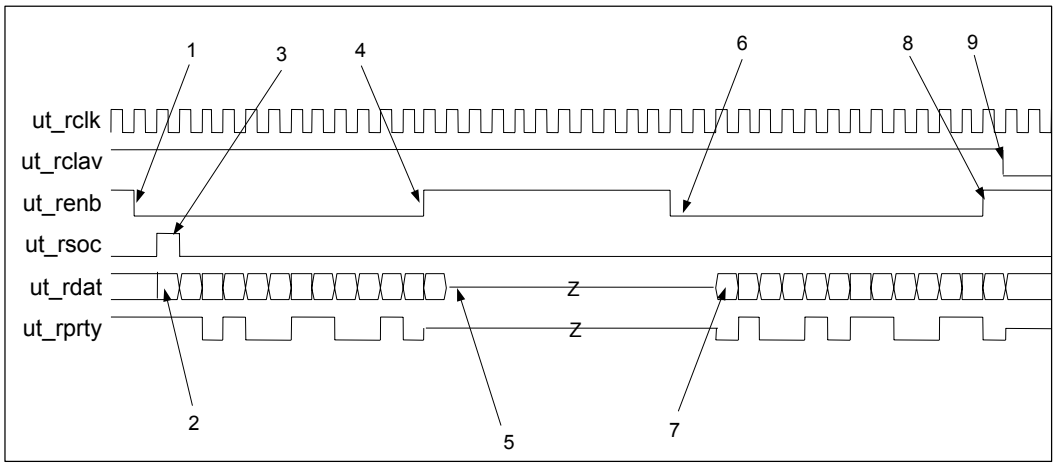

Figure 8: Single Cell Transfer – Cell Level Transfer

Cell Level Transfer – Back to Back Cells

If the Master keeps `ut_rxenb` asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps `ut_rxclav` asserted **2** and immediately drives the new cell asserting `ut_rxsoc` to indicate the start of a new cell **3**.

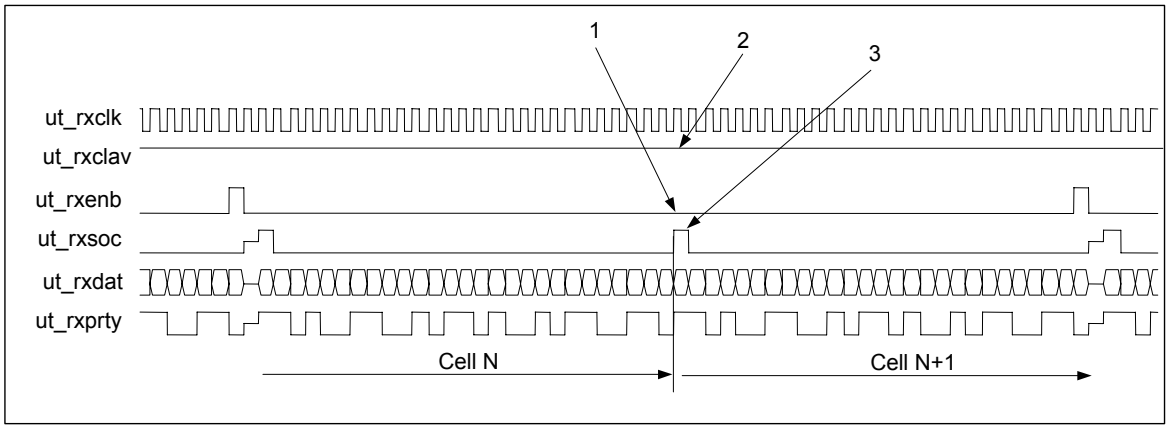

Figure 9: Back to Back Cells Transfer – Cell Level Transfer

Note: If the Master keeps `ut_rxenb` asserted at the end of a packet and if the Slave does not have a new cell available, the Slave de-asserts `ut_rxclav` and the data of the bus `ut_rxdat` are invalid.

7.3 Utopia Level 3 Interface Single PHY Transmit Interface

The Transmit interface is controlled by the Master.

The transmit interface has data flowing in the same direction as the ATM enable `ut_txenb`. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the Master to PHY layer via the following procedure. The Core indicates it can accept data using the `ut_txclav` signal, then the Master drives data onto `ut_txdat` and asserts `ut_txenb`.

Once a cell transfer has started, the Master or the Slave device cannot pause the transfer by any mean.

Single Cell Transfer

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Master asserts `ut_txenb` (Low) to indicate that it drives valid data to the Slave **2**. Together with the first octet of a cell, the Master asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the Master does not cause transmit overrun, the Slave de-asserts `ut_txclav` when `ut_txsoc` is de-asserted by the Master **4**.

When a cell transfer is initiated, the Master or the Slave cannot pause the transfer by any means.

To complete the cell transfer, the Master de-asserts the Utopia enable signal `ut_txenb` **5**.

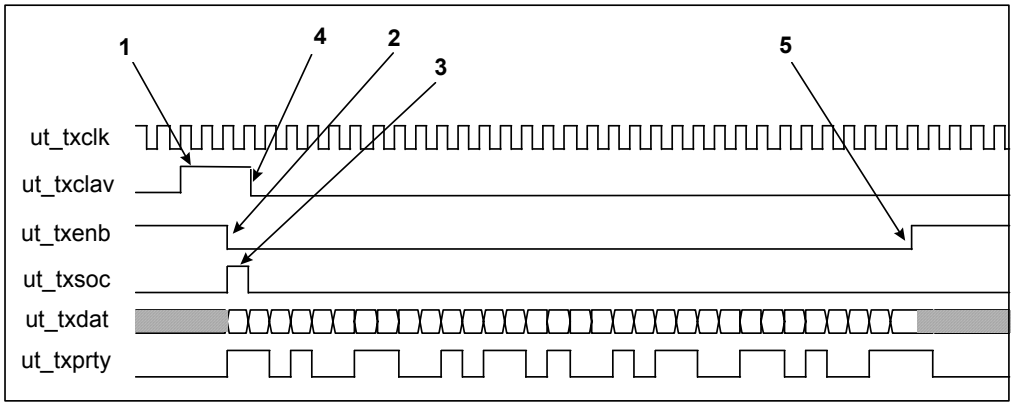

Figure 10: Single Cell Transfer

Back to Back Cells Transfer

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Master can keep `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last octet of the previous cell **2**.

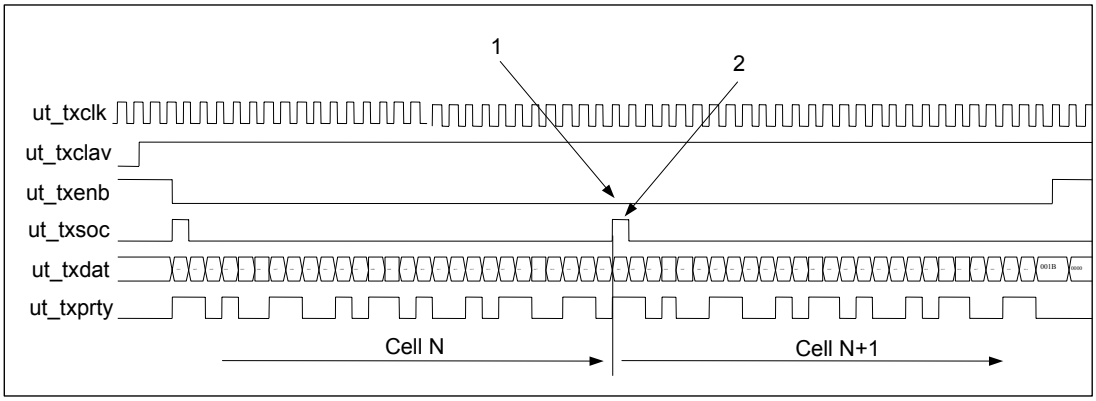

Figure 11: Back to Back Cell Transfer

7.4 Utopia Level 3 Interface Single PHY Receive Interface

The Receive interface is controlled by the Master interface. The receive interface has data flowing in the opposite direction to the Master enable `ut_rxenb`.

Receive data is transferred from the Slave to the Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Slave indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

Single Cell Transfer

The Slave asserts `ut_rxclav` when it is ready to send a complete cell to the Master device **1**. The Master interface asserts `ut_rxenb` to start the cell transfer **2**. The Slave samples `ut_rxenb` and starts driving data on the following clock edge **3**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **4**.

The Master drives `ut_txenb` high two clock cycles before the expected end of the current cell if the Slave has no more cell to transfer **5**. The Slave de-asserts ut_rxclav to indicate that no new cell is available **6** together with the start of cell indication.

When a cell transfer is initiated, the transfer cannot be paused by the Master or the Slave.

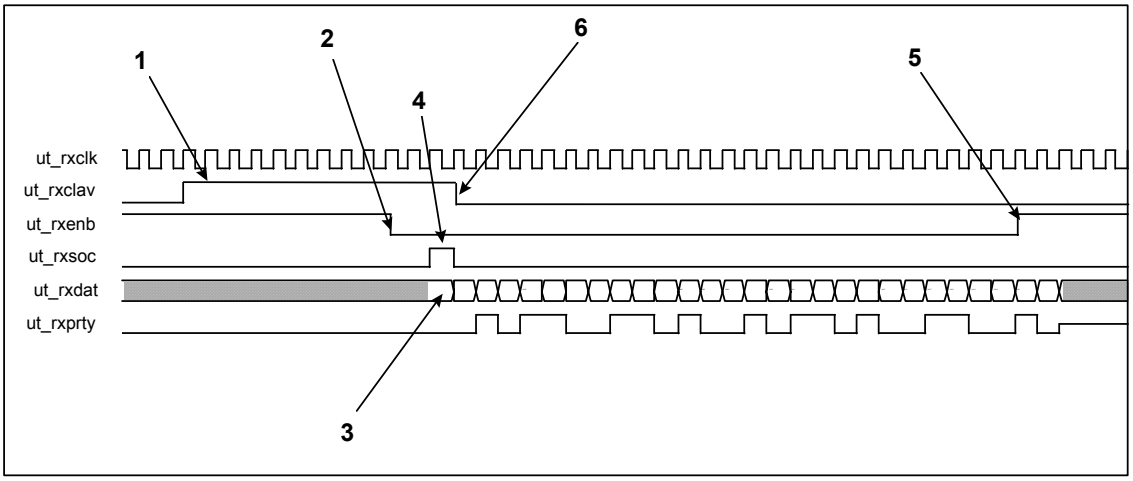

Figure 12: Single Cell Transfer

Back to Back Cell Transfer

If the Master keeps `ut_rxenb` asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps `ut_rxclav` drives the new cell asserting `ut_rxsoc` to indicate the start of a new cell **2**.

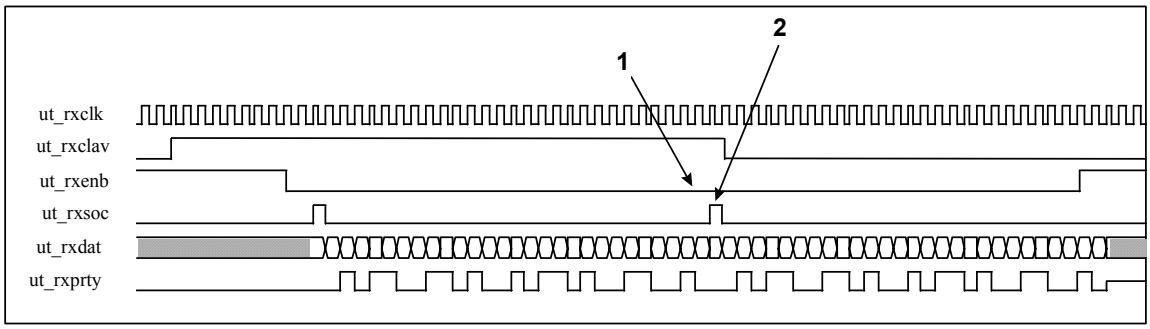

Figure 13: Back to Back Cells Transfer

8 Core Management and Error Handling

On Egress, the Core is designed to handle and report Utopia errors such as Parity error or wrong cell length. Errored cells are discarded with an error status indication provided to the user PHY application.

When an errored cell is received on the Utopia interface, the Core discards the complete cell and provides a cell discard indication to the User PHY application (Signal `eg_err(n)` asserted) **1** together with a cell discard status (Signal `eg_err_stat(1:0)`) **2**.

Note: eg_err is routed to the corresponding wtx_err and etx_err respectively (see Figure 4).

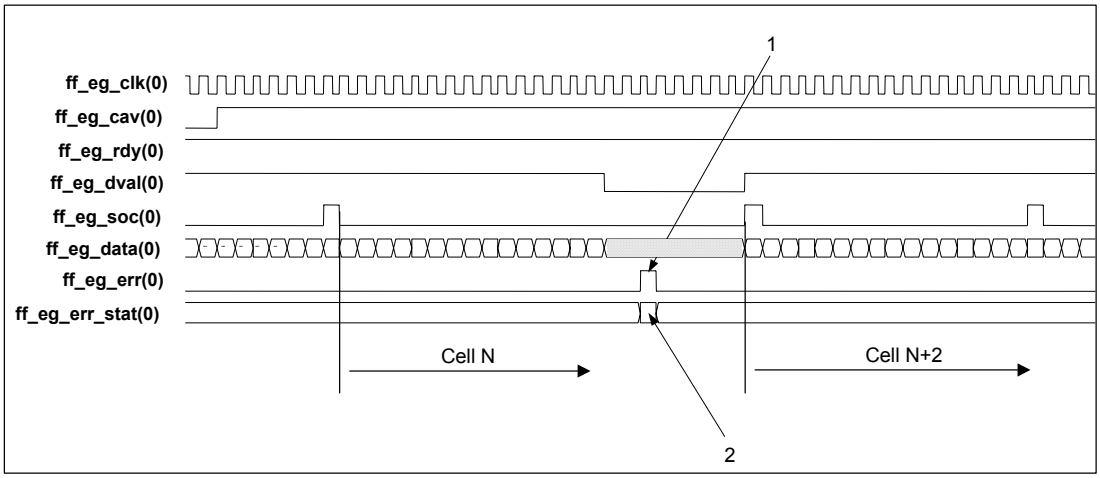

Figure 14: Cell Discard Indication

Table 9: Error Status Word Bit Coding

Error Status Bit	Name	Description
0	PARITY_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a parity error decoded by the Core.
1	LENGTH_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a cell length error detected on the Utopia interface.

The signals are sampled on the corresponding clocks from the west interface:

- etx_... sampled with wrxclk (west receive clock)
- wtx_... sampled with wtxclk (west transmit clock)

9 Complexity and Performance Summary

9.1 Timing Parameters Definition

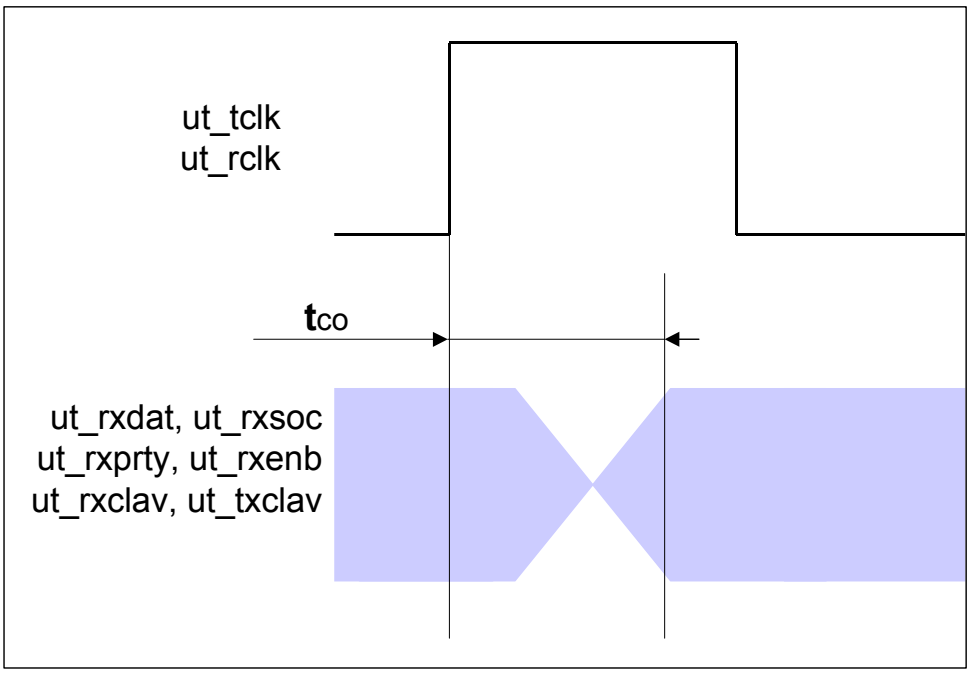

Figure 15: Tco Timing Parameter Definition

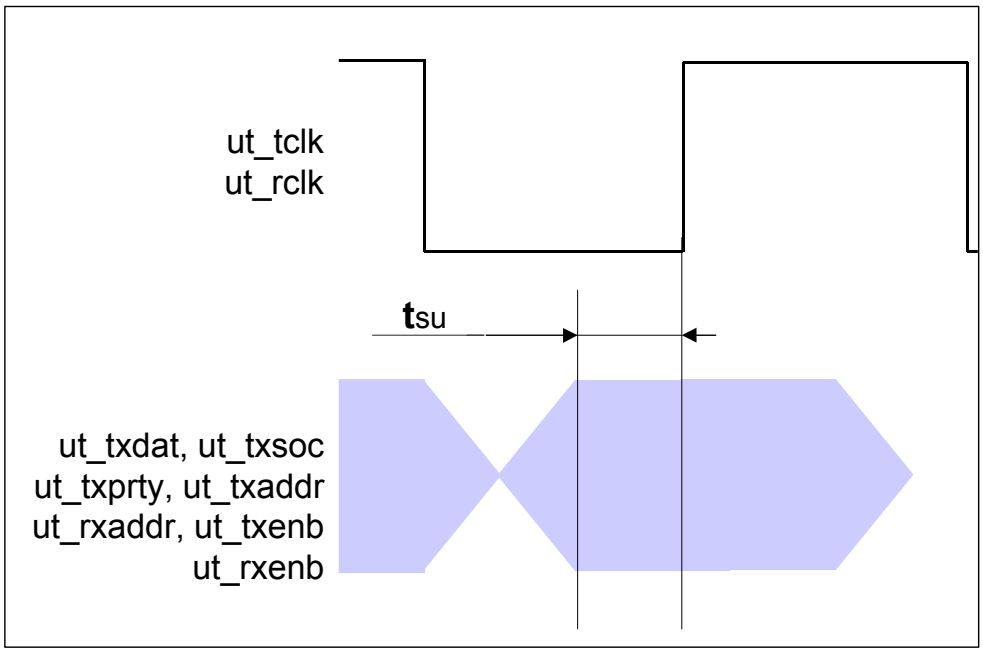

Figure 16: Tsu Timing Parameter Definition

9.2 Eclipse Implementation

Table 10: Eclipse Implementation Summary

Utopia Interface	MPHY	FIFO depth		Selected Options	Implementation	
		Ingress	Egress	Parity	Cells	RAM Blocks
16 Bit	1	768	768	odd	857	16

Table 11: 16-Bit Utopia Interface Timing Characteristics QL6250-PQ208

Parameter	typ	Max		Unit
		-6	-7	
t_{co}	10.0		6.0	ns
t_{su}	2.5		2.0	ns
wrxclk			104	MHz
wtxclk			104	MHz
erxclk			100	MHz
etxclk			100	MHz
minimum reset time	50			ns

Note: QL6250 with timing model "worst" at 25 degrees used.

10 Device Pinout

10.1 Signals Overview

Signals	*Description*
wrxclk, wrxclav, wrxenb*, wrxdat, wrxsoc	West Utopia Receive Interface.
wtxclk, wtxclav, wtxenb*, wtxdata, wtxsoc	West Utopia Transmit Interface.
wtx_err, wtx_err_stat	West Interface error indication (sampled with wtxclk).
erxclk, erxclav, erxenb*, erxdata, erxsoc	East Utopia Receive Interface.
etxclk, etxclav, etxenb*, etxdata, etxsoc	East Utopia Transmit Interface.
etx_err, etx_err_stat	East Interface error indication (sampled with wrxclk).
prty_en, cellsize	Configuration Pins to be board wired. Cellsize[0] should be left open or connected to GND.
reset	Active high device reset
GND	Ground
VCC	Device Power 3.3 V
clk(x)	unused clock inputs should be tied to GND
IOCTRL(x)	
VCCIO(x)	IO Power 3.3 V
INREF(x)	connect to GND
PLLRST(x)	connect to GND or VCC
PLLOUT(x)	connect to GND or VCC
VCCPLL(x)	
GNDPLL(x)	
TCK, TRSTB	JTAG signals. connect to GND
TMS, TDI	JTAG signals. connect to VCC
TDO	JTAG signal. leave open
iov	
nc	not connected. should be left open

*: active low signal

10.2 208 Pin PQFP (PQ208) Pinout Table

PIN	Function	PIN	Function	PIN	Function	PIN	Function
1	pllrst(3)	53	gnd	105	pllrst(1)	157	gnd
2	vccpll(3)	54	vccpll(2)	106	vccpll(1)	158	vccpll(0)
3	gnd	55	pllrst(2)	107	etxclav[0]	159	pllrst(0)
4	gnd	56	vcc	108	gnd	160	gnd
5	wtxclav[0]	57	wrxprty	109	etxprty	161	erxdat[0]
6	wtxprty	58	gnd	110	etxenb	162	vccio(g)
7	wtxenb	59	wrxenb	111	vccio(e)	163	erxdat[1]
8	vccio(a)	60	vccio(c)	112	etxsoc	164	erxdat[2]
9	wtxsoc	61	wrxsoc	113	vcc	165	vcc
10	wtxdat[0]	62	wrxdat[0]	114	etxdat[0]	166	erxdat[3]
11	ioctrl(a)	63	wrxdat[1]	115	etxdat[1]	167	erxdat[4]
12	vcc	64	wrxdat[2]	116	etxdat[2]	168	erxdat[5]
13	inref(a)	65	wrxdat[3]	117	ioctrl(e)	169	ioctrl(g)
14	ioctrl(a)	66	wrxdat[4]	118	inref(e)	170	inref(g)
15	wtxdat[1]	67	ioctrl(c)	119	ioctrl(e)	171	ioctrl(g)
16	wtxdat[2]	68	inref(c)	120	etxdat[3]	172	erxdat[6]
17	wtxdat[3]	69	ioctrl(c)	121	etxdat[4]	173	erxdat[7]
18	wtxdat[4]	70	wrxdat[5]	122	vccio(e)	174	iov
19	vccio(a)	71	wrxdat[6]	123	gnd	175	vcc
20	wtxdat[5]	72	vccio(c)	124	etxdat[5]	176	erxdat[8]
21	gnd	73	wrxdat[7]	125	etxdat[6]	177	vccio(g)
22	wtxdat[6]	74	wrxdat[8]	126	etxdat[7]	178	gnd
23	tdi	75	gnd	127	clk(5)	179	erxdat[9]
24	wtxclk	76	vcc	128	etxclk	180	erxdat[10]
25	clk(1)	77	wrxdat[9]	129	vcc	181	erxdat[11]
26	vcc	78	trstb	130	erxclk	182	vcc
27	wrxclk	79	vcc	131	vcc	183	tck
28	clk(3)	80	wrxdat[10]	132	clk(8)	184	vcc
29	vcc	81	wrxdat[11]	133	tms	185	erxdat[12]
30	clk(4)	82	wrxdat[12]	134	etxdat[8]	186	erxdat[13]
31	wtxdat[7]	83	gnd	135	etxdat[9]	187	erxdat[14]
32	wtxdat[8]	84	vccio(d)	136	etxdat[10]	188	gnd
33	gnd	85	wrxdat[13]	137	gnd	189	vccio(h)
34	vccio(b)	86	vcc	138	vccio(f)	190	erxdat[15]
35	wtxdat[9]	87	wrxdat[14]	139	etxdat[11]	191	cellsize[7]
36	wtxdat[10]	88	wrxdat[15]	140	etxdat[12]	192	ioctrl(h)
37	wtxdat[11]	89	vcc	141	etxdat[13]	193	cellsize[6]
38	wtxdat[12]	90	wtx_err	142	etxdat[14]	194	inref(h)
39	ioctrl(b)	91	wtx_err_stat[0]	143	etxdat[15]	195	vcc
40	inref(b)	92	ioctrl(d)	144	ioctrl(f)	196	ioctrl(h)
41	ioctrl(b)	93	inref(d)	145	inref(f)	197	cellsize[5]
42	wtxdat[13]	94	ioctrl(d)	146	vcc	198	cellsize[4]
43	wtxdat[14]	95	wtx_err_stat[1]	147	ioctrl(f)	199	cellsize[3]
44	vccio(b)	96	etx_err	148	nc	200	cellsize[2]
45	wtxdat[15]	97	etx_err_stat[0]	149	erxclav[0]	201	cellsize[1]
46	vcc	98	vccio(d)	150	vccio(f)	202	nc (cellsize[0])
47	nc	99	etx_err_stat[1]	151	erxprty	203	vccio(h)
48	wrxclav[0]	100	reset	152	erxenb	204	gnd
49	gnd	101	gnd	153	gnd	205	prty_en
50	tdo	102	pllout(0)	154	erxsoc	206	pllout(2)
51	pllout(1)	103	gnd	155	pllout(3)	207	gnd
52	gndpll(2)	104	gndpll(1)	156	gndpll(0)	208	gndpll(3)

10.3 208 Pin PQFP (PQ208) Device Diagram

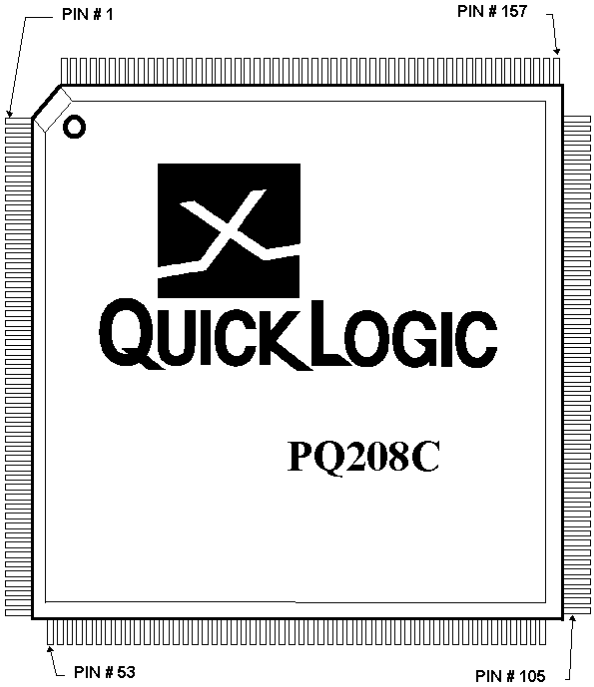

Figure 17: PQ208 top view

10.4 280 Pin FPBGA (PT280) Pinout Table

PIN	Function	PIN	Function	PIN	Function	PIN	Function	PIN	Function
A1	pllout(3)	D1	nc	G19	wrxdat[12]	N16	nc	U6	inref(a)
A2	gndpll(0)	D2	nc	H1	nc	N17	nc	U7	nc
A3	etx_err	D3	nc	H2	nc	N18	ioctrl(c)	U8	nc
A4	etx_err_stat[0]	D4	nc	H3	nc	N19	ioctrl(c)	U9	vccio(a)
A5	etx_err_stat[1]	D5	nc	H4	nc	P1	erxdat[10]	U10	erxclk
A6	ioctrl(f)	D6	nc (cellsize[0])	H5	vcc	P2	erxdat[11]	U11	vccio(b)
A7	wtxclav[0]	D7	prty_en	H15	vcc	P3	ioctrl(h)	U12	nc
A8	wtxprty	D8	reset	H16	vcc	P4	inref(h)	U13	etxdat[13]
A9	wtxenb	D9	clk(8)	H17	wrxdat[13]	P5	vcc	U14	ioctrl(b)
A10	wtxclk	D10	wrxclav[0]	H18	wrxdat[14]	P15	gnd	U15	vccio(b)
A11	wtxsoc	D11	wrxprty	H19	wrxdat[15]	P16	nc	U16	etxdat[5]
A12	wtxdat[0]	D12	wrxenb	J1	nc	P17	nc	U17	tdo
A13	wtxdat[1]	D13	inref(e)	J2	nc	P18	wtx_err	U18	pllrst(2)
A14	ioctrl(e)	D14	wrxsoc	J3	vccio(g)	P19	wtx_err_stat[0]	U19	etxprty
A15	wtxdat[2]	D15	wrxdat[0]	J4	nc	R1	erxdat[7]	V1	pllout(2)
A16	wtxdat[3]	D16	wrxdat[1]	J5	gnd	R2	erxdat[8]	V2	gndpll(3)
A17	wtxdat[4]	D17	wrxdat[2]	J15	vcc	R3	vccio(h)	V3	gnd
A18	pllrst(1)	D18	wrxdat[3]	J16	nc	R4	erxdat[9]	V4	erxprty
A19	gnd	D19	wrxdat[4]	J17	vccio(d)	R5	gnd	V5	erxenb
B1	pllrst(0)	E1	cellsize[3]	J18	nc	R6	gnd	V6	ioctrl(a)
B2	gnd	E2	cellsize[2]	J19	nc	R7	vcc	V7	nc
B3	wtxdat[5]	E3	vccio(g)	K1	vcc	R8	vcc	V8	nc
B4	wtxdat[6]	E4	cellsize[1]	K2	tck	R9	gnd	V9	nc
B5	wtxdat[7]	E5	gnd	K3	nc	R10	gnd	V10	clk(1)
B6	inref(f)	E6	vcc	K4	nc	R11	vcc	V11	clk(4)
B7	wtxdat[8]	E7	vcc	K5	gnd	R12	vcc	V12	nc
B8	wtxdat[9]	E8	vcc	K15	gnd	R13	vcc	V13	etxdat[14]
B9	tms	E9	vcc	K16	nc	R14	vcc	V14	inref(b)
B10	clk(6)	E10	gnd	K17	nc	R15	gnd	V15	etxdat[9]
B11	wtxdat[10]	E11	gnd	K18	nc	R16	etxdat[3]	V16	etxdat[6]
B12	wtxdat[11]	E12	vcc	K19	trstb	R17	vccio(c)	V17	etxdat[1]
B13	ioctrl(e)	E13	vcc	L1	nc	R18	etxenb	V18	gndpll(2)
B14	wtxdat[12]	E14	gnd	L2	nc	R19	wtx_err_stat[1]	V19	gnd
B15	wtxdat[13]	E15	gnd	L3	vccio(h)	T1	erxdat[2]	W1	gnd
B16	wtxdat[14]	E16	wrxdat[5]	L4	nc	T2	erxdat[3]	W2	pllrst(3)
B17	vccpll(1)	E17	vccio(d)	L5	vcc	T3	erxdat[4]	W3	nc
B18	gndpll(1)	E18	inref(d)	L15	gnd	T4	erxdat[5]	W4	nc
B19	pllout(0)	E19	ioctrl(d)	L16	nc	T5	erxdat[6]	W5	nc
C1	wtxdat[15]	F1	inref(g)	L17	vccio(c)	T6	ioctrl(a)	W6	erxclav[0]
C2	vccpll(0)	F2	ioctrl(g)	L18	nc	T7	nc	W7	nc
C3	nc	F3	cellsize[5]	L19	nc	T8	nc	W8	nc
C4	nc	F4	cellsize[4]	M1	erxdat[15]	T9	nc	W9	tdi
C5	vccio(f)	F5	gnd	M2	nc	T10	nc	W10	etxclk
C6	ioctrl(f)	F15	vcc	M3	nc	T11	clk(3)	W11	nc
C7	nc	F16	ioctrl(d)	M4	nc	T12	nc	W12	nc
C8	nc	F17	wrxdat[6]	M5	vcc	T13	etxdat[12]	W13	etxdat[15]
C9	vccio(f)	F18	wrxdat[7]	M15	vcc	T14	etxdat[11]	W14	ioctrl(b)
C10	wrxclk	F19	wrxdat[8]	M16	inref(c)	T15	etxdat[8]	W15	etxdat[10]
C11	vccio(e)	G1	nc	M17	nc	T16	etxdat[4]	W16	etxdat[7]
C12	nc	G2	cellsize[7]	M18	nc	T17	vccpll(2)	W17	etxdat[2]
C13	nc	G3	ioctrl(g)	M19	nc	T18	etxsoc	W18	etxdat[0]
C14	nc	G4	cellsize[6]	N1	ioctrl(h)	T19	etxclav[0]	W19	pllout(1)
C15	vccio(e)	G5	vcc	N2	erxdat[12]	U1	erxsoc		
C16	nc	G15	vcc	N3	erxdat[13]	U2	erxdat[0]		
C17	nc	G16	wrxdat[9]	N4	erxdat[14]	U3	vccpll(3)		
C18	nc	G17	wrxdat[10]	N5	vcc	U4	erxdat[1]		
C19	nc	G18	wrxdat[11]	N15	vcc	U5	vccio(a)		

10.5 280 Pin FPBGA (PT280) Device Diagram

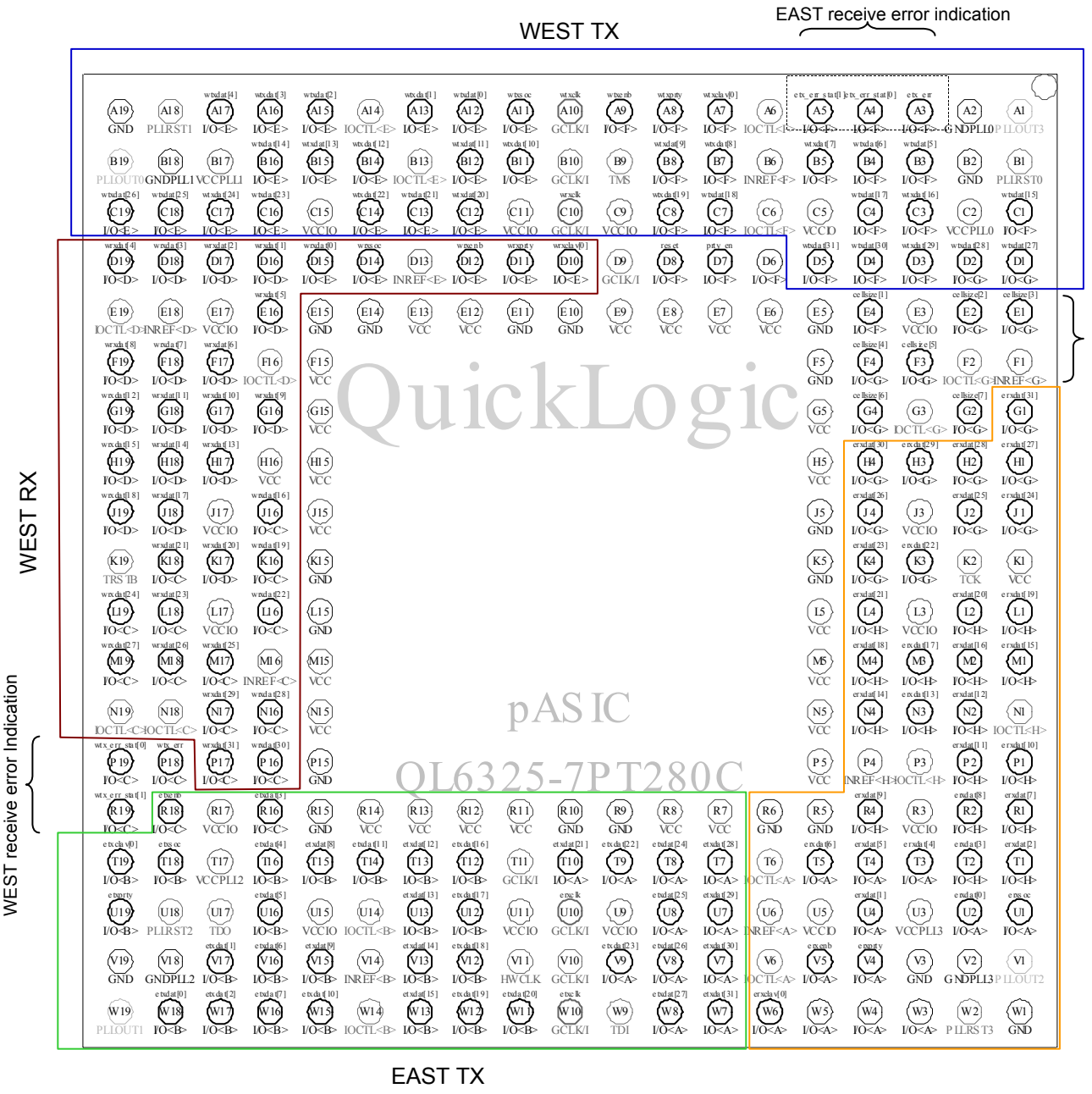

Figure 18: PT280 bottom view (0.8mm FPBGA)

11 References

- ATM Forum, Utopia Level 2, af-phy-0039.000
- ATM Forum, Utopia Level 3, af-phy-0136.000
- Quicklogic, Eclipse Family Datasheet

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