

2.488 Gbps FULLY INTEGRATED LOW POWER SONET/SDH TRANSCEIVER

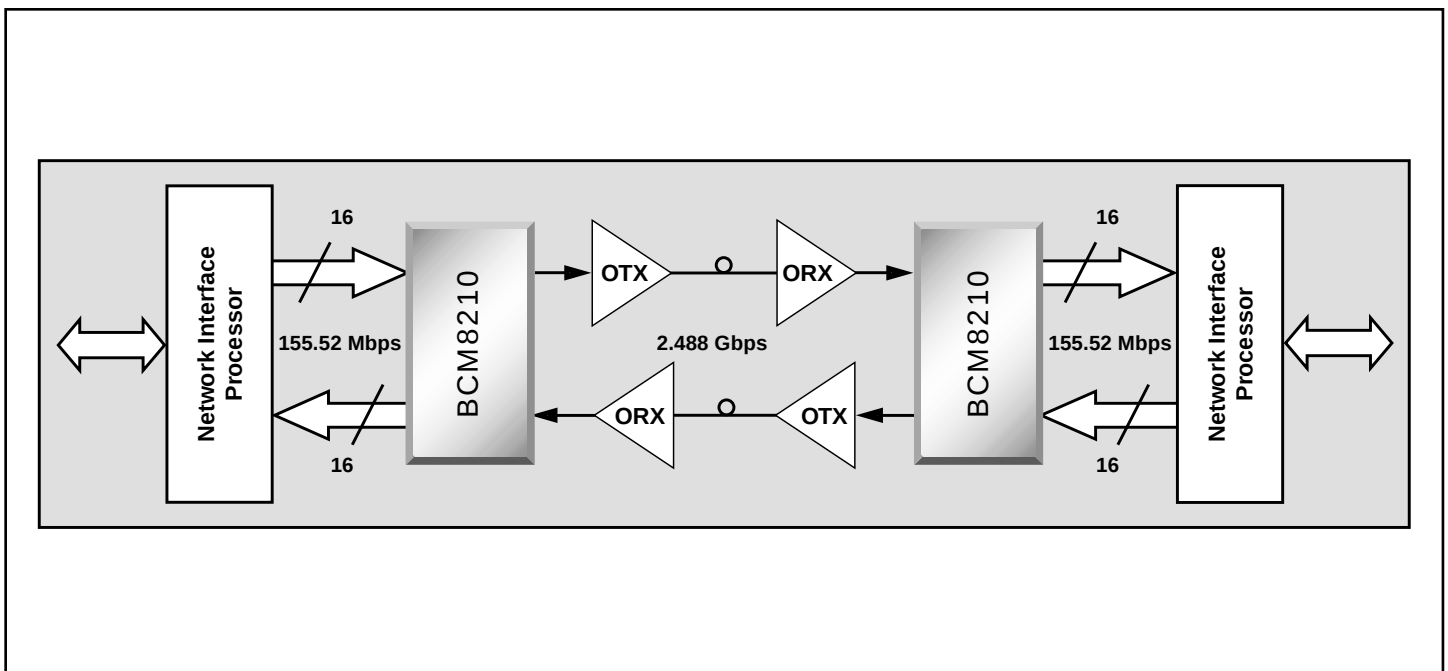
BCM8210 FEATURES

- Fully integrated OC-48/STM-16 SONET/SDH transceiver with CDR, MUX, DEMUX, and CMU
- 16-bit, 155.52-Mbps LVPECL interface
- On-chip, PLL-based clock generator
- Loss-of-signal (LOS) output
- Line and system loopback modes
- Lock detect
- Meets SONET, Telcordia, and ITU-T jitter requirements
- Power supply: 2.5V (core), 3.3V (LVPECL I/O)
- Power dissipation: 1.2W typical
- 14 × 20 mm, 128-pin PQFP package
- Standard CMOS fabrication process

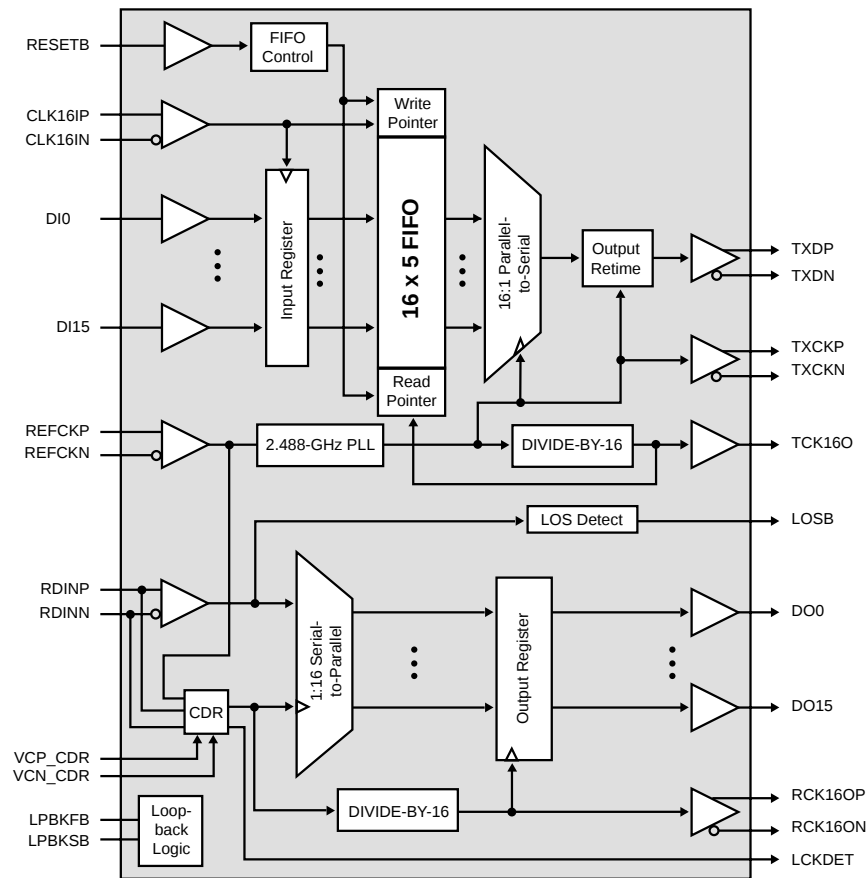
SUMMARY OF BENEFITS

- First CMOS OC-48 transceiver in the world.
- Low power consumption eliminates external heat sink, fans for system airflow, and expensive high current power supplies.
- High integration reduces design cycle and time to market.
- Increased port density per board and system.
- CMOS-based device takes advantage of the most effective silicon economy of scale.
- Features low-jitter CMU: 3 mUI_{RMS} typical.
- Target applications:
 - OC-48/STM-16 transmission equipment
 - SONET/SDH optical modules and test equipment
 - ADD/DROP multiplexers
 - Digital cross-connects
 - ATM switch backbones
 - Terabit routers

Application Block Diagram



Block Diagram



The **BCM8210** SONET/SDH transceiver is a fully integrated serialization/deserialization SONET OC-48 and STM SDH-16 (2.488 Gbps) interface device with an integrated clock multiplication unit (CMU) and an integrated clock and data recovery circuit (CDR). On-chip clock synthesis is performed by the high-frequency, low-jitter, phase-locked loop on the **BCM8210** transceiver chip, allowing the use of a slower 77.76 MHz external transmit clock reference. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The low-jitter LVPECL interface guarantees compliance with the bit error rate requirements of the Telcordia GR-253-CORE, ANSI, and ITU-T standards. The **BCM8210** is packaged in a 14 × 20 mm, 128-pin PQFP.

Transmitter Functions

- 16-bit parallel input
- 2.488-GHz clock generation
- Elastic buffering
- Parallel-to-serial conversion
- Serial differential data output

Receiver Functions

- 16-bit parallel output
- 2.488-Gbps differential data input
- Clock and data recovery (CDR)
- Serial-to-parallel conversion

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