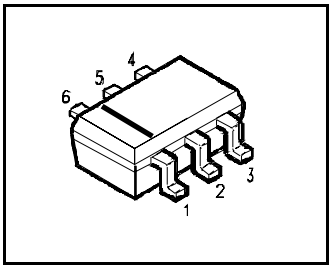
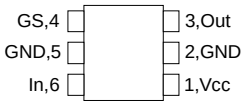
A 1.85 GHz High Gain Low Noise Transistor Amplifier using BGA428

Features

- **Two-stage Low Noise Amplifier**
- **SIEGET®45-Technology with 45 GHz f_T**
- **Small outline SOT363-Package**
- **Low Noise Figure: 1.5 dB at 1.85 GHz**
- **19 dB Gain at 1.85 GHz**
- **Gain step function:**
  - **19 dB typical in High Gain mode**
  - **-13 dB typical in Low Gain mode**
- **2.4 - 3.3 V Supply Voltage range**
- **Requires only 2 external matching elements at 1.85 GHz**





Note: Top View

Figure 2: Pin Connections, SOT-363.

Applications

Amplifier applications for cellular phones, cordless phones, PCS, DECT, W/LANs, PHS, GSM 1800, RF modems and others.

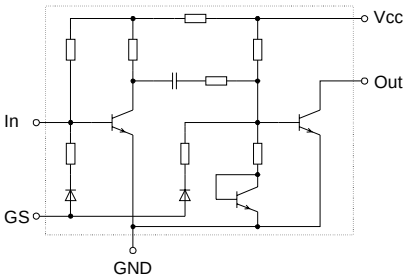


Figure 1: Equivalent Circuit of BGA428.

Introduction

The Infineon BGA428 is a high performance two stage CE-CE transistor amplifier based on the BH6Fplus SIEGET®45-Technology. High gain and low noise figure make it an ideal solution for Low Noise Amplifiers and receiver front end stages and other applications requiring moderate linearity up to 2 GHz. Internal prematching simplifies RF design effort and enables a simple, low-parts-count RF matching solution. The BGA428's typical supply voltage range is 2.4 to 3.3 volts. Gain may be reduced by approximately 32 dB in a single step by reducing Vcc to 0V and applying 2.7 V to GS.

Description

The BGA428 is an integrated circuit consisting of two silicon bipolar transistor amplifier stages. Each transistor stage was optimized for overall device gain, linearity, noise figure and RF pre-matching. A reduced gain step is provided as well as a complete bias circuit. The BGA428 is fabricated using SIEGET®45-Technology. SIEGET®45 stands for SIEMENS grounded emitter transistors having a transition frequency of 45 GHz. This process is tailored for high frequency operation at low current levels.

The features of the BGA428 allow fast, easy RF amplifier circuit designs requiring low component count and minimal printed circuit board area. DC power is provided by simply applying the proper voltage on the Vcc pin, although the circuit designer has the option of biasing each of the two stages separately. Internal prematching eases the external RF matching task while preserving some degree of flexibility for the user. In a typical application no additional input matching elements are required. Output matching is a simple task and the function of the RF matching circuit can be combined with the coil that brings in DC bias. Applying bias to the GS pin and grounding Vcc provides a reduced gain step of -32 dB.

The BGA428 is developed for use in battery powered equipment demanding high performance with low supply voltages. Typical applications for the device include low noise RF amplifiers, IF amplifiers and gain and buffer stages up to 2 GHz. The BGA428 is an excellent choice for use in cellular and cordless telephones and other commercial wireless equipment.

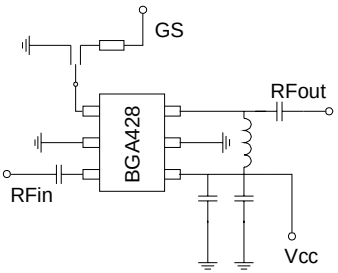


Figure 3: Typical Circuit using BGA428.

Design Steps

This section describes a general approach for designing amplifiers and points out the advantages of using the BGA428. The following list shows the most important steps in developing an amplifier board:

1. Selection of DC bias level
2. Check for stability
3. Determine the required DC supply circuit
4. Design input impedance matching circuit, if needed
5. Design output matching circuit
6. Layout of the printed circuit board
7. Optimization

These steps will now be discussed in the following sections.

Select DC bias voltage

Determining the bias voltage for the BGA428 is simple in most cases, since it is often limited by available system resources or by the desired gain or noise figure. Increasing Vcc offers higher gain and lower noise figure at the cost of higher device current and power consumption

Figures 4 - 6 show dependencies of the BGA428's noise figure, gain and device current on the supply voltage. These results were obtained using a test fixture which is described in the BGA428's data sheets.

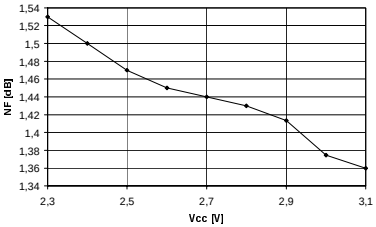


Figure 4: Noise Figure vs. Vcc.

Figure 5: Gain vs. Vcc.

Figure 6: Device Current vs. Vcc.

Stability check

A stability check is necessary to examine a circuit's tendency to oscillate. This can be done by using a CAD program to calculate the stability factor K and the stability measure $B1$. The factors K and $B1$ are both derived from the S-parameters for the BGA428 at the previously established bias voltage. The conditions for unconditional stability are:

$K > 1$ and $B > 0$.

Although for unconditional stability both factors, K and $B1$, have to be taken into account, most designers refer only to K, as this measure of stability alone can give good insight into the propensity of a circuit to oscillate. To ensure stable operation when the amplifier is terminated in any real, passive impedance, it is advisable to target a minimum K value in the range of 1.2 to 1.5, as a general rule.

Due to its internal prematching, the BGA428 offers a high degree of stability, so that for most applications no additional measures have to be taken.

Figures 7 and 8 show the application circuit's measured stability factor K and its stability measure $B1$. There were no additional measures taken to increase stability.

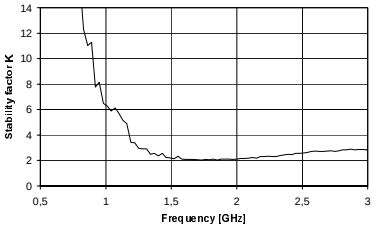


Figure 7: Measured Stability Factor.

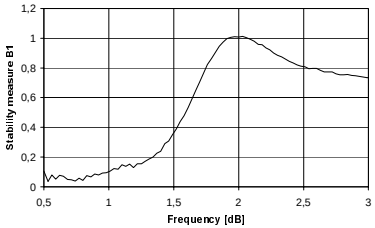


Figure 8: Measured Stability Measure.

DC bias supply

Setting up the bias supply of the BGA428 is fairly simple. Only the required voltage has to be applied as the circuit for setting the operating current is integrated into the device. The first stage is supplied by the Vcc pin, and the second stage through the open-collector RF output.

Vcc and Out are normally connected by an inductor, which is part of the output RF matching circuit, although it is possible to bias both stages separately. The RF at the output is blocked by the inductor and should be decoupled from the DC supply using shunt capacitance on the Vcc pin. The RF Input and RF Output should be DC blocked with capacitors if the amplifier is to be cascaded with stages that do not present a DC open circuit to the BGA428.

If the gain step feature is not being used the GS pin has to be tied to ground to ensure the diodes in figure 1 are reverse-biased. When turning on the gain step feature, it is recommended to use a current limiting series resistor between the GS pin and its voltage source.

Input match

The input matching circuit is designed for either of two goals, to achieve minimum noise figure or maximum power gain together with best possible return loss. In most cases, however, a compromise between noise figure and return loss (and thus gain) has to be made.

The BGA428's internal prematching offers a good tradeoff between high gain and low noise figure with sufficiently low return loss for most applications. This reduces required parts count for the input match.

The BGA428's input return loss values in the frequency band of interest are typically slightly below -10 dB.
Input return loss better than -15 dB is an indication for an increased parasitic emitter inductance, which will degrade gain and output match.

Output match

The output of an amplifier is normally matched for maximum power transfer, which implies maximum gain and best possible output return loss. Maximum power transfer occurs when the output is matched to the conjugate of Γ_{ML} . Γ_{ML} is the reflection coefficient of the load impedance resulting from simultaneous conjugate match of input and output.

Using the BGA428, output matching is normally done by using a high-pass shunt L - series C matching circuit. In this configuration the inductor can be used for both the RF output match and the DC biasing of the second stage. The series C element serves both an RF matching and a DC blocking function. The variation of the values of L and C determines the frequency of operation.

Board layout

For the printed circuit board design and layout it is necessary to know the height and relative dielectric constant (ε_r) of the board material to compute the width of 50 Ω microstrip lines.

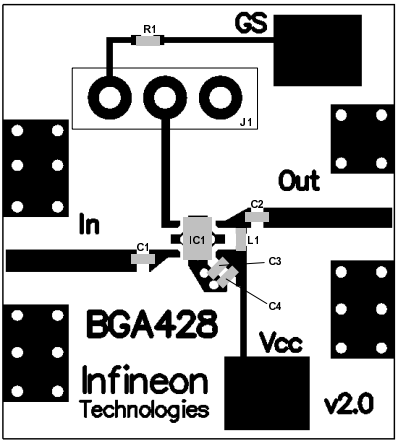


Figure 9: Application Board Layout (actual size: 18 mm x 20 mm).

All external components should be placed as close as possible to the BGA428 for best performance. Of utmost importance is keeping the paths from the ground pins to the via holes as short as possible to reduce parasitic emitter inductance, which degrades gain and the output match. It is suggested that numerous via holes be used for the ground connections in the PCB design to obtain as good of an RF ground as is possible.

Figure 10 shows the layout of the application board. The vias under the SOT-636-package provide a very short, low-inductance path to ground, and it is possible to place L1 directly next to the FCC and Out pin.

Table 1: List of components.

Name	Value	Package	Function
C1	150 pF	0402	DC block
C2	0.85 pF	0402	Output match
C3	47 pF	0402	RF decoupling
C4	220 pF	0402	RF decoupling
J1	3 pin	-	Switches GS on/off
L1	3.9 nH	0402	Output match
R1	3.3 kΩ	0402	Current limiter
V1	BGA428	SOT 363	

Optimization

With the completed electrical design and layout it is prudent to do a final analysis and optimization of the circuit. During this design iteration additional parasitics should be taken into account, such as actual transmission line dimensions, parasitic inductances in chip capacitors, and via-hole effects. Based on simulation results board dimensions and other parameters can be changed to their final values.

Measurement results

The performance of the circuit at 1.85 GHz can be summarized by the following data:

Vcc = 2.7 V
Icc = 8.1 mA
Gain = 19.4 dB
NF = 1.5 dB
RLin = -12.8 dB
RLout = -11.7 dB
$IP3_{out}$ = 8.5 dBm
$P_{1dB, in}$ = -19 dBm

The following figures show the small signal S-parameter measurement results. The graphs include losses caused by SMA connectors and microstrip lines on the PCB boards.

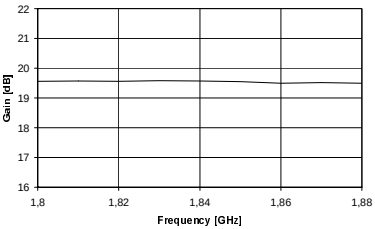


Figure 10: Measured Gain over GSM 1800 Frequency Band.

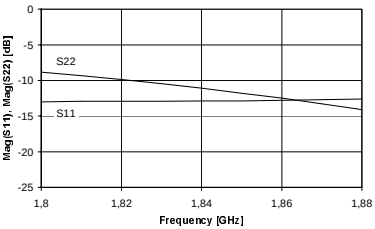


Figure 11: Measured Input and Output Return Loss over GSM 1800 Frequency Band.

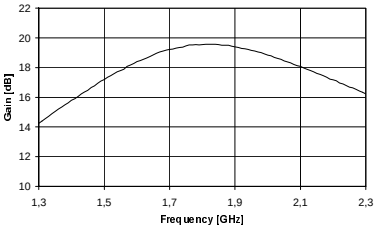


Figure 12: Measured Gain for Extended Frequency.

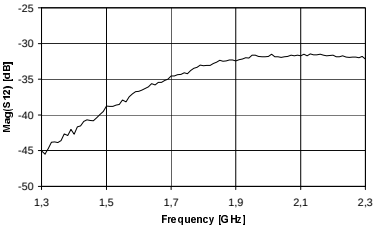


Figure 14: Measured Reverse Isolation.

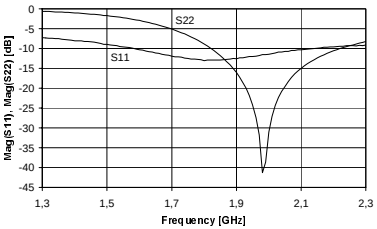


Figure 13: Measured Input and Output Return Loss for Extended Frequency.

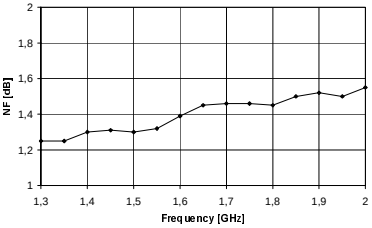


Figure 15: Measured Noise Figure.