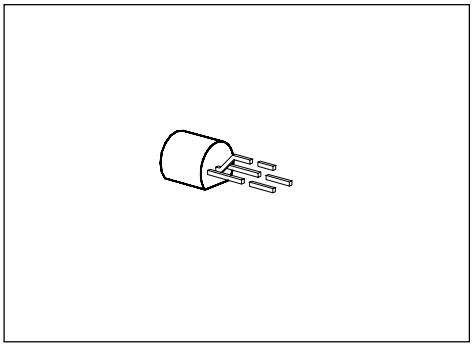
SIEMENS

## Silicon N Channel MOSFET Triode

**BF 987**

- For high-frequency stages up to 300 MHz, preferably in FM applications
- High overload capability



| Type | Marking | Ordering Code | Pin Configuration | | | Package[1] |
|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | |
| BF 987 | – | Q62702-F35 | D | S | G | TO-92 |

### Maximum Ratings

| Parameter | Symbol | Values | Unit |
|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | 20 | V |
| Drain current | $I_D$ | 30 | mA |
| Gate-source peak current | $\pm I_{GSM}$ | 10 | |
| Total power dissipation, $T_A \leq 45$ °C | $P_{tot}$ | 300 | mW |
| Storage temperature range | $T_{stg}$ | – 55 … + 150 | °C |
| Channel temperature | $T_{ch}$ | 150 | |

### Thermal Resistance

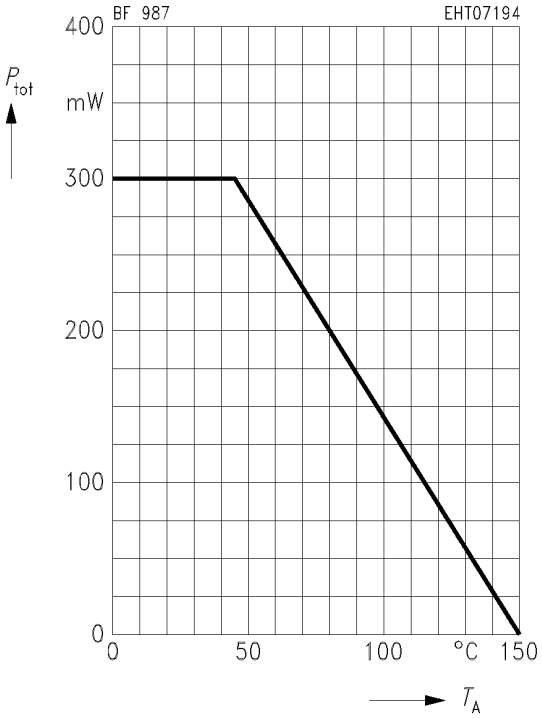
| | | | |
|---|---|---|---|
| Junction - ambient | $R_{th\ JA}$ | ≤ 350 | K/W |

[1] For detailed information see chapter Package Outlines.

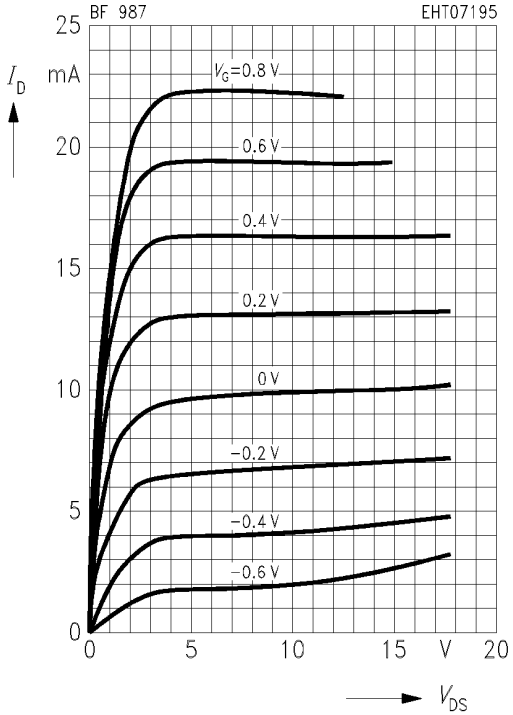
**Electrical Characteristics**
at $T_A$ = 25 °C, unless otherwise specified.

| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| **DC Characteristics** | | | | | |
| Drain-source breakdown voltage<br>$I_D$ = 10 µA, – $V_{GS}$ = 4 V | $V_{(BR)\ DS}$ | 20 | – | – | V |
| Gate-source breakdown voltage<br>± $I_{GS}$ = 10 mA, $V_{DS}$ = 0 | ± $V_{(BR)\ GSS}$ | 6.5 | – | 12 | |
| Gate-source leakage current<br>± $V_{GS}$ = 5 V, $V_{DS}$ = 0 | ± $I_{GSS}$ | – | – | 50 | nA |
| Drain current<br>$V_{DS}$ = 10 V, $V_{GS}$ = 0 | $I_{DSS}$ | 5 | – | 18 | mA |
| Gate-source pinch-off voltage<br>$V_{DS}$ = 10 V, $I_D$ = 20 µA | – $V_{GS\ (p)}$ | – | – | 2.5 | V |
| **AC Characteristics** | | | | | |
| Forward transconductance<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA, $f$ = 1 kHz | $g_{fs}$ | 14 | 16 | – | mS |
| Gate input capacitance<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA, $f$ = 1 MHz | $C_{gss}$ | – | 2.7 | – | pF |
| Reverse transfer capacitance<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA, $f$ = 1 MHz | $C_{dg}$ | – | 35 | – | fF |
| Output capacitance<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA, $f$ = 1 MHz | $C_{dss}$ | – | 1 | – | pF |
| Power gain (test circuit)<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA , $f$ = 200 MHz,<br>$G_G$ = 2 mS, $G_L$ = 0.5 mS | $G_p$ | – | 25 | – | dB |
| Noise figure (test circuit)<br>$V_{DS}$ = 10 V, $I_D$ = 10 mA , $f$ = 200 MHz,<br>$G_G$ = 2 mS, $G_L$ = 0.5 mS | $F$ | – | 1 | – | |

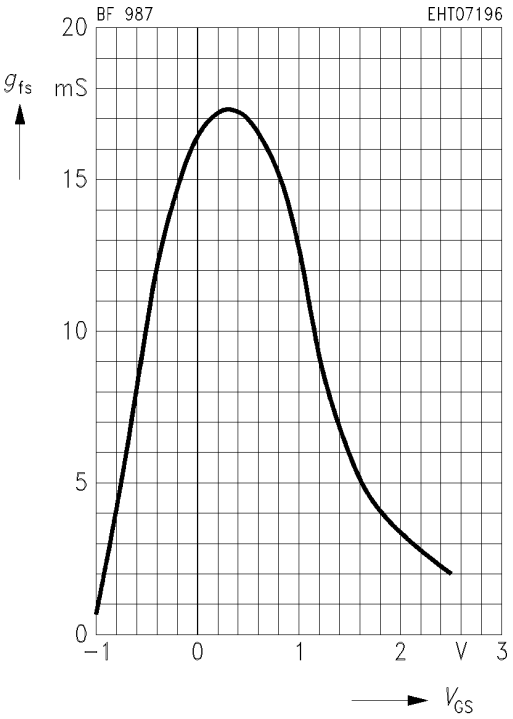
**Total power dissipation $P_{tot} = f(T_A)$**



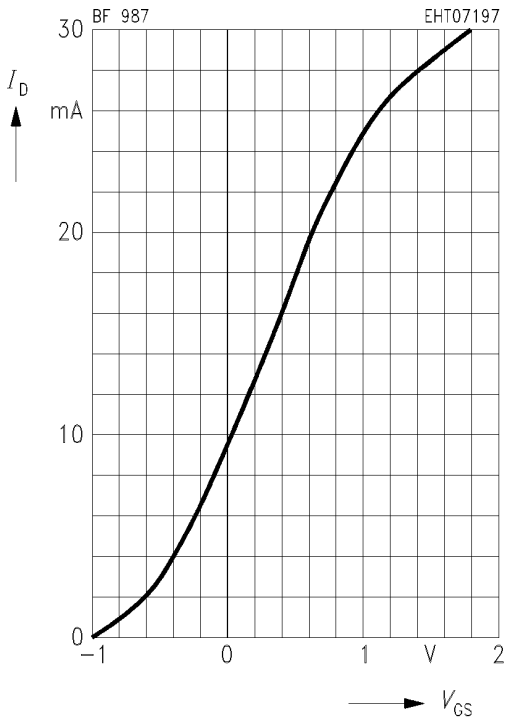

**Output characteristics $I_D = f(V_{DS})$**



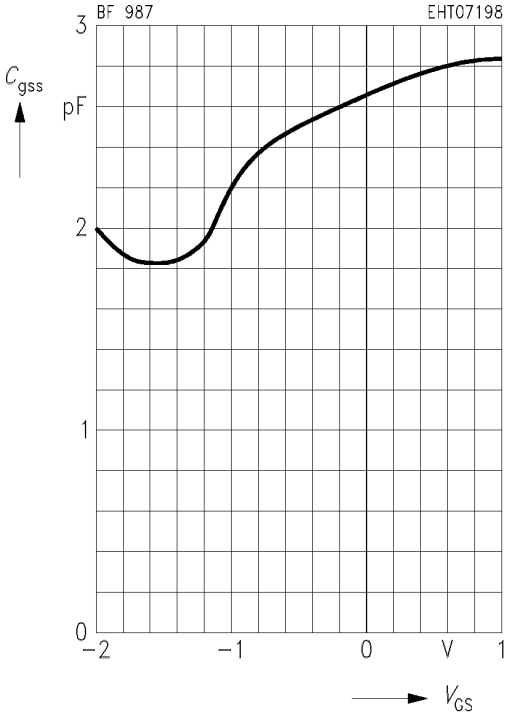

**Gate transconductance $g_{fs} = f(V_{GS})$**
$V_{DS}$ = 10 V, $I_{DSS}$ = 10 mA, $f$ = 1 kHz



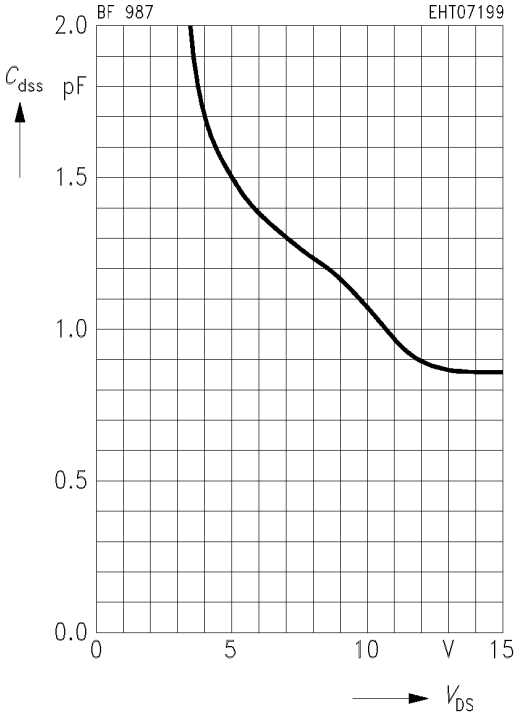

**Drain current $I_D = f(V_{GS})$**
$V_{DS}$ = 10 V



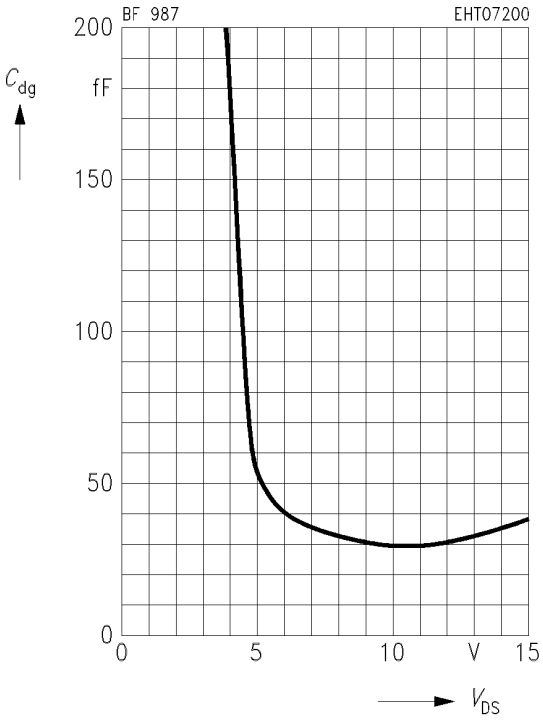
**Gate input capacitance $C_{gss} = f(V_{GS})$**
$V_{DS}$ = 10 V, $I_{DSS}$ = 10 mA, $f$ = 1 MHz



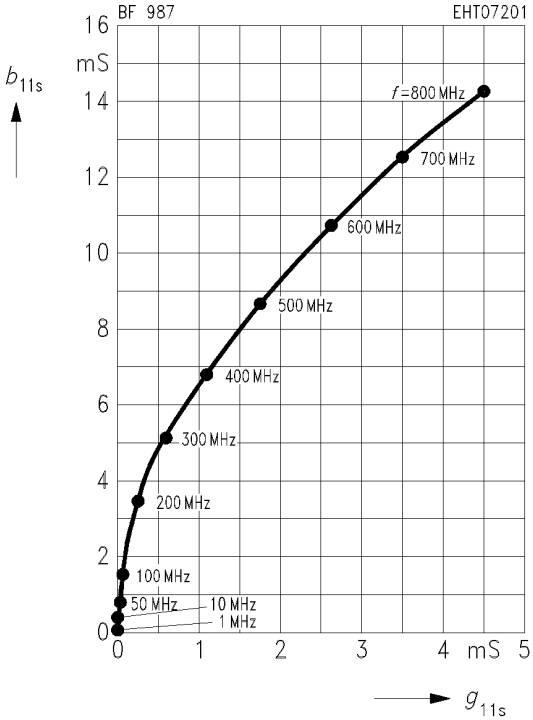

**Output capacitance $C_{dss} = f(V_{DS})$**
$V_{GS}$ = 0, $I_{DSS}$ = 10 mA, $f$ = 1 MHz



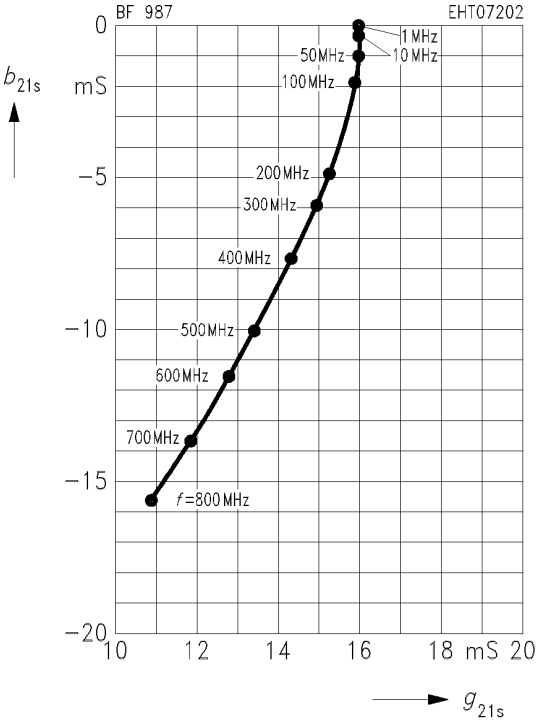

**Reverse transfer capacitance $C_{dg} = f(V_{DS})$**
$I_{DSS}$ = 10 mA, $f$ = 1 MHz, $V_{GS}$ = 0



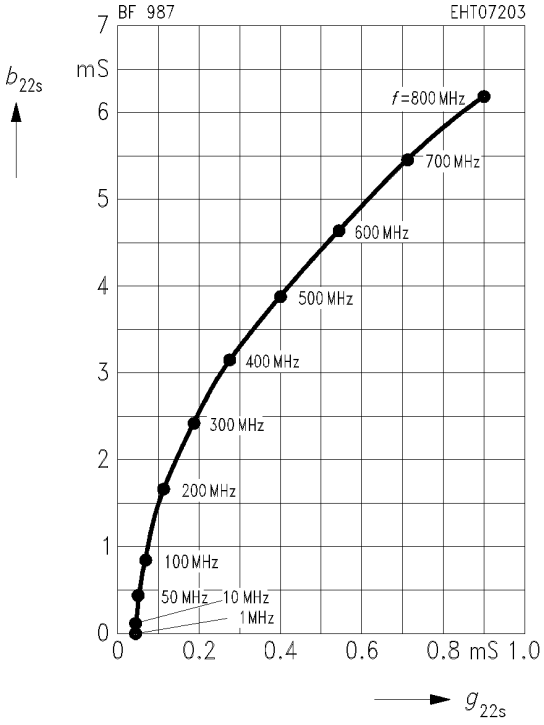

**Gate input admittance $y_{11s}$**
$V_{DS}$ = 10 V, $I_{DSS}$ = 10 mA, $V_G$ = 0
(common source)



**Gate forward transfer admittance $y_{21s}$**
$V_{DS}$ = 10 V, $V_G$ = 0, $I_{DSS}$ = 10 mA
(common source)




**Output admittance $y_{22s}$**
$V_{DS}$ = 10 V, $I_{DSS}$ = 10 mA, $V_G$ = 0
(common source)




**Test circuit for power gain and noise figure**
$f$= 200 MHz