# Bt812

## *NTSC/PAL to RGB/YCrCb Decoder*

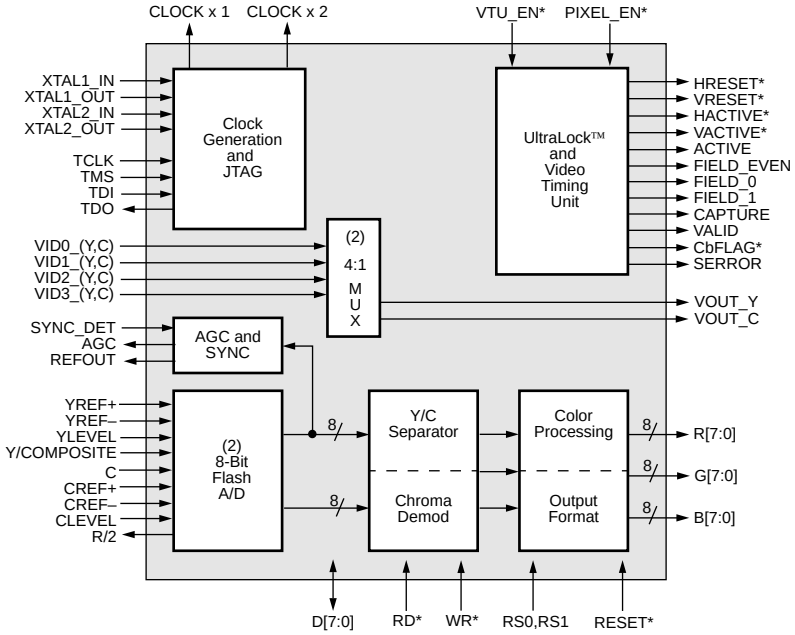
The Bt812 Image Digitizer converts NTSC and PAL composite or Y/C analog video signals to either digital RGB or YCrCb video data at pixel rates from 8–15 MHz. This digitizer supports 24-bit RGB, 16-bit RGB, 15-bit RGB, 4:4:4 24-bit YCrCb, or 4:2:2 16-bit YCrCb output formats.

The hue, contrast, saturation, and brightness levels are adjustable through the MPU interface.

The 4:1 analog multiplexers enable the NTSC, PAL, Y, and C video signals to be individually filtered before the Bt812 is driven, simplifying external circuitry.

Horizontal and vertical timing information is generated and output through HRESET* and VRESET*. Programmable blanking information is output on the HACTIVE*, VACTIVE* and ACTIVE pins. The FIELD_EVEN, FIELD_0, and FIELD_1 outputs specify which one of four (NTSC) or eight (PAL) fields is being processed.

### Functional Block Diagram




### Distinguishing Features

- Ability to Digitize Composite or Y/C (NTSC or PAL)
- Flexible Video Resolutions up to 15 MSPS
- On-Chip Ultralock™
- Programmable Hue, Brightness, Contrast, and Saturation
- Supports 2X Clock Operation
- RGB or YCrCb Output Formats
- 0.7–2 V Video Input Signals
- Standard MPU Interface
- 160-pin PQFP Package
- JTAG Support
- Typical Power Dissapation: 0.9 W

### Applications

- Multimedia
- Image Processing
- Desktop Video
- Video Phone
- Teleconferencing

### Related Products

- Bt851
- Bt858
- Bt885
- Bt895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## Ordering Information

| Model Number | Package | Ambient Temperature Range |
|---|---|---|
| Bt812KPF | 160-pin PQFP | 0° to +70° C |
| Bt812KPF27 | 160-pin PQFP | 0° to +70° C |

## Recommended Sockets For Prototyping With The Bt812KPF

| Manufacturer | Part Number | Part Description |
|---|---|---|
| Amp | A22 114-4<br>A22 115-4 | Housing Assembly<br>Lid |
| Yamaichi | IC51-1604-845-1 | Test and Burn-In Socket |


Print date: February, 1996



PRINTED IN THE UNITED STATES OF AMERICA

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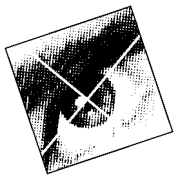


# FUNCTIONAL DESCRIPTION

## Pin Descriptions

**Table 1. Pin Assignments** *(1 of 3)*

| Pin Name | Description |
|---|---|
| **The Input Stage** | |
| VID(3–0)_Y, VID(3–0)_C | Analog video inputs to the multiplexers from the sources to be digitized. Unused inputs should be connected to ground. |
| VOUT_Y, VOUT_C | The analog video outputs of the two 4:1 multiplexers. Connected to the Y/Composite and C inputs of the ADCs. |
| Y/COMPOSITE | The analog video input to the Y-ADC. |
| C | The analog chroma input (for S-video) to the C-ADC. |
| R/2 | The midpoint tap output of the reference ladder for the chroma ADC. If not used, this pin should remain floating. A decoupling capacitor is not recommended on this pin. Used for DC restoration of the C-ADC. |
| YLEVEL | The level input for DC restoration of the luma input. Typically connected to ground. |
| CLEVEL | The level input for DC restoration of the chroma input. Typically connected to the R/2 ladder tap of the C-ADC. |
| SYNC_DET | The sync stripper input used to generate timing information. Must be connected to the same video source as the Y-ADC. |
| YREF–, CREF– | The bottom of the reference ladder for Y-and C-ADCs. Typically connected to ground. |
| YREF+, CREF+ | The top of the reference ladder for Y-and C-ADCs. Typically driven by REFOUT. |
| REFOUT | Output of the AGC, which drives YREF+ and CREF+. |
| AGC | Load capacitance for AGC circuitry. Must be connected to 0.1 µf capacitor. |
| **The MPU Interface** | |
| RD* | The read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. |
| WR* | The write control input (TTL compatible). If WR* is a logical zero, data is written into the device through D0–D7. Both RD* and WR* should not be asserted simultaneously. |
| D0–D7 | Bidirectional MPU data and address bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit. |

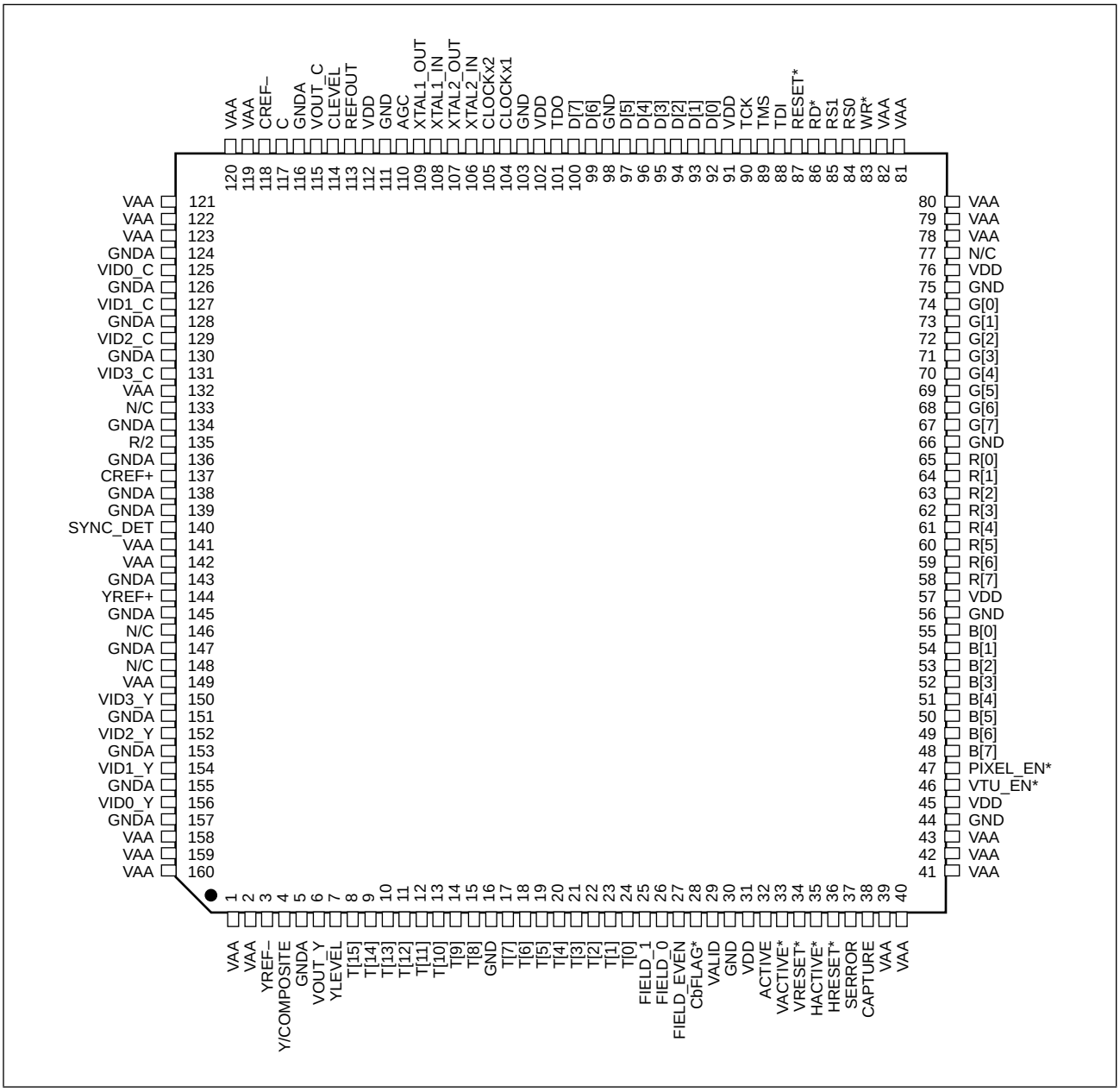
**Table 1. Pin Assignments** *(2 of 3)*

| Pin Name | Description |
|---|---|
| RS0, RS1 | MPU address control inputs (TTL compatible). RS0 and RS1 specify which internal register the MPU is accessing, as shown in Tables 2 and 3. They are latched on the falling edge of RD* and WR*. |
| RESET* | Reset control input (TTL compatible). A logical zero for a minimum of four consecutive clock cycles resets the device. A logical zero for less than four clocks will leave the device in an undefined state. |
| **The Video Timing Unit** | |
| CbFLAG* | Cb indicator output (TTL compatible). CbFLAG* is output following the rising edge of the CLOCKx1. For 16-bit YCrCb data, this output indicates whether the data on the B0–B7 outputs contains Cb (logical zero) or Cr (logical one) data. |
| HRESET* | Horizontal timing output (TTL compatible). The falling edge of this output indicates the beginning of a new scan line of video. HRESET* is output following the rising edge of CLOCKx1. |
| VRESET* | Vertical timing output (TTL compatible). The falling edge of this output indicates the beginning of a new field of video. VRESET* is output following the rising edge of CLOCKx1. |
| HACTIVE* | Horizontal blanking output (TTL compatible). The falling edge of HACTIVE* indicates the beginning of active video in a line (even in the vertical interval) and occurs HDELAY clocks (at the $f_{DESIRED\_HCLOCK}$ rate) after the falling edge of HRESET*. HACTIVE* is output following the rising edge of CLOCKx1. |
| VACTIVE* | Vertical blanking output (TTL compatible). The falling edge of VACTIVE* indicates the beginning of the active video lines in a field. This occurs VDELAY/2 lines after the rising edge of VRESET*. The rising edge of VACTIVE* indicates the end of active video lines and occurs ACTIVE_LINES/2 lines after the falling edge of VACTIVE*. Refer to Table 5 for details. VACTIVE* is output following the rising edge of CLOCKx1. |
| ACTIVE | Composite active output (TTL compatible). This output is a logical zero during the horizontal and vertical blanking intervals. ACTIVE is output following the rising edge of CLOCKx1. |
| FIELD_EVEN, FIELD_0, FIELD_1 | Field outputs (TTL compatible). These outputs indicate which field is currently being digitized. They are output following the rising edge of CLOCKx1. |
| CAPTURE | Capture control output (TTL compatible). This output is command bit CR7_6 or CR7_7 synchronized to the VRESET* and the FIELD_EVEN signal. It is output following the rising edge of CLOCKx1. |
| R0–R7, G0–G7, B0–B7 | Digitized video data outputs (TTL compatible). They are output following the rising edge of CLOCKx1. R0, G0, and B0 are the least significant bits. |
| VTU_EN* | Video timing enable pin (input). By asserting a logical one on this pin, the video timing unit outputs (CbFLAG*, HRESET*, VRESET*, HACTIVE*, VACTIVE*, VALID, ACTIVE, FIELD_EVEN, FIELD_0, FIELD_1, and CAPTURE) are three-stated. Writing to CR7_2 will also disable these outputs. |
| PIXEL_EN* | Pixel output-enable pin (input). By asserting a logical one on this pin, the pixel outputs (R0–R7, G0–G7, and B0–B7) are three-stated. Writing to CR7_3 will also disable these outputs. |
| VALID | Valid pixel (TTL compatible). This pin is asserted high to indicate a valid output pixel (during active video). It changes state following the rising edge of CLOCKx1. |
| SERROR | Ultralock™ phase information pin for future Brooktree encoders. |

**Table 1. Pin Assignments** *(3 of 3)*

| Pin Name | Description |
|---|---|
| **The Clock Interface** | |
| XTAL1_IN, XTAL1_OUT | Crystal-one pins. A crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XTAL1_IN. CMOS-level inputs must be used. The frequency of the clock source must be at least twice the desired pixel rate. |
| XTAL2_IN, XTAL2_OUT | Crystal-two pins. A crystal may be tied directly to these pins, or a single-ended oscillator may be connected to XTAL2_IN. CMOS-level inputs must be used. The frequency of the clock source must be at least twice the desired pixel rate. |
| CLOCKx1 | 1x clock output (TTL compatible). The frequency of this output is the selected XTAL(1 or 2)_IN frequency divided by 2. |
| CLOCKx2 | 2x clock output (TTL compatible). The output of the selected XTAL(1 or 2)_IN. |
| **The JTAG Interface** | |
| TCK | Test Clock (TTL compatible). Used to synchronize all JTAG test structures. When JTAG operations are not being performed, this pin should be driven to a logical low. After power-up this pin must have a minimum of five rising edges to reset the Bt812. See Power-up Initialization. |
| TMS | Test Mode Select (TTL compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin should be driven to logical high or left floating. |
| TDI | Test Data Input (TTL compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary-scan operation. When JTAG operations are not being performed, this pin should be driven to a logical high or left floating. |
| TDO | Test Data Output (TTL compatible). JTAG output pin used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG operations and will be three-stated at all other times. When JTAG operations are not being performed, this pin should be left floating. |
| **Test Pins** | |
| T0–T15 | Reserved. These are reserved testing pins, and must be left unconnected. |
| **Power and Ground Pins** *(1)* | |
| VDD +5 V | Power supply for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VDD pins and ground, as close to the device as possible. A ferrite bead is used to separate VDD from digital power. |
| VAA +5 V | Power supply for analog circuitry. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and ground, as close to the device as possible. A ferrite bead is used to separate VAA from digital power. |
| GND Ground | Ground for digital circuitry. All GND pins must be connected together as close to the device as possible. |
| GNDA Ground | Ground for analog circuitry. All GNDA pins must be connected together as close to the device as possible. |
| Notes: (1). Please refer to the PCB Layout Considerations section. | |

**Figure 1. Pinout Diagram**



## MPU Interface

As illustrated in Figure 2, the Bt812 supports a standard MPU bus interface.

The RS0 and RS1 register select inputs specify whether the MPU is accessing the address register or control registers, as specified in Tables 2 and 3. ADDR0 corresponds to D0 and is the least significant bit.

When the control registers are accessed, the address register resets to $00 following a read or a write cycle to address $FF. A data write cycle to address $FF resets the device. MPU write cycles to reserved locations may cause undefined behavior and should not be attempted. MPU read cycles from reserved locations return undefined values. The ($) preceding the address refers to a hexadecimal number.

The MPU interface operates asynchronously to the pixel clock.

### Writing Control Register Data

To write control register data, the MPU loads the address register (control register write mode) with the address of the control register to be accessed. The MPU performs a write cycle, using RS0 and RS1 to select the control registers. After the write cycle, the address register ADDR[7:0] then increments to the next location, which the MPU may write by simply writing another byte of data. A block of data in consecutive control registers may be written by writing the start address and performing continuous data write cycles until the entire block has been written.

**Table 2. Control Input Truth Table**

| RS1 | RS0 | Addressed by MPU |
|---|---|---|
| 0 | 0 | Address Register |
| 1 | 1 | Reserved |
| 0 | 1 | Reserved |
| 1 | 0 | Control Registers |

### Reading Control Register Data

To read control register data, the MPU loads the address register (control register read mode) with the address of the control register to be read. The MPU performs a read cycle, using RS0 and RS1 to select the control registers. After the read cycle, the address register (ADDR0–ADDR7) then increments to the next location, which the MPU may read by simply reading another byte of data. A block of data in consecutive control registers may be read by writing the start address and performing continuous read cycles until the entire block has been read.

### Hardware and Software Reset

The device is reset when a logical zero is asserted for a minimum of four consecutive clock cycles on the RESET* pin. The same effect can be achieved by writing to control register $FF.

Upon reset, the device initializes itself for the NTSC square-pixel format. The horizontal loop and subcarrier loop registers are not reset to default values; however, the device may need to reacquire line and subcarrier lock.

### Power-Up Initialization

On power-up, the Bt812 requires resetting of the JTAG circuitry. This requires a minimum of five rising edges on TCK (the JTAG clock pin) after power-up. TMS (the JTAG control pin) must be left floating or tied high during these edge transitions. This will guarantee the Bt812 has been completely reset. For full details please refer to JTAG Initialization in the JTAG Information section of this document.

### Power-Down Mode

The device is placed in power-down mode when (1) is written to command register bit CR4_7. In the power-down mode, internal circuits are disabled to minimize power consumption. MPU register values are retained, and they remain accessible through the MPU interface. The outputs are not three-stated automatically, but may be three-stated by driving VTU_ENABLE*, PIXEL_ENABLE* high, or writing to CR7_2 or CR7_3.

The Bt812 becomes operational approximately 1 second after the power-down mode is disabled.

**Figure 2. Detailed Block Diagram**

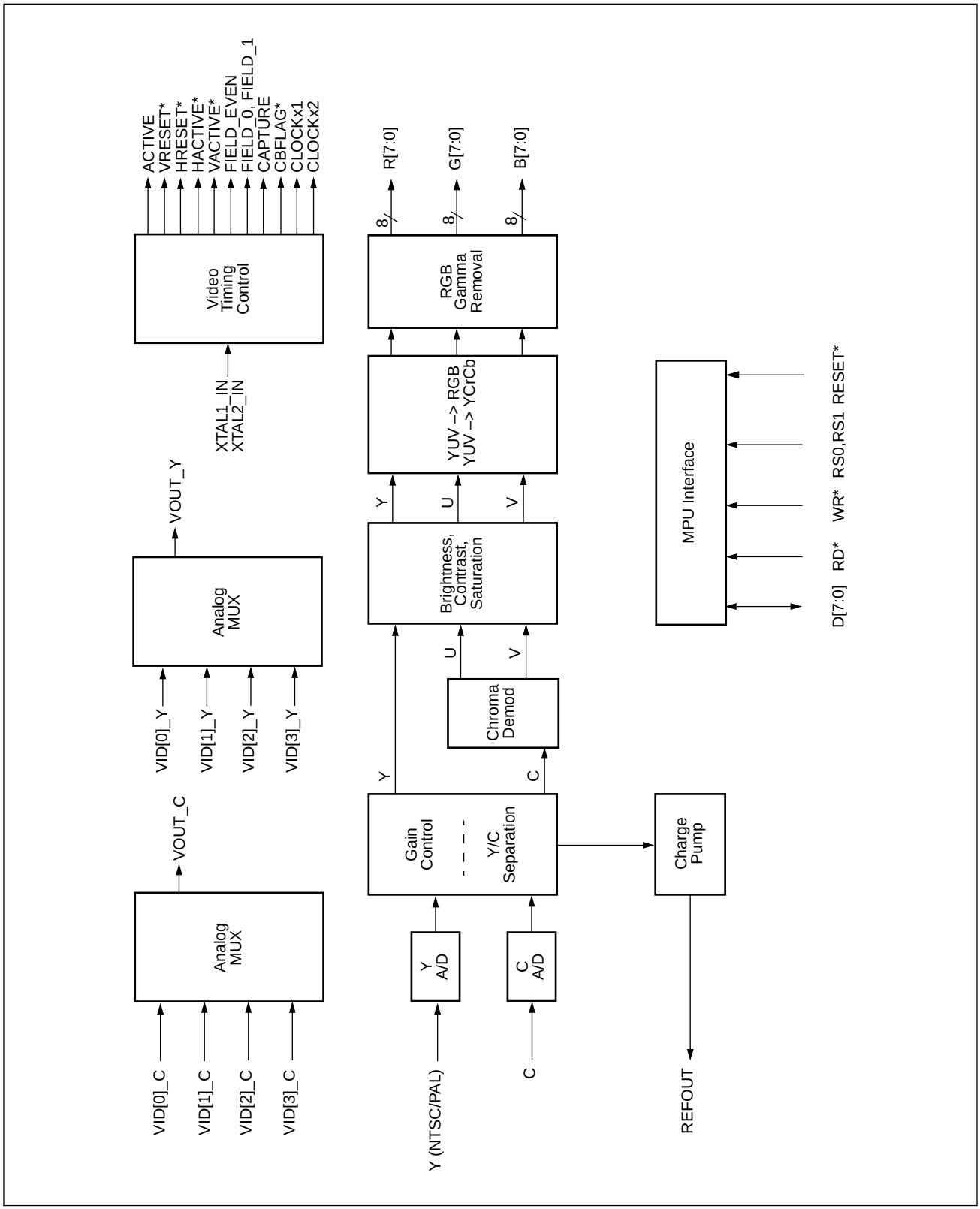


**Table 3. Address Register (ADDR) Operation**

| | Value | RS1 | RS0 | Addressed by MPU |
|---|---|---|---|---|
| ADDR_0–7 (Counts Binary) | $00 | 1 | 0 | Command Register 0, Input Select Register |
| | $01 | 1 | 0 | Reserved |
| | $02 | 1 | 0 | Command Register 2, Status Register |
| | $03 | 1 | 0 | Command Register 3, Output Format Register |
| | $04 | 1 | 0 | Command Register 4, Operation Mode Select Register |
| | $05 | 1 | 0 | Command Register 5, Input Format Register |
| | $06 | 1 | 0 | Command Register 6, Clock Definition Register |
| | $07 | 1 | 0 | Command Register 7, Video Timing Definition Register |
| | $08 | 1 | 0 | Brightness Adjust Register |
| | $09 | 1 | 0 | Contrast Adjust Register |
| | $0A | 1 | 0 | Saturation Adjust Register |
| | $0B | 1 | 0 | Hue Adjust Register |
| | $0C | 1 | 0 | HCLOCK Low Register |
| | $0D | 1 | 0 | HCLOCK High Register |
| | $0E | 1 | 0 | HDELAY Low Register |
| | $0F | 1 | 0 | HDELAY High Register |
| | $10 | 1 | 0 | ACTIVE_PIXELS Low Register |
| | $11 | 1 | 0 | ACTIVE_PIXELS High Register |
| | $12 | 1 | 0 | VDELAY Low Register |
| | $13 | 1 | 0 | VDELAY High Register |
| | $14 | 1 | 0 | ACTIVE_LINES Low Register |
| | $15 | 1 | 0 | ACTIVE_LINES High Register |
| | $16 | 1 | 0 | P (subcarrier freq) Register 0 |
| | $17 | 1 | 0 | P (subcarrier freq) Register 1 |
| | $18 | 1 | 0 | P (subcarrier freq) Register 2 |
| | $19 | 1 | 0 | AGC Delay Register |
| | $1A | 1 | 0 | Burst Delay Register |
| | $1B | 1 | 0 | Sample Rate Conversion Low Register |
| | $1C | 1 | 0 | Sample Rate Conversion High Register |
| | $1D | 1 | 0 | Command Register 1D, Video Timing Polarity Register |
| | $1E:$FE | 1 | 0 | Reserved |
| | $FF | 1 | 0 | Software Reset |

Note: The ($) refers to a hexadecimal number.

# Video Inputs

## Analog Signal Selection

The Bt812 supports four analog input sources: VID[3:0]. These inputs can be connected to two 4:1 multiplexers. The selected sources are output onto pins VOUT_Y and VOUT_C. The selection is made through command register bits CR0_7 through CR0_3.

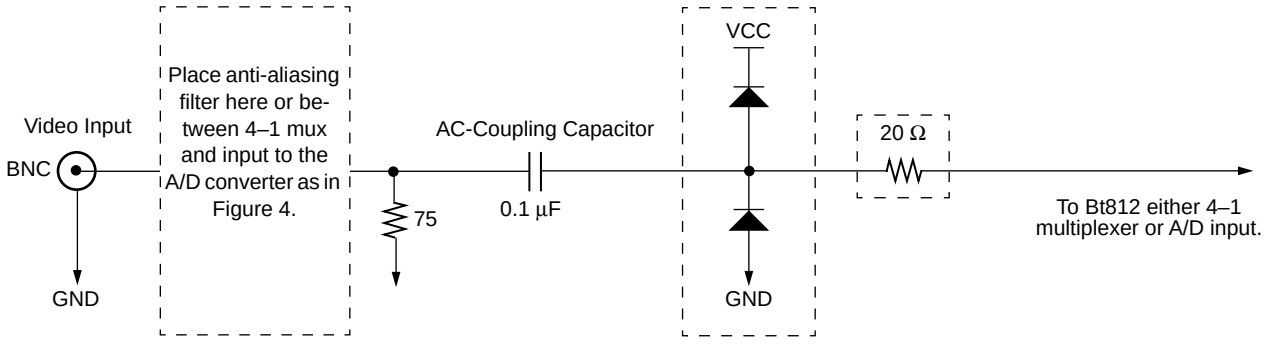
VOUT_Y and VOUT_C may be connected directly to the A/D inputs (Y/Composite and C, respectively) if no filtering or gain of the video signal is required. Sync information (if present) will still be present on VOUT_Y and VOUT_C.

## Multiplexer Considerations

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

The multiplexers cannot be switched on a real-time pixel-by-pixel basis. If additional ESD protection is required, diodes and series resistance may be added to the input circuit (see Figure 3).

**Figure 3. Additional ESD Protection**




Note: Suggested diodes: Hewlett Packard 5082-2305.

### Flash Analog-to-Digital Converters

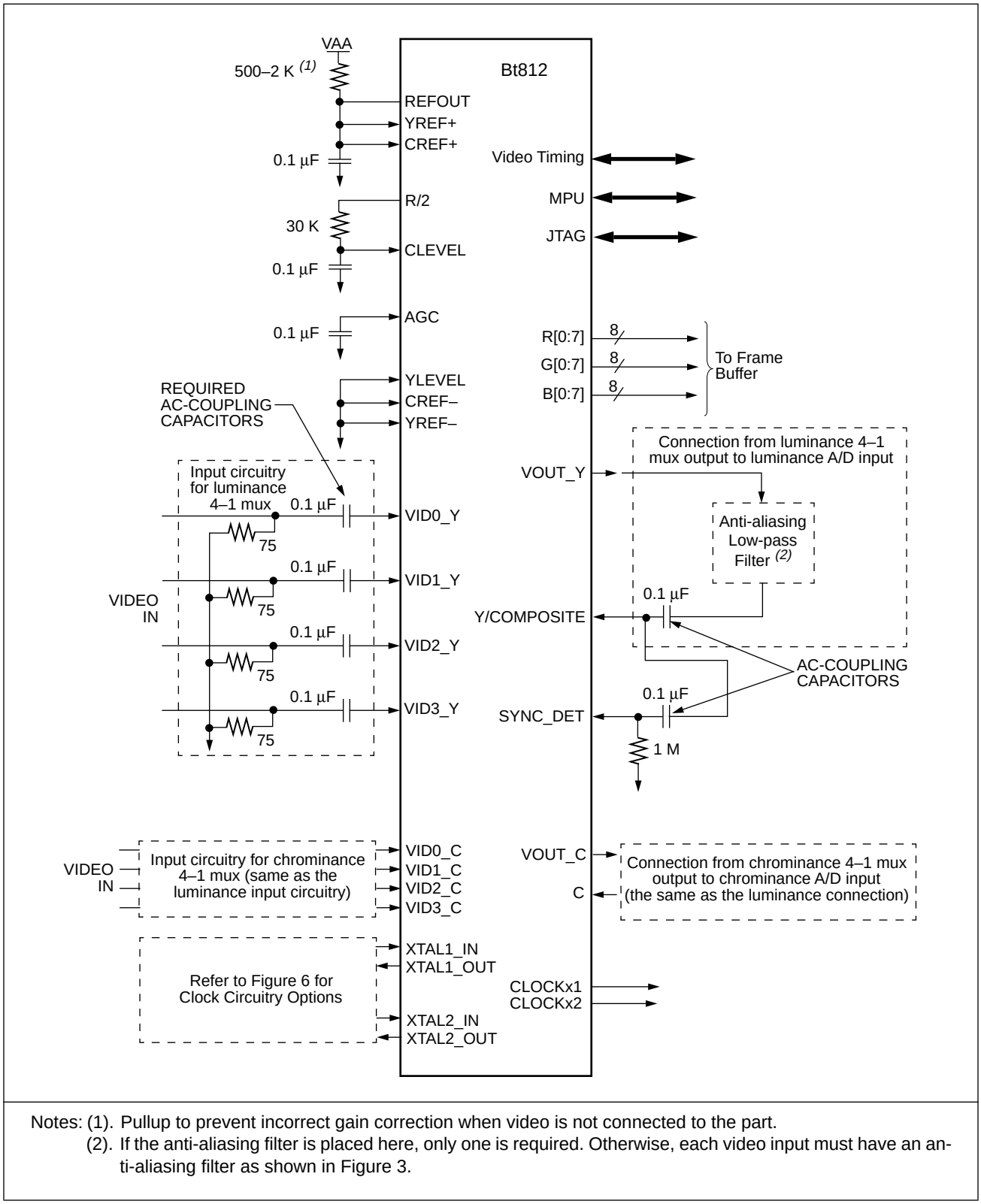
The Bt812 uses two 8-bit flash Analog-to-Digital Converters (ADCs) to digitize the video signals. Each ADC digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+). Video signals with a peak amplitude of 0.7–2 V can be decoded by the Bt812. For video signals with a peak amplitude less than 1 V, as the peak amplitude decreases, the video quality decreases accordingly. The input signal should be band limited to 6 MHz for anti-aliasing purposes.

REF+ voltage levels are controlled by the automatic gain control (AGC) circuitry within the Bt812, as shown in Figure 4. If the Y/composite video-signal amplitude exceeds the YREF+ voltage level, command bit CR2_5 is set to a logical one. If the C video-signal amplitude exceeds the CREF+ voltage level, command bit CR2_4 is set to a logical one. This could occur in automatic gain control mode if the video momentarily exceeds the corresponding REF+ voltage.

### A/D Clamping

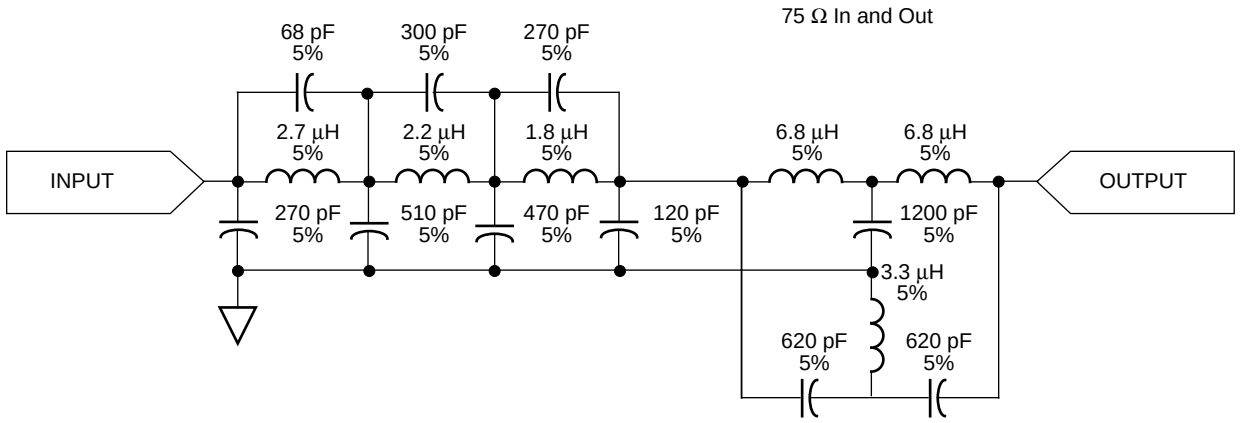
An internally generated CLAMP control signal is used to clamp the inputs of the A/D converters for DC restoration of the video signals. Clamping for both the Y and C analog inputs occurs within the horizontal sync tip. The Y/composite and C inputs are always DC restored to YLEVEL and CLEVEL, respectively. External clamping is not required as internal clamping is automatically performed.

**Figure 4. Typical External Circuitry**




Notes: (1). Pullup to prevent incorrect gain correction when video is not connected to the part.
(2). If the anti-aliasing filter is placed here, only one is required. Otherwise, each video input must have an anti-aliasing filter as shown in Figure 3.

**Figure 5. Cauer-Chebychev 7-Pole Anti-aliasing Filter, Optimized for both NTSC and PAL Video**




Note: Used on Bt812 Evaluation Module.

## VIN Input Considerations

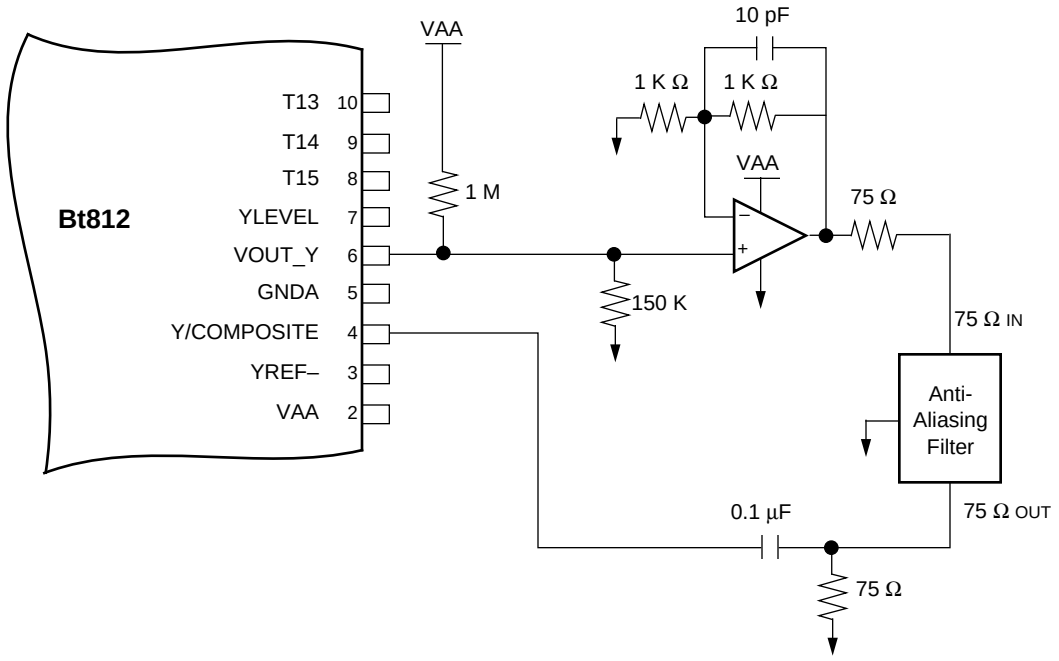
Analog filtering is suggested in order to avoid aliasing. The filter can be placed at the input to the 4–1 multiplexer or between the multiplexer and the input to the A/D converters. Figure 5 is an example of a filter that will preserve signal fidelity of the input video.

When implementing an anti-aliasing filter between the output of the 4–1 multiplexer and the input to the A/D, impedances must be matched in order to minimize signal reflections. To ensure proper signal termination it is recommended that an op-amp be used between the output of the multiplexer and the input to the filter. Figure 6 shows this configuration. When the anti-aliasing filter is implemented at the input to the multiplexer this op amp is not needed, as shown in Figure 3.

## Automatic Gain Controls

When the REFOUT, YREF+ and CREF+ pins are connected together as shown in Figure 4, the Bt812 automatically controls the voltage level for the top of the reference ladder for each ADC. The automatic composite gain control adjusts the YREF+ and CREF+ voltage levels until the back porch of the Y video input generates a digital code 56 from the ADC. The automatic composite gain control may be disabled by command bit CR4_5. If the AGC is disabled an external reference must be provided. This is useful if there is no relationship between the sync height and the active video signal amplitude.

**Figure 6. Suggested Configuration when Filter is Implemented Between 4–1 Multiplexer and A/D**




Notes: 1. Suggested op amp: Elantec EL2044.
2. 10 pF is layout dependent and may or may not be necessary.
3. When using the opamp with –5 volt and +5 volt supplies, this 1 M Ω resistor is not needed.
4. For video signals with peak voltage greater than 1 volt, the ± 5 volt configuration must be used.

# Color Processing

### Hue Adjustment

The hue may be adjusted through the Hue-Adjust Register. Hue adjustments may be in the range –45 to +44.3 degrees, in increments of 0.7 degree. The hue adjustment is implemented by adjusting the color subcarrier phase during active video. Hue adjustment should be set to 0 degree when PAL video signals are decoded. A nonzero value for this register will result in line-to-line hue shifts when PAL formats are decoded.

### Contrast, Brightness, and Saturation

The Bt812 provides MPU-programmable brightness, contrast, saturation and hue registers.

### Low Color Detection and Removal

If a color burst of 25 percent (NTSC) or 35 percent (PAL) or less of the nominal amplitude is detected for 127 consecutive scan lines, the color-difference signals U and V are set to zero. When the low color detection is active, the reduced chrominance signal is still separated from the composite signal to generate the luminance portion of the signal. If YCrCb data is generated, the resulting Cr and Cb values are 128. If RGB data is generated, the resulting R, G, and B values are the same, which produces gray-scale video rather than color. Output of the chrominance signal is re-enabled when a color burst of 43 percent (NTSC) or 60 percent (PAL) or greater of nominal amplitude is detected for 127 consecutive scan lines.

Low color detection and removal may be disabled by setting CR4_3 to a logical one.

### Automatic Chrominance Gain Control

The automatic chrominance gain control compensates for reduced chrominance and color-burst amplitudes caused by, for example, high-frequency loss in cabling. Here, the color-burst amplitude is calculated and compared to nominal. The color-difference signals are then increased or decreased in amplitude according to the color-burst amplitude difference from nominal.

The maximum amount of chrominance gain is 0.5–2 times the original amplitude. This compensation coefficient is then multiplied by the value in the Saturation Adjust Register for a total chrominance gain range of 0–2 times the original signal.

Automatic chrominance gain control may be disabled by setting CR4_4 to a logical one.

## Gamma Correction Circuitry

Circuitry is provided to optionally remove gamma correction (nominally, 2.2 for NTSC and 2.8 for PAL) when RGB data is output. When YCrCb data is output, the circuitry should be bypassed (with no change in the pipeline delay). If this circuitry is not bypassed in this mode, the Bt812 will perform a gamma translation on YCrCb data (see Table 4).

RGB data with the gamma correction removed, (linear RGB), may be generated by setting command register bits CR3_4 and CR3_3 to the appropriate value. Either of the three gamma values may be chosen regardless of the input video format.

**Table 4. Programming the Command Register for Gamma Removal**

| Gamma Removal Type | CR3_4 | CR3_3 |
|---|---|---|
| No Gamma Removal | 0 | 0 |
| Remove Gamma Correction of 2.2 | 0 | 1 |
| Remove Gamma Correction of 2.8 | 1 | 0 |
| Reserved | 1 | 1 |

## Color Output Modes

The Bt812 outputs several modes of color information, as shown in Table 10 (in the Internal Registers section).

### 16-bit YCrCb Output Data Format

When 16-bit YCrCb data is output, a multiplexer decimates the CrCb data to generate 4:2:2 YCrCb data.

The CbFLAG* output is used to specify whether Cr or Cb data is being output onto the blue channel. While CbFLAG* is a logical zero, Cb data is present. While CbFLAG* is a logical one, Cr data is present. Cb data is output during the first clock cycle after ACTIVE is asserted (indicating active video) if HDELAY is even.

### 24-bit YCrCb Output Data Format

When 24-bit YCrCb data is output, the CbFLAG* output should not be used.

### 15 and 16-bit RGB Output Data Format

When either 15 or 16-bit RGB data is output, rounding is performed on the data.

# Video Timing

## CLOCK Operation

XTAL1_IN and XTAL2_IN can be software-selected to clock the Bt812. Standard CMOS crystals or single-ended CMOS oscillators may be used. The clock source tolerance should be 50 parts-per-million (ppm) or less. Devices that output CMOS voltage levels are required.

It is recommended that 68 pF of capacitance be placed on the XTAL_IN and XTAL_OUT pins when the device is attached to an external crystal. Care must be taken to ensure that the 68 pF includes board parasitic capacitance. In reality, the capacitor values attached should be such that the total capacitance observed between the two crystal connections is about 30 pF. Note that the two 68 pF capacitors in the datasheet are in series as far as the crystal is concerned, and represent a combined capacitance of 34 pF. If parasitic board capacitance is appreciable, the added chip capacitor values should be decreased appropriately. The specifications for the crystal are as follows:

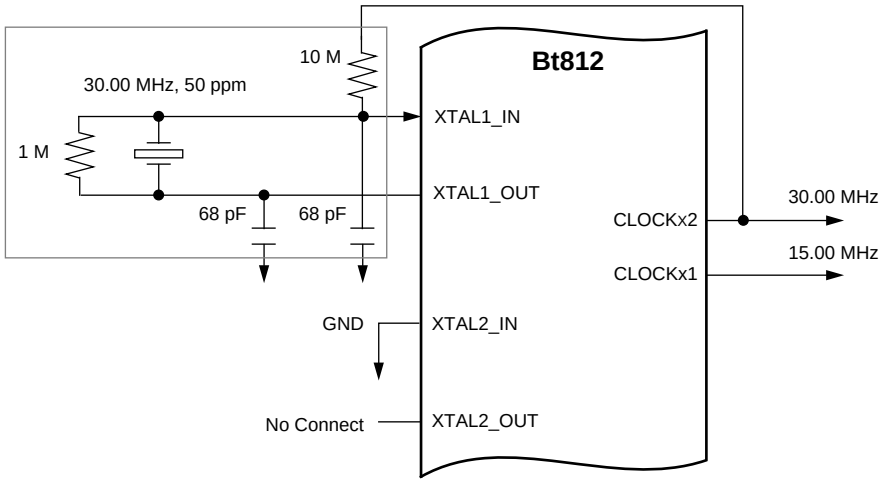
- Fundamental Cut
- Parallel Resonant
- 30 pF Load Tolerant
- 50 ppm Device
- Equivalent Series Resistance (ESR) less than 15 Ω

These can be obtained from several vendors. Brooktree uses General Electronic Devices (619) 591-4170. The GED part number for a 29.5 MHz crystal is PK29.500000-30-005-15R.

## Sample Rate Conversion Operation

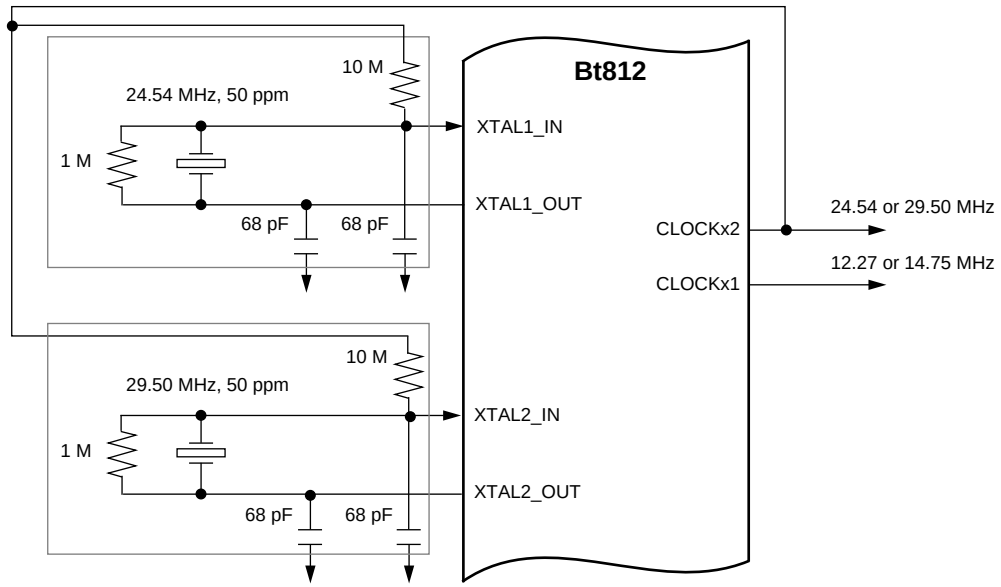
CLOCKx2 and CLOCKx1 are generated and output from the Bt812 to drive external circuitry. CLOCKx2 operates at the XTAL_IN rate (maximum 30 MHz) while CLOCKx1 operates at CLOCKx2/2 (maximum 15 MHz). HCLOCK is the number of clocks per line of video at the frequency, $f_{CLOCKx1}$. DESIRED_HCLOCK is defined as the number of clocks per line of video at the effective sample rate. It is defined by the user and programmed into the Sample Rate Conversion Register. Values from 8/11 to 1 times the HCLOCK are allowed. Thus, the Bt812 will output ACTIVE_PIXELS valid pixels per line of video. See Figures 7 through 10.

**Figure 7. Clock Circuitry Block Diagram, Option 1**



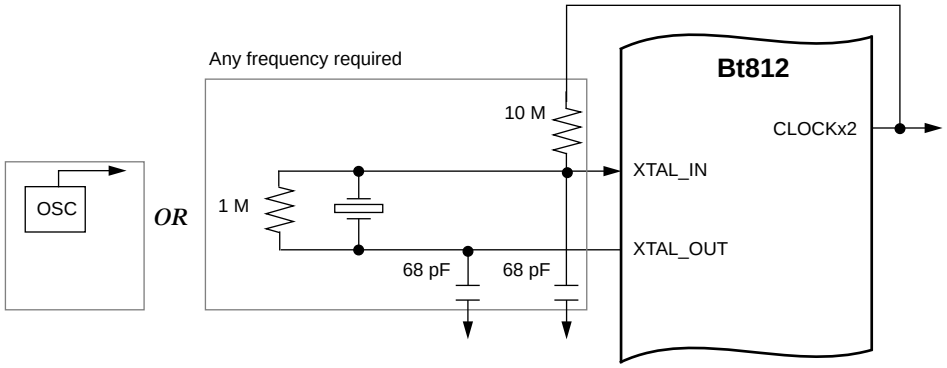

Note: This example demonstrates the use of one clock source to drive the Bt812. CLOCKx2 is the same frequency as the clock source, while CLOCKx1 is 1/2 that frequency. Using this method, Ultralock™ allows the desired pixel rate ($f_{DESIRED\_HCLOCK}$)to be software-programmed to output pixels at any rate between 8 and 15 MHz. This enables operation at both square pixel NTSC and PAL pixel rates with one clock source.

**Figure 8. Clock Circuitry Block Diagram, Option 2**



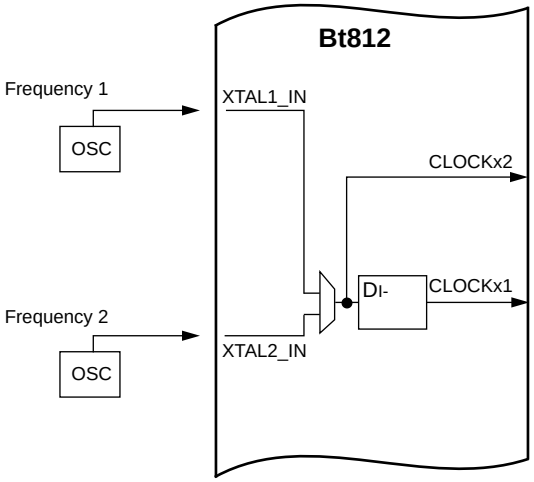

Note: This option is useful when the system clock must be driven at the desired pixel rate. Two clock sources can be software-selected for decoding square pixel NTSC or PAL video.

**Figure 9. Clock Circuitry Block Diagram, Option 3**




Note: Both XTAL ports may be driven with either single-ended oscillators or crystals. (CMOS levels required.)

**Figure 10. Clock Circuitry Block Diagram, Option 4**




Note: Either XTAL1_IN or XTAL2_IN may be software selected to drive internal circuitry. The selected clock source generates CLOCKx2 directly while CLOCKx1 is a divided-down version of the clock source.

### Y/C Separation

The Bt812 performs luma/chroma separation as shown in Figures 11–13b. The composite video signal is demodulated and low pass filtered to generate the chrominance. This signal is then remodulated and subtracted from the delayed composite video to generate the luminance.

### Ultralock™ Operation

An on-chip sync detector is used to determine the position of the horizontal sync pulse for ADC clamping and AGC sampling on the back porch. The input to the sync detector (SYNC_DET) must be AC coupled to the Y input, as shown in Figure 4.

For horizontal and subcarrier locking, Ultralock™ is implemented to ensure locking to stable, unstable, and noisy sources. Ultralock™ implements digital signal processing techniques to interpolate the digitized video to match the expected sample positions of a line-locked clock. The horizontal and vertical sync pulses are detected and used to adaptively generate coefficients for the interpolators. The interpolators implemented provide a flat response for standard video bandwidths. Because the Bt812 interpolation is based on sample points from a stable clock and the actual video line length will vary, a VALID pin is used to indicate when valid pixel data is being output. Because the clock rate into the Bt812 is constant and the video line length can vary, the Bt812 has a pixel buffer for handling horizontal timing errors. This buffer enables the Bt812 to easily support line length errors up to seven clocks in magnitude. This error is defined as the difference between the expected line length and the actual line length measured in clock counts at the frequency $f_{CLOCKx1}$. The expected line length is programmed into the HCLOCK Register. If the video line is longer or shorter than the expected length by seven clocks or less, the operation of VALID and ACTIVE will not change from line to line. This is especially useful when the clock source is driven at exactly twice the $f_{DESIRED\_HCLOCK}$ rate. In the example when XTAL1_IN is driven at 24.54 MHz and $f_{DESIRED\_HCLOCK}$ is 12.27 MHz ($f_{CLOCKx2}$ = 24.54 MHz and $f_{CLOCKx1}$ = 12.27 MHz), as long as the video source has a maximum line length error of seven clocks, the VALID pin outputs exactly the same signal as the ACTIVE pin (Figure 14, Example 1).

In this same example when the line length error from nominal exceeds seven clocks, the Bt812 responds differently depending on whether the video line is shorter or longer than expected. If the video line is longer by more than seven clocks, the decoder will have more clocks per line of video than needed. To account for this the ACTIVE length is extended and the VALID pin is used to indicate when an invalid pixel is being output by the chip. In this case, the same number of active pixels will always be output, but the logical “and” of the ACTIVE and VALID signals should be used to indicate valid pixel data (Figure 14, Example 2).

In the second case, when the video line is shorter than the expected value by more than seven clocks, there will not be enough clocks to output pixel data and the buffer will fill to capacity. At this point, the Bt812 will drop a pixel creating a one-pixel jump in the data. The ACTIVE and VALID signals will remain high during this jump. At the end of the line the Bt812 will continue to process data with the ACTIVE and VALID pins remaining high until the effective number of pixels have been output (Figure 14, Example 3).

Figure 14, Example 4, demonstrates how Ultralock™ handles very short lines. In this example the line of video is approximately 10 percent shorter than the expected length. The VALID and ACTIVE pins indicate valid output data exactly the same as in Figure 14, Example 3. However, when the next line of video is detected (indicated by the falling sync edge), VALID and ACTIVE both are set to a logical low. The effective number of pixels of video during this line is less than that defined in HACTIVE. In this extreme case a small number of pixels on the right side of the image are simply not updated. The benefit is that Ultralock™ is still locking the poor video source to the stable clock. Because Ultralock™ updates the interpolator coefficients continuously while the digitizing clock frequency remains constant, the Bt812 can lock to extremely unstable sources.

The interpolation technique used in the Bt812 enables horizontal scaling. With a stable clock to drive the part, the chip will generate video with a frequency $f_{DESIRED\_HCLOCK}$ that can be programmed to vary from 8/11 to 1 times the frequency $f_{CLOCKx1}$. For systems requiring multiple clock rates, Ultralock™ allows the system to use one clock source for the complete system. For example, if the XTAL1_IN is driven at its maximum speed of 30 MHz, then $f_{CLOCKx2}$ = 30 MHz and $f_{CLOCKx1}$ = 15 MHz; and the $f_{DESIRED\_HCLOCK}$ can be programmed to be between 11 MHz and 15 MHz. Thus, one crystal will provide standard pixel rates of both 12.27 MHz and 14.75 MHz for square pixel NTSC and PAL. For example, with HCLOCK=954 (NTSC) and 960 (PAL), DESIRED_HCLOCK values of 780 pixels/line (NTSC) and 944 pixels/line (PAL) are easily obtained.

In this oversampling mode of operation the difference in frequency between $f_{CLOCKx1}$ and $f_{DESIRED\_HCLOCK}$ requires the use of the VALID pin because each line of video will have more CLOCKx1 clocks than pixel data to output. This is an asset because when the video line is shorter than expected by more than seven clocks (the special case demonstrated in Figure 14, Example 3) there will still be enough CLOCKx1 clocks to output valid data. The Bt812 will fully lock to the highly erroneous source while always generating a constant number of active pixels/line. The magnitude of the line length error will affect how often the VALID pin toggles in the ACTIVE window. In this mode of operation, normally the logical “and” of the VALID and ACTIVE pins will be used to enable writes to memory. See Figure 15.

**Figure 11. Generalized Block Diagram of Bt812 Y/C Separation**

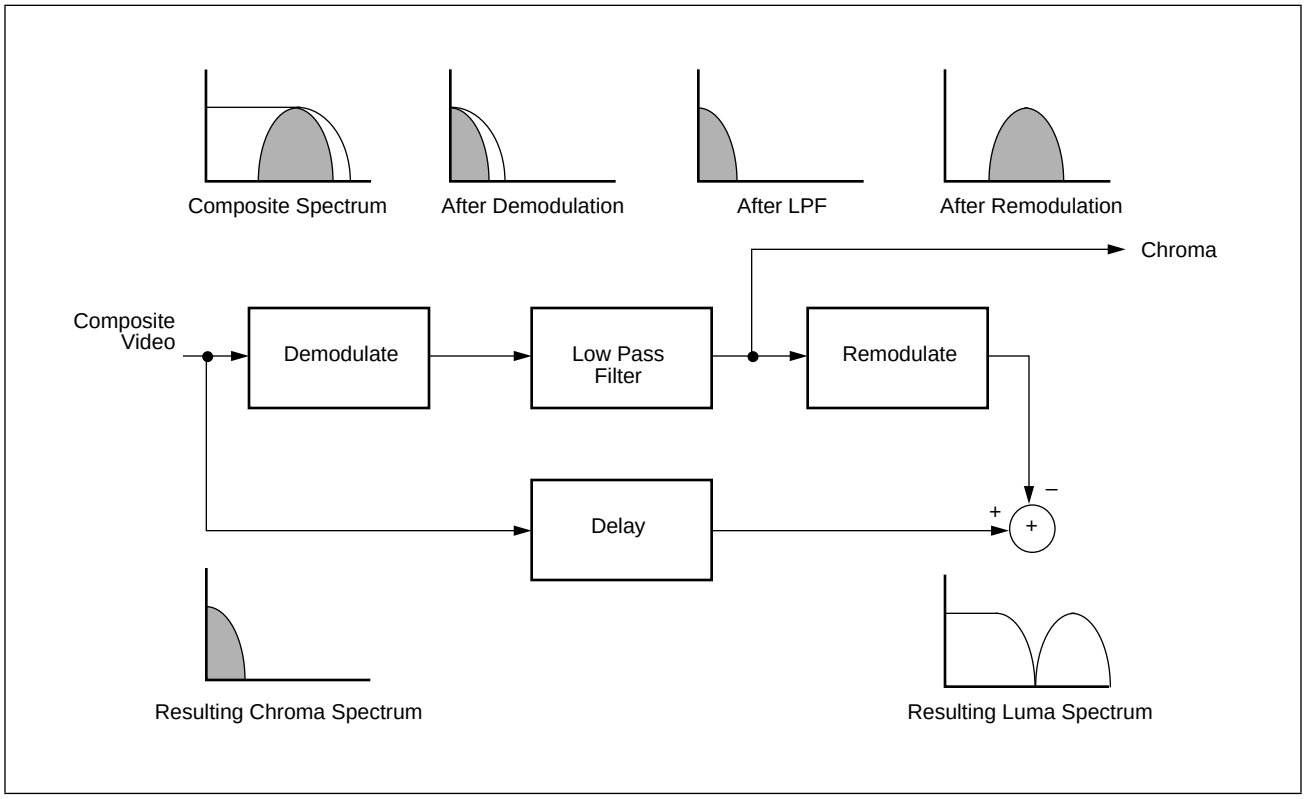



**Figure 12. Bt812 Y/C Separation and Chrominance Demodulation**

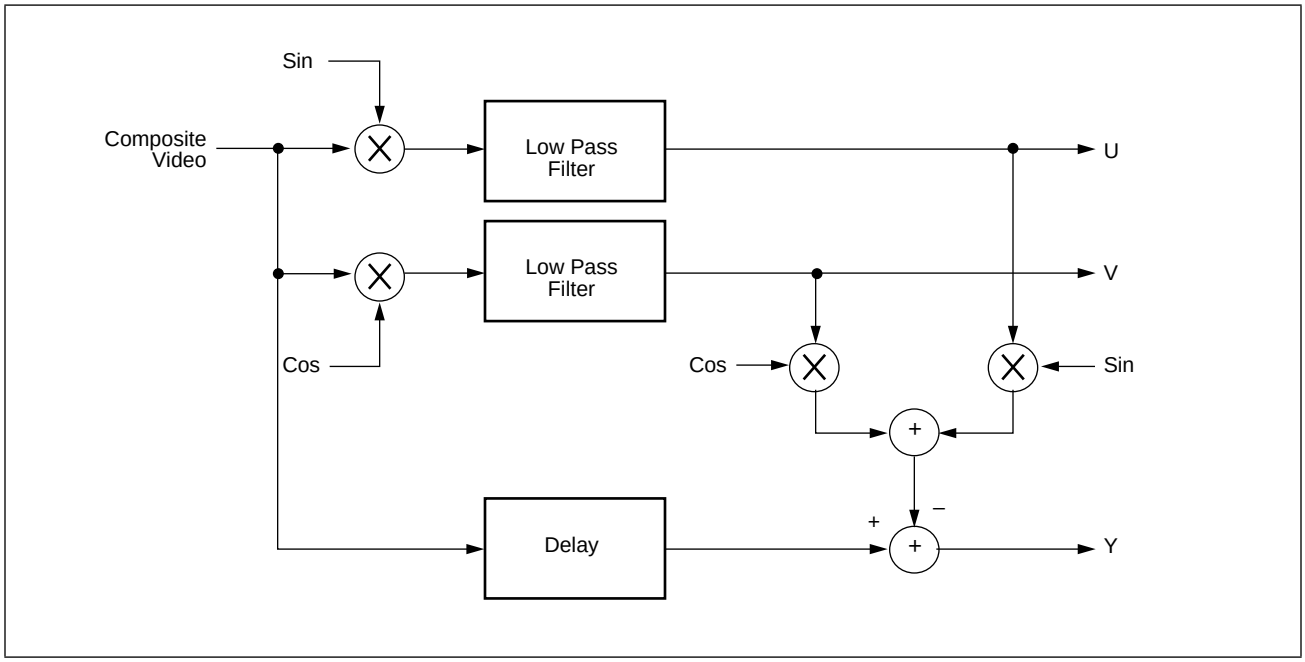
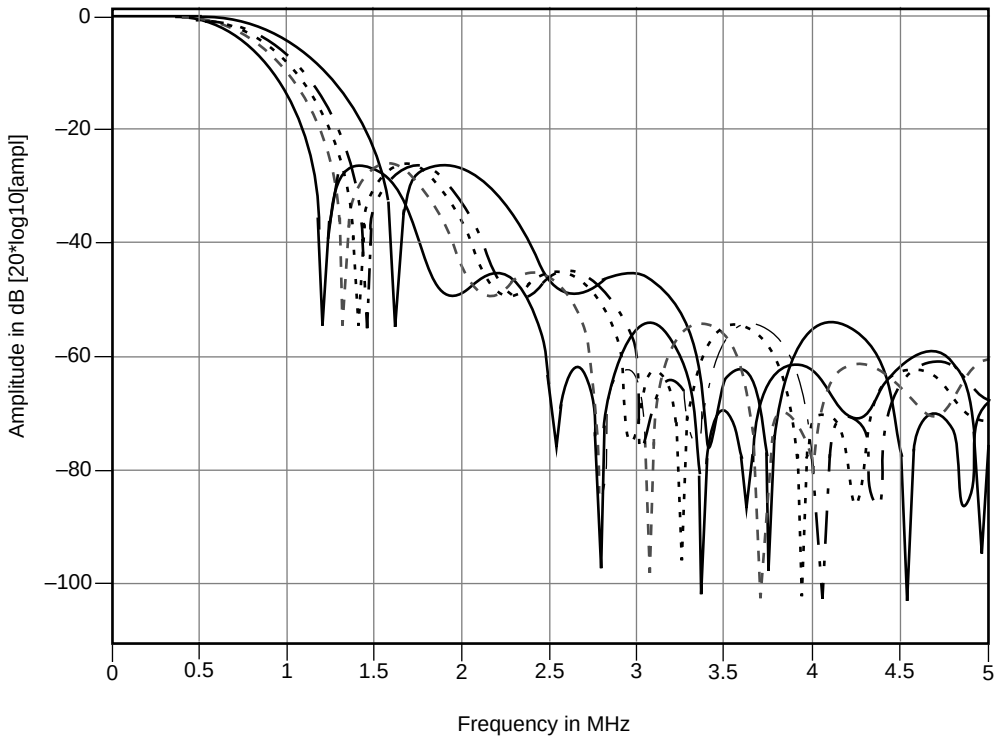
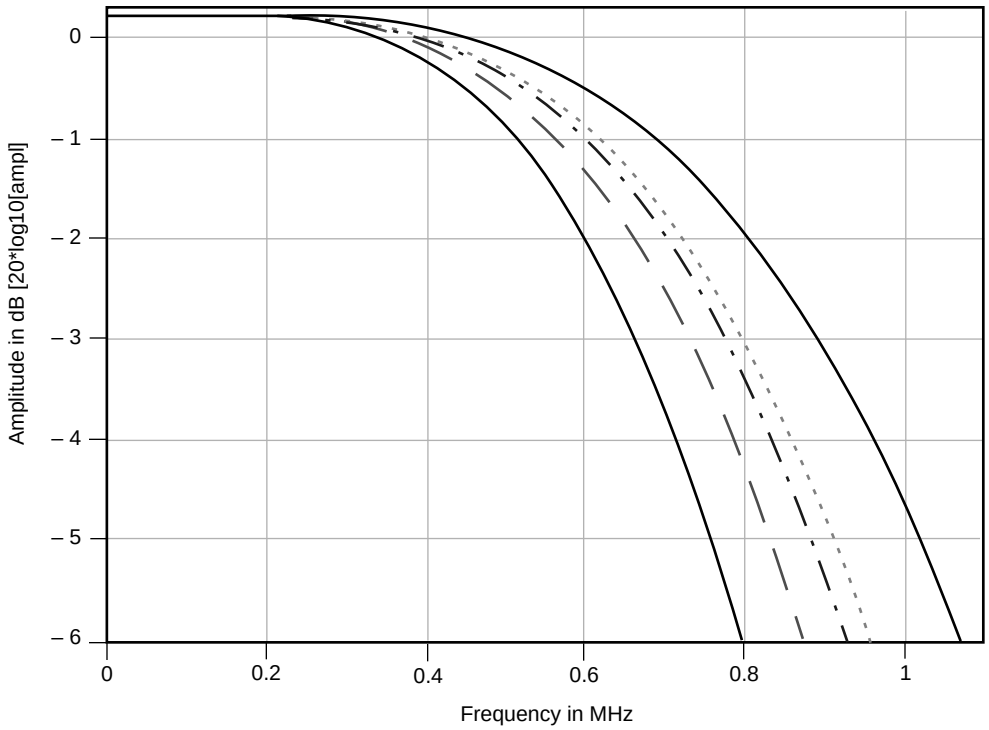


**Figure 13a. Frequency Response of Low Pass Filter Used in Y/C Separation. Stop Band**



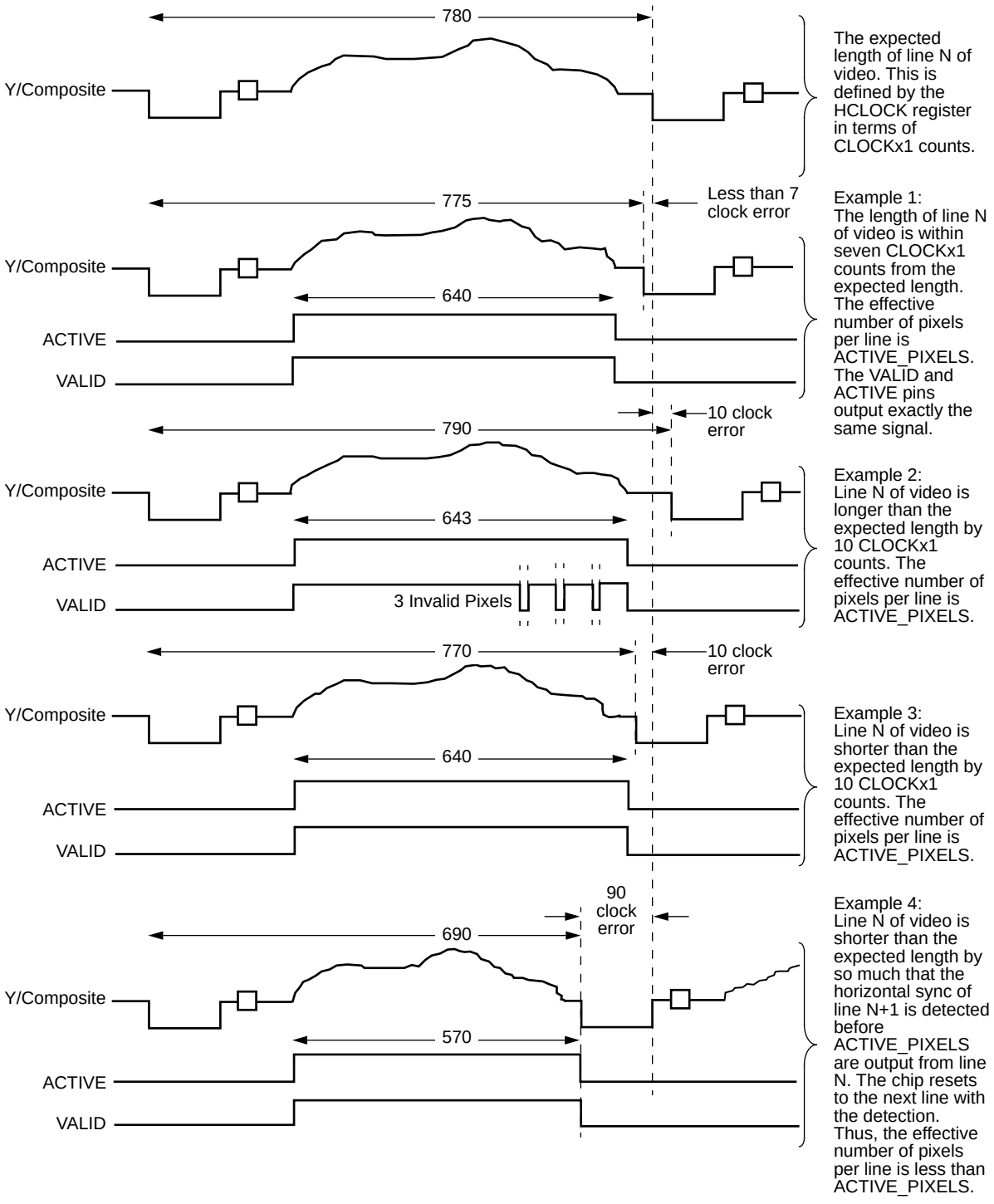

Note: Bt812 Chroma Freq Resp at 12.2727, 13.5, 14.318, 14.75, and 16.5 MHz clock rate, defined by CLOCK x 1.

**Figure 13b. Frequency Response of Low Pass Filter Used in Y/C Separation. Pass Band**



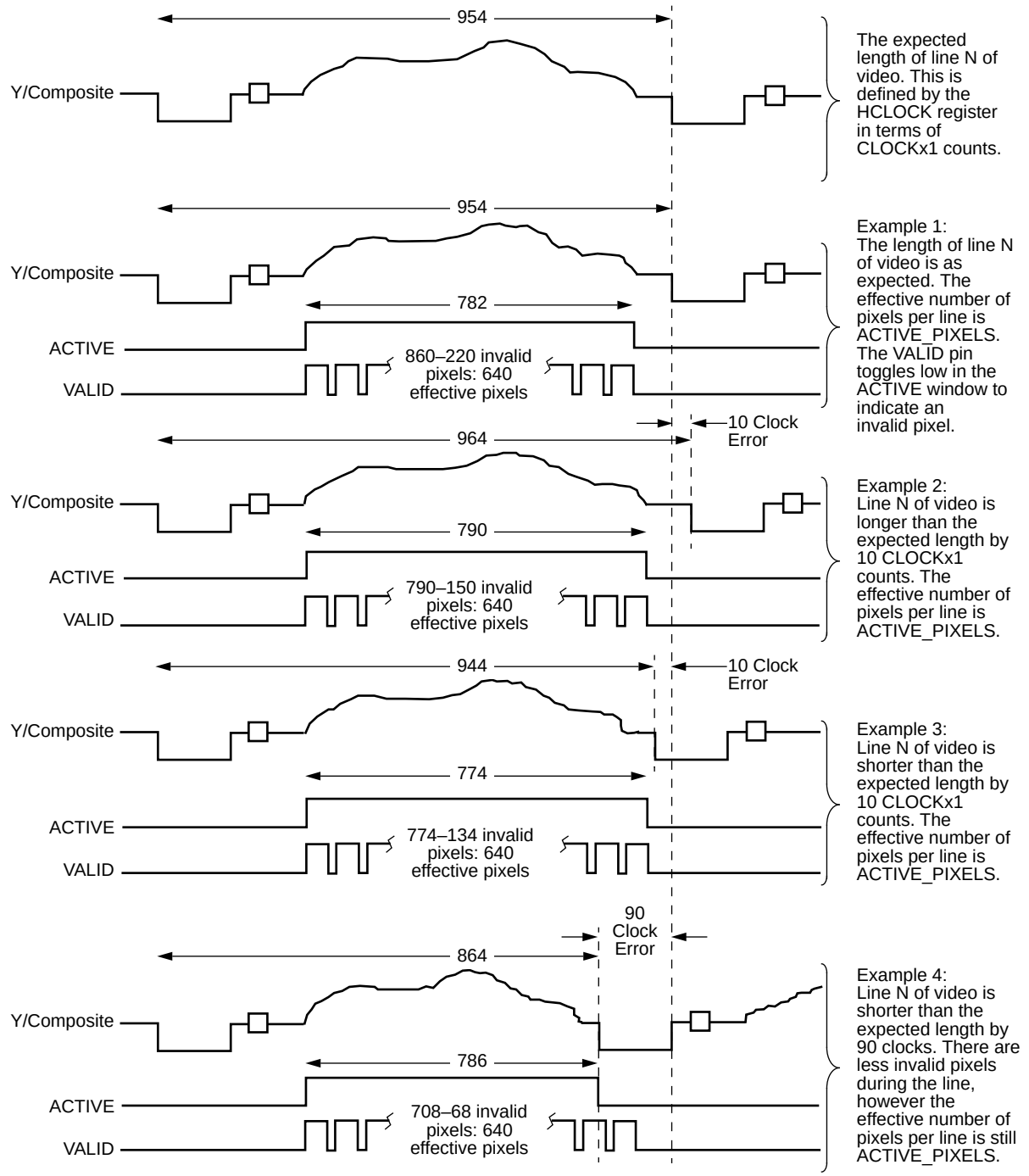

Note: Bt812 Chroma Freq Resp at 12.2727, 13.5, 14.318, 14.75, and 16.5 MHz clock rate, defined by CLOCK x 1.

**Figure 14. Examples of Ultralock™ and Operation of VALID Pin**




Note: The above timing is an example of driving XTAL_IN at Twice the frequency of the effective pixel rate.
$f_{DESIRED\_HCLOCK}$ = fCLOCKx1 = 1/2 X fCLOCKx2

**Figure 15. Examples of Ultralock™ and Operation of VALID Pin**




Note: The above timing is an example of $f_{DESIRED\_HCLOCK}$ = 12.27 MHz; $f_{CLOCKx1}$ = 15 MHz.

### HRESET* Generation

HRESET* is output following the rising edge of CLOCKx1. The falling edge of HRESET* indicates the beginning of a new scan line of video output. The width of the HRESET* active low pulse is 64 clock cycles. See Figure 16. Please note that for stable inputs, Ultralock™ guarantees the time between falling edges of HRESET* only to within one pixel. However, the time between HRESET*, the rise of ACTIVE, and the fall of ACTIVE will remain constant.

### VRESET* Generation

VRESET* is output following the rising edge of CLOCKx1. The falling edge of VRESET* indicates the beginning of a new field of video output. The width of the VRESET* active low pulse is six scan lines.

The falling edge of VRESET* follows the falling edge of HRESET* by one clock at the start of odd fields (fields 1 and 3 for NTSC; and fields 1, 3, 5, and 7 for PAL). At the start of even fields (fields 2 and 4 for NTSC; and fields 2, 4, 6, and 8 for PAL), the falling edge of VRESET* occurs at horizontal count (HCOUNT/2) + 1 on scan line 263 for NTSC and scan line 313 for PAL.

### Horizontal (HACTIVE*) Generation

HACTIVE* is output following the rising edge of CLOCKx1. The falling edge of HACTIVE* indicates the beginning of active video in a line (even in the vertical blanking interval) and occurs HDELAY clocks after the falling edge of HRESET*. The value in the HDELAY register is measured in terms of the frequency $f_{DESIRED\_HCLOCK}$.

### Vertical (VACTIVE*) Generation

VACTIVE* is output following the rising edge of CLOCKx1, and changes state synchronously with the falling edge of HRESET*. The falling edge of VACTIVE* indicates the beginning of the active video lines in a field. If VDELAY is even, the falling edge of VACTIVE* occurs VDELAY/2 lines after the rising edge of VRESET* in the odd fields (1,3,5,7) and (VDELAY/2+1)/2 lines after the rising edge of VRESET* in the even fields (2,4,6,8).

The rising edge of VACTIVE* indicates the end of the active video lines in a field. If ACTIVE_LINES is even, the rising edge of VACTIVE* occurs ACTIVE_LINES/2 lines after the falling edge of VACTIVE* in both even and odd fields. If ACTIVE_LINES is odd and VDELAY is even, the rising edge of VACTIVE* occurs (ACTIVE_LINES+1)/2 lines after the falling edge of VACTIVE* in the odd fields (1,3,5,7), and (ACTIVE_LINES–1)/2 lines after the falling edge of VACTIVE* in the even fields (2,4,6,8). If ACTIVE_LINES is odd and VDELAY is odd, the rising edge of VACTIVE* occurs (ACTIVE_LINES–1)/2 lines after the falling edge of VACTIVE* in the odd fields (1,3,5,7), and (ACTIVE_LINES+1)/2 lines after the falling edge of VACTIVE* in the even fields (2,4,6,8).

Thus, if VDELAY is even, the first line of active video in the odd fields (1,3,5,7) will become the first line of a de-interlaced captured frame, and the first line of active video in the even fields (2,4,6,8) will become the second line of a de-interlaced captured frame. Likewise, if VDELAY is odd, the first line of active video in the odd fields (1,3,5,7) will become the second line of a de-interlaced captured frame,

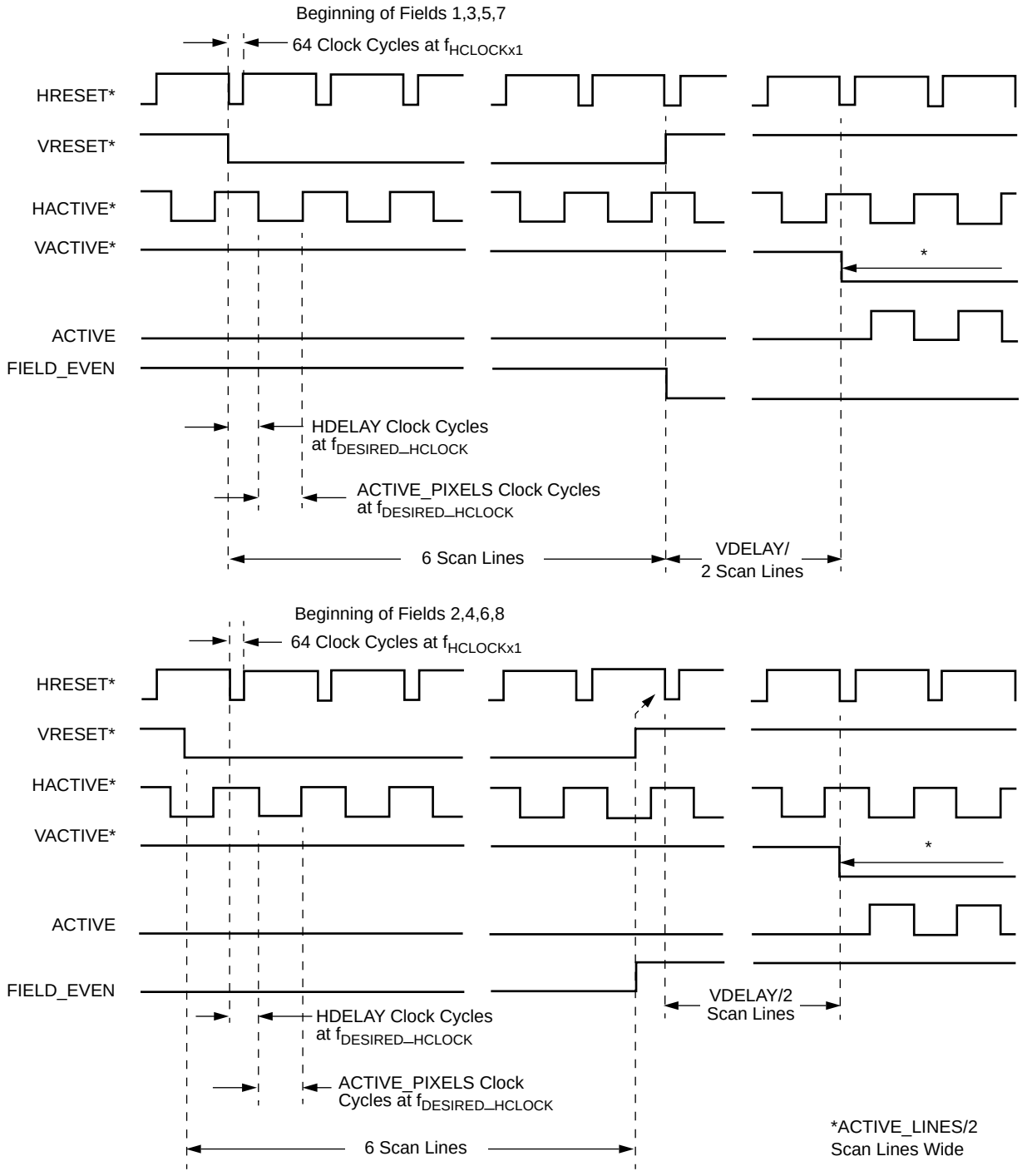
and the first line of active video in the even fields (2,4,6,8) will become the first line of a de-interlaced captured frame.

Similarly, if ACTIVE_LINES is odd, the "extra" line in the de-interlaced captured frame will be captured from the same interlaced field that contained the first line in that de-interlaced captured frame. See Figure 16 and Table 5.

### ACTIVE Generation

ACTIVE is the logical NOR of the HACTIVE* and VACTIVE* signals, and is output following the rising edge of CLOCKx1. The rising edge of ACTIVE indicates the beginning of active video, and the falling edge indicates the end of active video.

**Figure 16. VTU Timing**




Note: The polatiry of the output signals above (both even and odd fields) assume the Video Timing Polarity Register (address $1D) is programmed with $30.

**Table 5. Relationship Between Even and Odd Values of ACTIVE_LINES and VDELAY and the Number of Lines Between VRESET* Rise and VACTIVE* Fall**

| | | Number of Lines Between VRESET* Rise and VACTIVE* Fall | | Number of Lines Between VACTIVE* Fall and VACTIVE* Rise | |
|---|---|---|---|---|---|
| **VDELAY** | **ACTIVE_LINES** | **Odd Fields** | **Even Fields** | **Odd Fields** | **Even Fields** |
| Even | Even | VDELAY/2 | (VDELAY + 1)/2 | ACTIVE_LINES/2 | ACTIVE_LINES/2 |
| Even | Odd | VDELAY/2 | (VDELAY + 1)/2 | (ACTIVE_LINES + 1)/2 | (ACTIVE_LINES –1)/2 |
| Odd | Even | (VDELAY + 1)/2 | VDELAY/2 | ACTIVE_LINES/2 | ACTIVE_LINES/2 |
| Odd | Odd | (VDELAY + 1)/2 | VDELAY/2 | (ACTIVE_LINES –1)/2 | (ACTIVE_LINES + 1)/2 |

## FIELD_1, FIELD_0, and FIELD_EVEN Outputs

FIELD_1, FIELD_0, and FIELD_EVEN outputs change state following the rising edge of CLOCKx1 at the start of a new field. FIELD_EVEN is determined by the relationship between VRESET* and HRESET*. During NTSC operation, the FIELD_0 and FIELD_EVEN outputs indicate which of the four fields is being output. In NTSC mode, FIELD_1 output is driven but carries no valid information.

**Table 6. NTSC Field Identification When SC/H is Valid**

| FIELD_1 | FIELD_0 | FIELD_EVEN | Field |
|---|---|---|---|
| x | 0 | 0 | 1 |
| x | 0 | 1 | 2 |
| x | 1 | 0 | 3 |
| x | 1 | 1 | 4 |

If the input video source is stable (the subcarrier to the falling edge of Hsync has a defined relationship, i.e., SC/H phase is valid), the FIELD_0 signal is determined by monitoring the burst phase. If the SC/H phase is not valid, FIELD_0 signal cannot be accurately derived by monitoring the burst phase. Instead, FIELD_EVEN is divided by 2 and output onto the FIELD_0 pin. In this case, FIELD_0 cannot be used to determine uniquely which field is being output.

**Table 7. NTSC Field Identification When SC/H is Invalid**

| FIELD_1 | FIELD_0 | FIELD_EVEN | Field |
|---|---|---|---|
| x | 0 | 0 | 1 or 3 |
| x | 0 | 1 | 2 or 4 |
| x | 1 | 0 | 3 or 1 |
| x | 1 | 1 | 4 or 2 |

During PAL operation, the FIELD_1, FIELD_0, and FIELD_EVEN outputs indicate which of the possible eight fields is being output. If the input video source is not stable (i.e., the Subcarrier Horizontal (SC/H) phase relationship is not valid), the FIELD_0 and FIELD_1 signals cannot be accurately derived by monitoring the burst phase.

**Table 8. PAL Field Identification When SC/H is Valid**

| FIELD_1 | FIELD_0 | FIELD_EVEN | Field |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

Instead, the FIELD_EVEN signal is divided by 2 and output onto the FIELD_0 pin and divided by 4 and output onto the FIELD_1 pin. In this instance, the FIELD_0 and FIELD_1 signals cannot be used to uniquely determine which field is being output. Thus, if either the FIELD_EVEN signal or the HRESET* and VRESET* timing relationship is used in conjunction with FIELD_0 and FIELD_1, eight fields are identified but only with odd-field and even-field resolution.

Both FIELD_1 and FIELD_0 output timings are coincident with the FIELD_EVEN timing.

**Table 9. PAL Field Identification When SC/H is Invalid**

| FIELD_1 | FIELD_0 | FIELD_EVEN | Field |
|---|---|---|---|
| 0 | 0 | 0 | 1, 3, 5, or 7 |
| 0 | 0 | 1 | 2, 4, 6, or 8 |
| 0 | 1 | 0 | 3, 5, 7, or 1 |
| 0 | 1 | 1 | 4, 6, 8, or 2 |
| 1 | 0 | 0 | 5, 7, 1, or 3 |
| 1 | 0 | 1 | 6, 8, 2, or 4 |
| 1 | 1 | 0 | 7, 1, 3, or 5 |
| 1 | 1 | 1 | 8, 2, 4, or 6 |

### Absence of Video

If a video signal is not present, the Bt812 will continue to generate free-running horizontal and vertical timing information. The absence or presence of video is indicated by CR2_7.

When a video signal is present again, the Bt812 will Ultralock™ to it.

### Capture Output

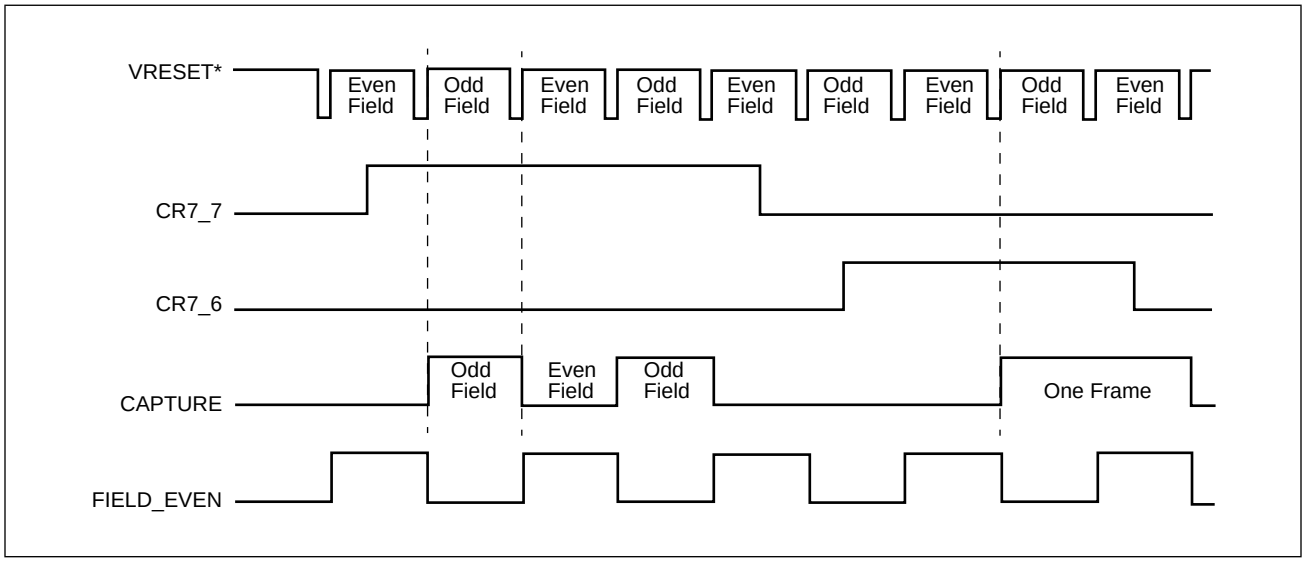
The Bt812 outputs a CAPTURE signal, which is a command register bit (CR7_7 or CR7_6) that is synchronized to the vertical sync, and field or frame intervals. Odd field refers to fields 1 or 3 for NTSC and fields 1, 3, 5, or 7 for PAL.

To capture one or more odd fields, the MPU writes a logical one to command bit CR7_7. At the beginning of the next vertical sync interval, indicating the start of an odd field, CAPTURE is asserted to a logical one. CAPTURE will be a logical one during odd field times (and a logical zero during even field times) while command bit CR7_7 is a logical one. If command bit CR7_7 is a logical zero at the beginning of a vertical sync interval indicating the start of an odd field, CAPTURE will remain a logical zero until either command bit CR7_7 or CR7_6 is again set to a logical one.

To capture one or more frames (a frame comprises two fields), the MPU writes a logical one to command bit CR7_6. At the beginning of the next vertical sync interval, indicating the start of an odd field, CAPTURE is asserted to a logical one. CAPTURE will be a logical one while command bit CR7_6 is a logical one. If command bit CR7_6 is a logical zero at the beginning of vertical sync interval, indicating the start of an odd field, CAPTURE is negated to a logical zero until either command bit CR7_6 or CR7_7 is again set to a logical one.

The value of the CAPTURE pin may be read by the MPU with command bit CR7_4. See Figure 17.

**Figure 17. CAPTURE Output**



# JTAG Information

## Boundary Scan Testability Structures

As the complexity of imaging chips increases, the need to easily access the individual chip for functional verification is becoming vital. The Bt812 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to the IEEE P1149.1 "Standard Test Access Port and Boundary Scan Architecture," the Bt812 has dedicated pins that are used for testability purposes only.

JTAG's approach to testability utilizes boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a boundary-scan register (Figure 18a) which applies or captures test data used for functional verification of the integrated circuit. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), and Test Data Out (TDO). Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these four TAP pins. With boundary-scan cells at each digital pin, the Bt812 has the capability to apply and capture the respective logic levels. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt812 from the other components on the board, the user has easy access to all Bt812 digital pins through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

The Power-On Reset (POR) circuitry ensures that the Bt812 initializes each pin to operate in a video decoder mode instead of a JTAG test mode during a power-up sequence.

The Bt812 has the optional device identification register defined by the JTAG specification. This register contains information concerning the revision, actual part number and manufacturers identification code specific to Brooktree. This register can be accessed through the TAP controller via the standard JTAG instruction set. See Figure 18b.

A variety of verification procedures can be performed through the TAP Controller. Through a set of four instructions, the Bt812 can verify board connectivity at all digital pins. The instructions are accessible through the use of a state machine standard to all JTAG controllers. The Bt812 supports the following four instructions, Sample/Preload, Extest, ID Code and Bypass (see Figure 18c). Refer to the IEEE P1149.1 specification for details concerning the Instruction Register and JTAG state machine.

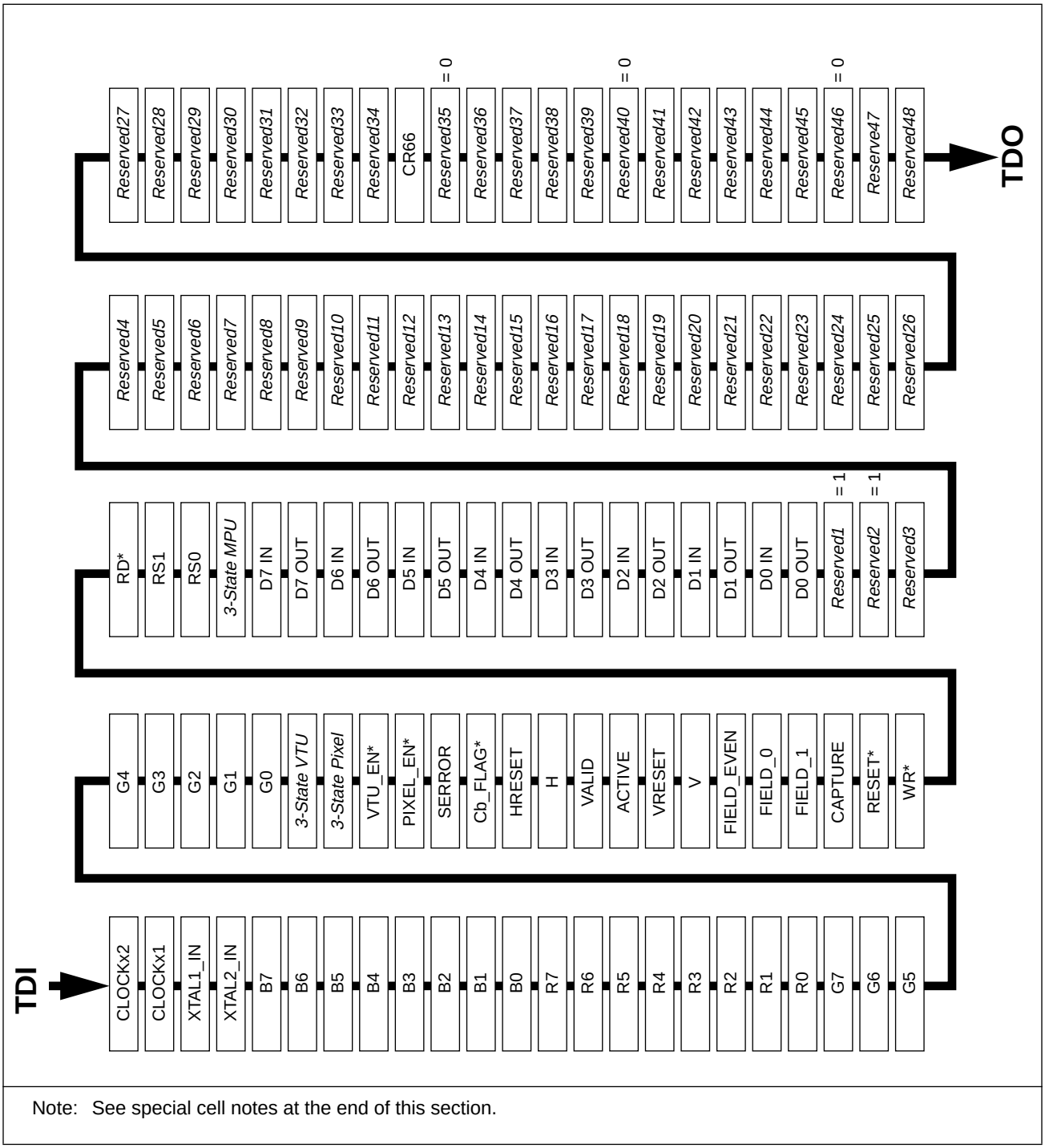
### JTAG Initialization

On power-up, the Bt812 requires resetting of the JTAG circuitry. This requires a minimum of five rising edges on TCK after power-up. TMS must be left floating or tied high during these edge transitions. As indicated in the IEEE JTAG specification, this will guarantee the Bt812 has been reset.

A continuous free-running clock can be used to drive the TCK pin (it does not need to be disconnected during normal operation of the Bt812). The clock into TCK can be driven at a maximum speed of 30 MHz or as slowly as desired. However, five clock cycles must be completed before attempting to write to the Bt812.

Possible clock sources to TCK are the ISA bus clock, RESET* pulsed five times, RD* pulsed five times or the oscillator driving the Bt812. (If using a crystal with the Bt812, this signal should not be directly connected to TCK as it will alter the crystal timing).

**Figure 18a. Boundary Scan Register**




Note: See special cell notes at the end of this section.

## Boundary Scan–Special Cells Notes

Three-State VTU — By loading a logical one into this cell, the video timing unit outputs (CbFLAG*, HRESET*, VRESET*, HACTIVE*, VACTIVE*, VALID, ACTIVE, FIELD_EVEN, FIELD_0, FIELD_1, and CAPTURE) are three-stated.

Three-State Pixel — By loading a logical one into this cell, the video timing unit outputs (R0–R7, G0–G7, B0–B7) are three-stated.

Three-State MPU — By loading a logical one into this cell, the MPU interface D0–D7 are three-stated.

Reserved1–Reserved48 — For internal use, the state of these cells is undefined; however Reserved1 and Reserved2 must be loaded with a logical one. Reserved35, Reserved40, and Reserved46 must be loaded with a logical zero. These restrictions are shown on the Serial Scan Path Diagram.

**Figure 18b. Device Identification Register**

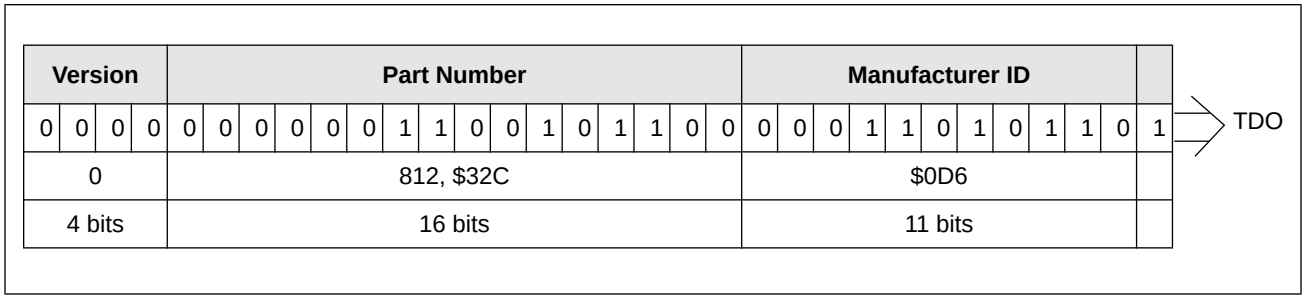
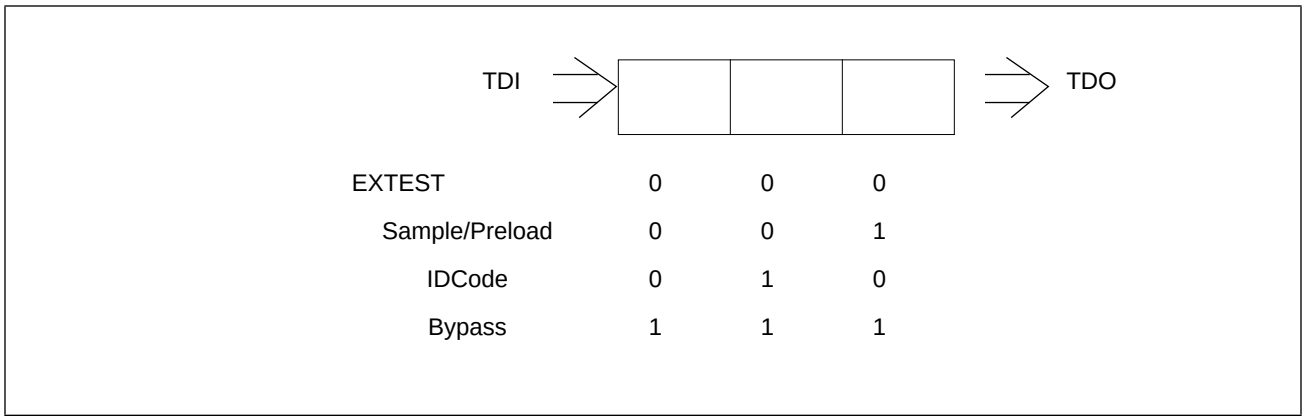
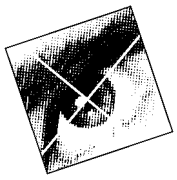



**Figure 18c. Instruction Register**





# INTERNAL REGISTERS

### Software Reset

The device is reset when the MPU writes to the address $FF. The same effect is achieved by taking the RESET* pin low. Upon reset, the MPU registers are initialized to their preset values (for decoding square pixel NTSC format). These values have been highlighted by an @ sign before them in the preceding register definitions. The RESET* pin must be held low for at least four clocks for proper operation.

### Command Register 0 (Input Select Register)

This command register may be written to or read by the MPU at any time and is initialized to $00. CR0_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR0_7–CR0_5 | VOUT_Y Select<br>@(000) VID0_Y<br>(001) VID1_Y<br>(010) VID2_Y<br>(011) VID3_Y<br>(100) Reserved<br>(101) Reserved<br>(110) Reserved<br>(111) Reserved | These bits specify which analog input is to be output onto VOUT_Y. |
| CR0_4, CR0_3 | VOUT_C Select<br>@(00) VID0_C<br>(01) VID1_C<br>(10) VID2_C<br>(11) VID3_C | These bits specify which analog input is to be output onto VOUT_C. |
| CR0_2–CR0_0 | Reserved (Logical Zero) | |

### Command Register 1 (Reserved)

This command register is reserved for future use. MPU write cycles to this register may cause undefined behavior and should not be attempted. MPU read cycles return an undefined value.

## Command Register 2 (Status Register)

This command register may be written to or read by the MPU at any time and is initialized to $00. CR2_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR2_7 | Video Present Status Bit<br>@(0) Video not present<br>(1) Video present | Video is valid when at least 31 clock cycles with video levels above 1/2 the sync height are present during the first half of each line of video. In the presence of video this bit is set to a logical one. It can be reset to zero by writing a logical zero to this bit. |
| CR2_6 | Video Stability Status Bit<br>@(0) Hsync not detected in window<br>(1) Hsync detected in window | If Hsync is found within ±1 clock of the expected position of Hsync for 32 consecutive lines, this bit is reset to a logical one. It is set to a logical zero if Hsync is not found in the ±1 clock window for 32 consecutive lines. MPU write cycles to this bit are ignored. This bit indicates the stability of the incoming video. |
| CR2_5 | Y Overflow Status Bit<br>@(0) No overflow in Y-ADC<br>(1) Overflow in the Y-ADC | The Y Overflow Status Bit is set to logical high when an overflow occurs in the Y/composite ADC. It can be reset by writing a logical zero to this bit. |
| CR2_4 | C Overflow Status Bit<br>@(0) No overflow in C-ADC<br>(1) Overflow in the C-ADC | The C Overflow Status Bit is set to logical high when an overflow occurs in the C-ADC. It can be reset by writing a logical zero to this bit. |
| CR2_3 | Color Status Bit<br>@(0) Valid color source<br>(1) Invalid color source | If the input subcarrier amplitude is below 25 percent (NTSC) or 35 percent (PAL) of nominal for 127 consecutive scan lines, or if the input has been defined as being monochrome, the Color Status Bit is set to logical high. It is reset to zero when a valid color source is detected, and the input is not defined as being monochrome. This bit is used to determine operation of the automatic low color detection and removal. MPU write cycles to this bit are ignored. |
| CR2_2–CR2_0 | Reserved (Logical Zero) | |

### Command Register 3 (Output Format Definition Register)

This command register may be written to or read by the MPU at any time and is initialized to $00. CR3_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR3_7–CR3_5 | Color Output Format Select<br>@(000) 24-bit RGB (8:8:8)<br>(001) Reserved<br>(010) Rounded 16-bit RGB (5:6:5)<br>(011) Rounded 15-bit RGB (5:5:5)<br>(100) Reserved<br>(101) 24-bit YCrCb (4:4:4)<br>(110) 16-bit YCrCb (4:2:2)<br>(111) Reserved | Color output mode select. (See Table 10 for details of the formats.) |
| CR3_4, CR3_3 | Gamma Removal Type<br>@(00) No gamma removal, bypass lookup tables<br>(01) Remove gamma correction of 2.2<br>(10) Remove gamma correction of 2.8<br>(11) Reserved | These bits specify whether to bypass the ROM lookup tables that remove gamma correction from the RGB data. Regardless of the selection, there is no change in the pipeline delay through the device. A gamma value of 2.2 or 2.8 is usually selected for NTSC and PAL, respectively. |
| CR3_2–CR3_0 | Reserved (Logical Zero) | |

**Table 10. Color Output Configurations**

| | 24-Bit True-Color RGB | 16-Bit True-Color RGB | 15-Bit True-Color RGB | 24-Bit YCrCb | 16-Bit YCrCb |
|---|---|---|---|---|---|
| **Output Pins** | **Mode (000)** | **Mode (010)** | **Mode (011)** | **Mode (101)** | **Mode (110)** |
| R7 | R7 | R7 | R7 | Cr7 | x |
| R6 | R6 | R6 | R6 | Cr6 | x |
| R5 | R5 | R5 | R5 | Cr5 | x |
| R4 | R4 | R4 | R4 | Cr4 | x |
| R3 | R3 | R3 | R3 | Cr3 | x |
| R2 | R2 | x | x | Cr2 | x |
| R1 | R1 | x | x | Cr1 | x |
| R0 | R0 | x | x | Cr0 | x |
| G7 | G7 | G7 | G7 | Y7 | Y7 / Y7’ |
| G6 | G6 | G6 | G6 | Y6 | Y6 / Y6’ |
| G5 | G5 | G5 | G5 | Y5 | Y5 / Y5’ |
| G4 | G4 | G4 | G4 | Y4 | Y4 / Y4’ |
| G3 | G3 | G3 | G3 | Y3 | Y3 / Y3’ |
| G2 | G2 | G2 | x | Y2 | Y2 / Y2’ |
| G1 | G1 | x | x | Y1 | Y1/ /Y1’ |
| G0 | G0 | x | x | Y0 | Y0/ /Y0’ |
| B7 | B7 | B7 | B7 | Cb7 | Cb7 / Cr7 |
| B6 | B6 | B6 | B6 | Cb6 | Cb6 / Cr6 |
| B5 | B5 | B5 | B5 | Cb5 | Cb5 / Cr5 |
| B4 | B4 | B4 | B4 | Cb4 | Cb4 / Cr4 |
| B3 | B3 | B3 | B3 | Cb3 | Cb3 / Cr3 |
| B2 | B2 | x | x | Cb2 | Cb2 / Cr2 |
| B1 | B1 | x | x | Cb1 | Cb1 / Cr1 |
| B0 | B0 | x | x | Cb0 | Cb0 / Cr0 |

Note: An “x” indicates undefined data.

### Command Register 4 (Operation Mode Select Register)

This command register may be written to or read by the MPU at any time and is initialized to $00. CR4_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR4_7 | Power Down<br>@(0) Normal operation<br>(1) Power down | Power-down mode minimizes power consumption. The values of the control registers are retained and remain accessible through the MPU interface. The Bt812 becomes operational about 1 second after the power-down mode is disabled. |
| CR4_6 | Mode Select<br>@(0) Normal operation<br>(1) Generate color bars | If color bar generation is selected, the Bt812 generates 75% amplitude, 100% saturation color bars in the following sequence: gray, yellow, cyan, green, magenta, red, blue, and black. The width of each color bar is 64 pixels wide. If HACTIVE is set to output more or less than 512 pixels (8 color bars, each 64 pixels wide) then the excess (or lack of) pixels will be accounted for in the first color bar. If HACTIVE is set to output more than 512 pixels, then the first color bar will be wider than the remaining seven. If HACTIVE is set to output less than 512 pixels then the first color bar will not be as wide as the following seven. When generating color bars, the analog video inputs are ignored, except to extract timing information. The format of the data output can be either YCrCb or RGB and depends on the mode selected through CR3_7–CR3_5. |
| CR4_5 | AGC Enable/Disable<br>@(0) AGC enabled<br>(1) AGC disabled | This bit determines whether the on-chip automatic gain control is enabled or disabled. |
| CR4_4 | Chroma AGC Enable/Disable<br>@(0) Chroma AGC enabled<br>(1) Chroma AGC disabled | This bit determines whether the on-chip automatic chroma gain control is enabled or disabled. |
| CR4_3 | Low Color Detection Enable/Disable<br>@(0) Low color detection and removal enabled<br>(1) Low color detection and removal disabled | This bit determines whether the low color detection circuit is enabled or disabled. The status is reflected by bit CR2_3 in Command Register 2. |
| CR4_2–CR4_0 | Reserved (Logical Zero) | |

### Command Register 5 (Input Format Definition Register)

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR5_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR5_7 | Y/C or Composite<br>@(0) Composite format<br>(1) Y/C component format | This bit defines whether the input is in composite or component format. |
| CR5_6 | Chroma Modulation<br>@(0) No phase alternation (NTSC)<br>(1) Phase alternation (PAL) | This bit defines whether the input has been modulated with phase alternation (as in PAL formats) or not (as in NTSC formats). |
| CR5_5 | Sync, Blank, and Black Level<br>@(0) –40, 0, 7.5 IRE (NTSC)<br>(1) –43, 0, 0 IRE (PAL) | This bit defines the sync, blank, and black levels of the input signal. |
| CR5_4 | Lines per Frame<br>@(0) 525 lines per frame (NTSC)<br>(1) 625 lines per frame (PAL) | This bit defines whether 525 or 625 lines per frame input format is being decoded. |
| CR5_3 | Reserved (Logical Zero) | |
| CR5_2 | Number of Sync Pulses in Vertical Interval<br>@(0) 6 pulses (NTSC)<br>(1) 5 pulses (PAL) | This bit defines the number of serration or equalization pulses in the vertical interval. |
| CR5_1 | Monochrome Input Source<br>@(0) Color input<br>(1) Monochrome input | The monochrome bit, when set to logical high, inhibits Y/C separation and sets the saturation level of the chroma path to zero. |
| CR5_0 | Reserved (Logical Zero) | |

### Command Register 6 (Clock Definition Register)

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR6_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR6_7 | Reserved (Logical Zero) | |
| CR6_6 | Crystal Select<br>@(0) XTAL1_IN<br>(1) XTAL2_IN | The crystal select bit determines which of the two crystals is to be used to generate the internal clock. This enables software selection of either a PAL or NTSC clock source. For square-pixel NTSC and PAL video, the frequencies would be 24.545454 MHz and 29.50 MHz, respectively. |
| CR6_5–CR6_0 | Reserved (Logical Zero) | |

### Command Register 7 (Video Timing Definition Register)

This command register may be written to or read by the MPU at any time and is initialized to $00. CR7_0 is the least significant bit and corresponds to data bus bit D0.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR7_7 | Capture (Field) Strobe | This bit is synchronized to the vertical sync and odd field information, and is output onto the CAPTURE output pin. |
| CR7_6 | Capture (Frame) Strobe | This bit is synchronized to the vertical sync and frame information, and is output onto the CAPTURE output pin. |
| CR7_5 | Reserved (Logical Zero) | |
| CR7_4 | CAPTURE Status | This bit reflects the value of the CAPTURE output pin. MPU write cycles to this bit are ignored. |
| CR7_3 | Pixel Output Enable<br>@(0) Outputs enabled<br>(1) Outputs three-stated | This bit specifies whether to three-state the R0–R7, G0–G7, and B0–B7 outputs. The outputs are three-stated asynchronously to the pixel clock. |
| CR7_2 | Control Output Enable<br>@(0) Outputs enabled<br>(1) Outputs three-stated | This bit specifies whether to three-state the HRESET*, VRESET*, ACTIVE, HACTIVE*, VACTIVE*, SERROR, CAPTURE, CbFLAG*, VALID, FIELD_1, FIELD_0, and FIELD_EVEN outputs. The outputs are three-stated asynchronously to the pixel clock. The clock outputs are not three-stated. |
| CR7_1, CR7_0 | Reserved (Logical Zero) | |

### Brightness-Adjust Register

The Brightness-Adjust Register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR8_0 corresponds to data bus bit D0 and is the least significant bit.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR8_7–CR8_1 | Brightness Control | Brightness-control bits. The brightness may be adjusted in 128 steps, from –64 to +63. The increments are .77%/step. These values are percentages with respect to full scale brightness. The (+) specifies to increase brightness; the (–) specifies to decrease brightness. |
| CR8_0 | Reserved (Logical Zero) | |

| CR87–CR80 | CR87–CR81, CR80 | Value |
|---|---|---|
| 80 | 1000000 0 | –64 |
| 82 | 1000001 0 | –63 |
| : | : | : |
| FC | 1111110 0 | –2 |
| FE | 1111111 0 | –1 |
| 00 | 0000000 0 | 0 |
| 02 | 0000001 0 | +1 |
| : | : | : |
| 7E | 0111111 0 | +63 |

### Contrast-Adjust Register

The Contrast-Adjust Register may be written to or read by the MPU at any time and is initialized to $80 following a reset sequence. CR9_0 corresponds to data bus bit D0 and is the least significant bit.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR9_7–CR9_1 | Contrast Control | Contrast-control bits. The contrast may be adjusted in 128 steps, from 0–198.44%, in increments of 1.56%. Contrast of 0% corresponds to black output. |
| CR9_0 | Reserved (Logical Zero) | |

| CR97–CR91 | CR97–CR91, CR90 | % Contrast |
|---|---|---|
| FE | 1111111 0 | 198.44 |
| FC | 1111110 0 | 196.87 |
| : | : | : |
| 82 | 1000001 0 | 101.56 |
| 80 | 1000000 0 | 100 |
| 7E | 0111111 0 | 98.44 |
| : | : | : |
| 02 | 0000001 0 | 1.56 |
| 00 | 0000000 0 | 0 |

### Saturation-Adjust Register

The Saturation-Adjust Register may be written to or read by the MPU at any time and is initialized to $80 following a reset sequence. CRA_0 corresponds to data bus bit D0 and is the least significant bit.

| Bit(s) | Field Names | Description |
|---|---|---|
| CRA_7–CRA_1 | Saturation Adjust | Saturation-adjust bits. The saturation may be adjusted in 128 steps, from 0–200 percent, in increments of 1.56 percent. |
| CRA_0 | Reserved (Logical Zero) | |

| CRA7–CRA0 | CRA7–CRA1, CRA0 | % Saturation |
|---|---|---|
| FE | 1111111 0 | 198.44 |
| FC | 1111110 0 | 196.87 |
| : | : | : |
| 82 | 1000001 0 | 101.56 |
| 80 | 1000000 0 | 100 |
| 7E | 0111111 0 | 98.44 |
| : | : | : |
| 02 | 0000001 0 | 1.56 |
| 00 | 0000000 0 | 0 |

### Hue-Adjust Register

The Hue-Adjust Register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CRB_0 corresponds to data bus bit D0 and is the least significant bit.

| Bit(s) | Field Names | Description |
|---|---|---|
| CRB_7–CRB_1 | Hue Adjust | Hue-adjust bits. The hue may be adjusted in 128 steps, from –45 to +44.3 degrees in increments of 0.7 degree. |
| CRB_0 | Reserved (Logical Zero) | |

| CRB7–CRB0 | CRB7–CRB1, CRB0 | Degrees Shift |
|---|---|---|
| 80 | 1000000 0 | –45 |
| 82 | 1000001 0 | –44.3 |
| : | : | : |
| FC | 1111110 0 | –1.4 |
| FE | 1111111 0 | –0.7 |
| 00 | 0000000 0 | 0 |
| 02 | 0000001 0 | +0.7 |
| : | : | : |
| 7E | 0111111 0 | +44.3 |

### HCLOCK Register

This 11-bit register specifies the number of clocks per line of video at the frequency $f_{CLOCKx1}$. It is initialized to $030C (780) following a reset condition and may be written to or read by the MPU at any time. The HCLOCK high (address $0D) and the HCLOCK low (address $0C) registers are independent and are individually written to and read by the MPU.

The HCLOCK low and high registers are cascaded to form an 11-bit HCLOCK register. D7–D3 of HCLOCK high are ignored during MPU write cycles and return logical zeros during MPU read cycles. Values from $201 (513) to $07FF (2047) may be specified.

| | HCLOCK High ($0D) | | | HCLOCK Low ($0C) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | H10 | H9 | H8 | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

### HDELAY Register

This 11-bit register specifies the number of clocks (at the frequency $f_{DESIRED\_HCLOCK}$) after HRESET* that active video output should begin. In the input video signal this corresponds to the number of pixels after Hsync that active video should begin. It is initialized to $0075 (117) following a reset condition and may be written to or read by the MPU at any time. The HDELAY high (address $0F) and the HDELAY low (address $0E) registers are independent and are individually written to and read by the MPU.

The HDELAY low and high registers are cascaded to form an 11-bit HDELAY register. D7–D3 of HDELAY high are ignored during MPU write cycles and return logical zeros during MPU read cycles. Values from $0001 (1) to $07FF (2047) may be specified. In 16-bit YCrCb mode, the first pixel will contain Cb if HDELAY is even. The first pixel will contain Cr if HDELAY is odd

| | HDELAY High ($0F) | | | HDELAY Low ($0E) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | H10 | H9 | H8 | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

### ACTIVE_PIXELS Register

This 11-bit register specifies the number of active pixels per scan line. It is initialized to $0280 (640) following a reset condition and may be written to or read by the MPU at any time. The ACTIVE_PIXELS low (address $10) register and the ACTIVE_PIXELS high register (address $11) may be written to or read by the MPU at any time.

The ACTIVE_PIXELS low and high registers are cascaded to form an 11-bit ACTIVE_PIXELS Register. D7–D3 of ACTIVE_PIXELS high are ignored during MPU write cycles and return logical zeros during MPU read cycles. Values from $0000 (0) to $07FF (2047) may be specified.

| | ACTIVE_PIXELS High ($11) | | | ACTIVE_PIXELS Low ($10) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | H10 | H9 | H8 | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

### VDELAY Register

This 10-bit register (addresses $13 and $12) specifies the number of lines after the rising edge of VRESET* that active video should begin for one full frame of video. The beginning of active video lines is indicated by the falling edge of V. See Table 5 and Figure 14 for details. Values from $0001 (1) to $03FF (1023) may be specified. The register may be written to or read by the MPU at any time and is initialized to $16 (22). If the MPU writes to the VDELAY low register (address $13), it is not updated until the MPU writes to the VDELAY high register (address $12).

The VDELAY low and high registers are cascaded to form a 10-bit VDELAY Register. D7–D2 of VDELAY high are ignored during MPU write cycles and return logical zeros during MPU read cycles. Values from $0000 (0) to $03FF (1023) may be specified.

| | VDELAY High ($13) | | VDELAY Low ($12) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | V9 | V8 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

### ACTIVE_LINES Register

This 10-bit Register specifies the number of active (nonblanked) scan lines per frame (two fields). It is initialized to $01E0 (480) following a reset condition and may be written to or read by the MPU at any time. If the MPU writes to the ACTIVE_LINES low register (address $14), it is not updated until the MPU writes to the ACTIVE_LINES high register (address $15). Active display resolution is one scan line per frame.

The ACTIVE_LINES low and high registers are cascaded to form a 10-bit ACTIVE_LINES Register. D7–D2 of ACTIVE_LINES high are ignored during MPU write cycles and return logical zeros during MPU read cycles.

Values from $0000 (0) to $03FF (1023) may be specified.

| | ACTIVE_LINES High ($15) | | ACTIVE_LINES Low ($14) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | V9 | V8 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

## P (Subcarrier Frequency) Register

The P (Subcarrier Frequency) Register 0 (address $16), Register 1 (address $17), and Register 2 (address $18) are cascaded to form a 22-bit P (Subcarrier Frequency) Register. D6 and D7 of P (Subcarrier Frequency) Register 2 are ignored during MPU write cycles and return logical zeros during MPU read cycles. Values from $000000 (0) to $100000 (4194303) may be specified. The 22-bit register is initialized to $12AAAB (1223339) following a reset condition (for 12.27 MHz clock and 3.579 MHz subcarrier frequency). D0 of P (Subcarrier Frequency) Register 0 is the LSB, and D7 of P (Subcarrier Frequency) Register 2 is the MSB. The value to be loaded into this register is given by the following formula:

$$P = (\text{subcarrier frequency}/f_{CLOCKx1})*2^{22}$$

| | P (Subcarrier Frequency) Register 2 $18 | | | | | | P (Subcarrier Frequency) Register 1 $17 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | V21 | V20 | V19 | V18 | V17 | V16 | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 |

| | P (Subcarrier Frequency) Register 2 $18 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

## AGC Delay Register

The AGC Delay Register (address $19) defines the number of clock cycles between the falling edge of sync and the point on the back porch where the AGC samples to determine the back-porch level. This 8-bit register (with D7 the MSB and D0 the LSB) can be written to or read by the MPU at any time. This register is initialized to the value of $51 (81) upon reset. The value loaded in this register is approximately the number of clock cycles in a 6.75 microsecond interval.

$$\text{AGC delay value} = 6.75\ \mu S \times f_{CLOCKx1}+8$$

## Burst-Delay Register

The subcarrier Burst-Delay Register (address $1A) specifies the number of clock cycles between the falling edge of the hsync and the middle of the subcarrier burst. This 8-bit register (with D7 the MSB and D0 the LSB) can be written to or read by the MPU at any time. This register is initialized to the value of $46 (70) upon reset.

$$\text{Burst-delay value} = 6.5\ \mu S \times f_{CLOCKx1} - 10$$

### Sample-Rate Conversion Register

This 16-bit register (addresses $1C, $1B) specifies the sample-rate conversion ratio that is calculated with the following formula:

$$\text{Sample-rate conversion ratio} = [(\text{HCLOCK} - \text{DESIRED\_HCLOCK})/\text{DESIRED\_HCLOCK}]*2^{16}$$

DESIRED_HCLOCK is defined as the number of clocks in a line at the resampled pixel frequency. DESIRED_HCLOCK must be between 8/11 and 1 times HCLOCK, (HCLOCK ≥ DESIRED_HCLOCK ≥ 8/11 * HCLOCK). Equivalent formulas can be obtained by substituting either clock frequencies or clocks of active video per line for clocks per line in the above formula.

This is the actual register which defines the effective pixel rate versus the clock rate driving the Bt812.

When generating square pixel NTSC from a 15 MHz HCLOCK the Sample-Rate Conversion Register should be programmed as follows:

$$\text{Sample-Rate Conversion Register Value} = \frac{(954 - 780)}{780} \text{¥ } 2^{16}$$
$$= .2230769 \times 2^{16}$$
$$= 14{,}620$$
$$= \$391C \text{ (hex)}$$

The Sample-Rate Conversion Register can be written to or read from at any time. This register is initialized to $0000 upon reset. If the MPU writes to the Sample-Rate Conversion low register (address $1C), it is not updated until the MPU writes to the Sample-Rate Conversion high register (address $1B).

The Sample-Rate Conversion low and high registers are cascaded to form a 16-bit Sample-Rate Conversion Register.

| | **Sample-Rate Conversion High ($1C)** | | | | | | | | **Sample-Rate Conversion Low ($1B)** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data Bit** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Cascaded** | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

## Command Register 1D (Video Timing Polarity Register)

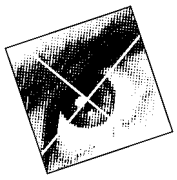
This command register may be written to or read by the MPU at any time and is initialized to $35. CR1D_0 is the least significant bit and corresponds to data bus bit D0.

***NOTE:*** The Video Timing description in Figure 16 assumes this register is programmed with $30.

| Bit(s) | Field Names | Description |
|---|---|---|
| CR1D_7 | Reserved (Logical Zero) | |
| CR1D_6 | Reserved (Logical Zero) | |
| CR1D_5 | VALID Polarity<br>(0) Active low<br>@(1) Active high | This bit defines whether the VALID pin output will be active high or active low. |
| CR1D_4 | ACTIVE Polarity<br>(0) Active low<br>@(1) Active high | This bit defines whether the ACTIVE pin output will be active high or active low. |
| CR1D_3 | HRESET* Polarity<br>@(0) Active low<br>(1) Active high | This bit defines whether the HRESET* pin output will be active high or active low. |
| CR1D_2 | HACTIVE* Polarity<br>(0) Active low<br>@(1) Active high | This bit defines whether the HACTIVE* pin output will be active high or active low. |
| CR1D_1 | VRESET* Polarity<br>@(0) Active low<br>(1) Active high | This bit defines whether the VRESET* pin output will be active high or active low. |
| CR1D_0 | VACTIVE* Polarity<br>(0) Active low<br>@(1) Active high | This bit defines whether the VACTIVE* pin output will be active high or active low. |

**Table 11. Register Programming Values**

| Address | Name | Example #1 | Example #2 | Example #3 |
|---|---|---|---|---|
| | | **Square Pixel NTSC** | **Square Pixel PAL** | **Square Pixel NTSC** |
| | | $f_{DESIRED\_HCLOCK}$ = 12.27 MHz<br>XTAL_IN = 24.54 MHz | $f_{DESIRED\_HCLOCK}$ = 14.75 MHz<br>XTAL_IN = 29.5 MHz | $f_{DESIRED\_HCLOCK}$ = 12.27 MHz<br>XTAL_IN = 29.5 MHz |
| $00 | CR0, Input Select | $60 | $60 | $60 |
| $03 | CR3, Output Format | $00 | $00 | $00 |
| $04 | CR4, Operation Mode Select | $00 | $00 | $00 |
| $05 | CR5, Input Format Definition | $00 | $74 | $00 |
| $06 | CR6, Clock Definition | $40 | $40 | $40 |
| $07 | CR7, Video Timing Definition | $00 | $00 | $00 |
| $08 | Brightness Adjust | $00 | $00 | $00 |
| $09 | Contrast Adjust | $80 | $80 | $80 |
| $0A | Saturation Adjust | $80 | $80 | $80 |
| $0B | Hue Adjust | $00 | $00 | $00 |
| $0C | HCLOCK Low | $0C | $B0 | $A9 |
| $0D | HCLOCK High | $03 | $03 | $03 |
| $0E | HDELAY Low | $75 | $9B | $75 |
| $0F | HDELAY High | $00 | $00 | $00 |
| $10 | ACTIVE_PIXELS Low | $80 | $00 | $80 |
| $11 | ACTIVE_PIXELS High | $02 | $03 | $02 |
| $12 | VDELAY Low | $16 | $21 | $16 |
| $13 | VDELAY High | $00 | $00 | $00 |
| $14 | ACTIVE_LINES Low | $E0 | $3E | $E0 |
| $15 | ACTIVE_LINES High | $01 | $02 | $01 |
| $16 | P0, Subcarrier Frequency | $AB | $C6 | $15 |
| $17 | P1, Subcarrier Frequency | $AA | $3C | $88 |
| $18 | P2, Subcarrier Frequency | $12 | $13 | $0F |
| $19 | AGC Delay | $5A | $6C | $6C |
| $1A | Burst Delay | $46 | $56 | $56 |
| $1B | Sample Rate Conversion Low | $00 | $00 | $AC |
| $1C | Sample Rate Conversion High | $00 | $00 | $33 |
| $1D | CR1D, Video Timing Polarity | $30 | $30 | $30 |



# PC BOARD CONSIDERATIONS

## PC Board Layout

The layout should be optimized for lowest noise on the Bt812 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The lead length between groups of power and ground pins should be minimized to reduce inductive ringing.

### Ground Planes

The ground plane area should encompass all Bt812 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt812, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt812.

### Power Planes

The Bt812 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 19. This bead should be located within 3 inches of the Bt812. The Bt812 should also have a separate digital power plane. This power plane should be connected to the regular PCB power plane in the same mannner as the analog power plane is connected.

The digital power plane should provide power to VAA and VDD pins from pin 31 to pin 112 while the analog power plane should provide power to VAA pins from pin 113 to pin 30, as well as other external analog circuitry such as AGC components, input amplifiers, protection diodes, and anti-aliasing filters.

Portions of the regular PCB power planes must not overlay portions of the Bt812 analog or digital power plane. Linear regulators are not recommended because their delay characteristics may induce destructive latchup.

### Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

Each group of VAA and VDD pins should have a 0.1 µF ceramic bypass capacitor to ground, located as close as possible to the device.

### Digital Signal Interconnect

The digital signals of the Bt812 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

### Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VID_Y and VID_C inputs.

Also, high-speed TTL signals should not be routed close to the analog signals to minimize noise coupling.

### Latch-Up Avoidance

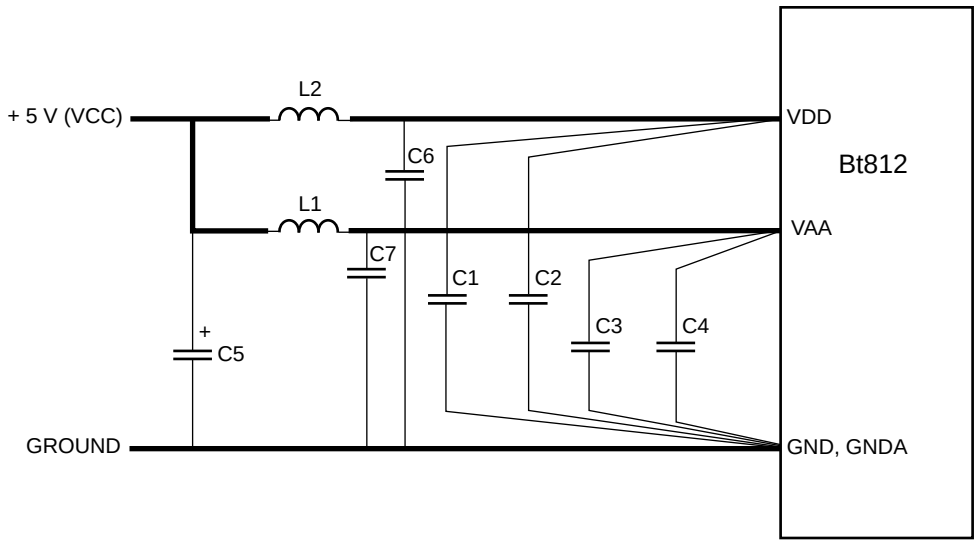
Latch-up is a failure mechanism inherent to any CMOS device. It is triggered by static or impulse voltages on any signal input pin exceeding the voltage on any power pin by more than 0.5 V, or falling below the GND pins by more than 0.5 V. Latchup can also occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

In some cases devices with mixed signal interfaces such as the Bt812 can appear more sensitive to latchup. In reality this is not the case. However, mixed signal devices tend to interact with peripheral devices such as video monitors or cameras that are referenced to different ground potentials or apply voltages to the device prior to the time that its power system is stable. This interaction sometimes creates conditions amenable to the onset of latchup.

To maintain a robust design with the Bt812, the following precautions should be taken:

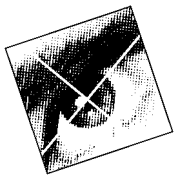
- Connect all digital power pins together through a low impedance plane (VAA and VDD pins 31 to 112).
- Connect all analog power pins together through a low impedance plane (VAA pins 113 to 30).
- Connect all GND and AGND pins together through a low impedance plane.
- Apply power to the device before or at the same time as the interface circuitry. Minimize the bulk decoupling on the VAA side of the ferrite bead to minimize the delay in VAA power-up. Do not use a regulator to provide power to VAA for the same reason.
- Do not apply voltages below GND–0.5 V or higher than VAA+0.5 V to any pin of the device. All logic inputs should be held low until power to the device has settled to the specified tolerance.
- Always apply power to the board containing the Bt812 before powering the cameras or monitors connected to it.

**Figure 19. Typical Connection Diagram and Parts List**




| Location | Description | Vendor Part Number (1) |
|---|---|---|
| C1, C2, C3, C4 (2) | 0.1 µF Ceramic Capacitor | Erie RPE112Z5U104M50V |
| C5, C6, C7 | 10 µF Tantalum Capacitor | Mallory CSR13G106KM |
| L1, L2 | Ferrite Bead | Fair-Rite 2743021447 |

Notes: (1). These vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt812.
(2). A 0.1 µF capacitor should be connected between each group of power pins and ground as close to the device as possible (ceramic chip capacitors are preferred).



# PARAMETRIC INFORMATION

## DC Electrical Parameters

**Table 12. Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply–Analog | VAA | 4.75 | 5.00 | 5.25 | V |
| Power Supply–Digital | VDD | 4.75 | 5.00 | 5.25 | V |
| VID0–VID3 Peak Voltage | | 0.7 | | 2.0 | V |
| Y, C Amplitude Range | | 0.7 | | 2.0 | V |
| YLEVEL Input Voltage | | YREF– | YREF– | YREF+ | V |
| CLEVEL Input Voltage | | CREF– | CREF+/2 | CREF+ | V |
| Ambient Operating Temperature | TA | 0 | | +70 | °C |

**Table 13. Absolute Maximum Ratings**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| VAA (measured to GNDA) | | | | 7.0 | V |
| VDD (measured to GND) | | | | 7.0 | V |
| Voltage on any Signal Pin (1) | | GND–0.5 | | VDD+0.5 | V |
| Analog Input Voltage | | GNDA–0.5 | | VAA+0.5 | V |
| R/2 Output Current | | | | 25 | µA |
| Storage Temperature | TS | –65 | | +150 | °C |
| Junction Temperature | TJ | | | +125 | °C |
| Vapor Phase Soldering (15 seconds) | TVSOL | | | 220 | °C |

Notes: (1). This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

2. Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 14. DC Characteristics**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Digital Inputs | | | | | |
| Input High Voltage (TTL) | VIH | 2.0 | | VDD + 0.5 | V |
| Input High Voltage (CMOS) XTAL1_IN and XTAL2_IN only | VIH | 3.5 | | VDD + 0.5 | V |
| Input Low Voltage (TTL) | VIL | GND–0.5 | | 0.8 | V |
| Input Low Voltage (CMOS) XTAL1_IN and XTAL2_IN only | VIL | GND–0.5 | | 1.5 | V |
| Input High Current (Vin = VDD) | IIH | | | 10 | µA |
| Input Low Current (Vin = GND) | IIL | | | –10 | µA |
| Input Capacitance (f = 1 MHz, Vin = 2.4 V) | CIN | | 7 | | pF |
| Digital Outputs | | | | | |
| Output High Voltage (IOH = –400 µA) | VOH | 2.4 | | VDD | V |
| Output Low Voltage (IOL = 3.2 mA) | VOL | | | 0.4 | V |
| Three-state Current | IOZ | | | 10 | µA |
| Output Capacitance | CO | | 10 | | pF |

Note: Test conditions (unless otherwise specified): “Recommended Operating Conditions.”

# AC Electrical Parameters

**Table 15. AC Characteristics** *(1 of 2)*

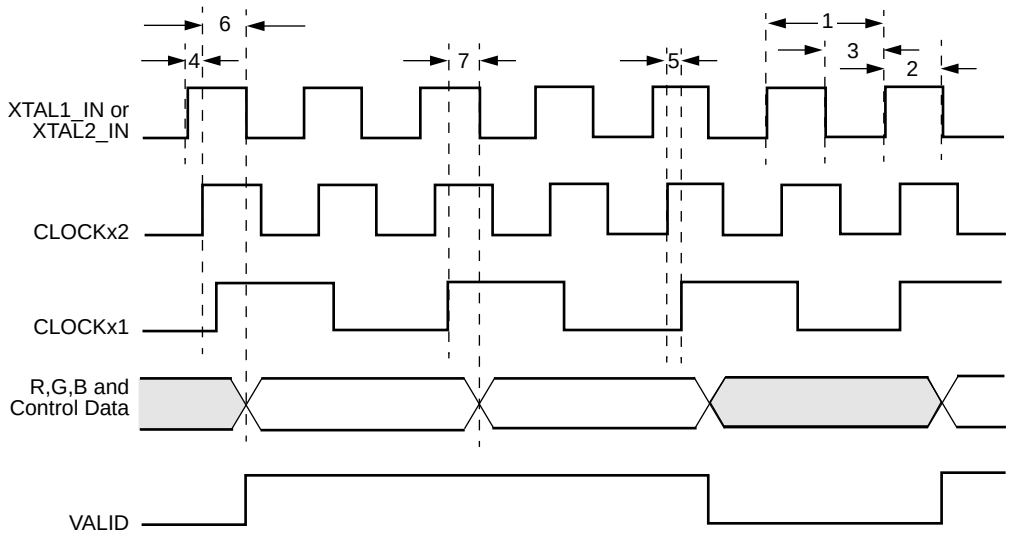
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| CLOCKx1 Rate | Fs | 8 | | 15 | MHz |
| XTAL_1 and XTAL_2 Input (Twice the Sample Rate) | | | | | |
| Cycle Time | 1 | 33.33 | | | ns |
| High Time | 2 | 12 | | | ns |
| Low Time | 3 | 12 | | | ns |
| XTAL_1,2 to CLOCKx2 Delay | 4 | 5 | | 30 | ns |
| CLOCKx2 Duty Cycle | | 40 | | 60 | % |
| CLOCKx2 to CLOCKx1 Delay | 5 | 2 | | 8 | ns |
| CLOCKx2 to Data Delay | 6 | 8 | | 20 | ns |
| CLOCKx1 Duty Cycle | | 40 | 50 | 60 | % |
| CLOCKx1 to Data Delay | 7 | 6 | | 21 | ns |
| JTAG: TMS, TDI Setup Time | 8 | 10 | | | ns |
| JTAG: TMS, TDI Hold Time | 9 | 10 | | | ns |
| JTAG: TCK Asserted to TDO Valid | 10 | | | 60 | ns |
| JTAG: TCK Asserted to TDO Driven | 11 | 5 | | | ns |
| JTAG: TCK Negated to TDO three-stated | 12 | | | 80 | ns |
| JTAG: TCK Low Time | 13 | 25 | | | ns |
| JTAG: TCK High Time | 14 | 25 | | 65 | ns |
| JTAG: TCK Asserted to TDO Delay (1) | # | | | | |
| A/D Full-Power Input Bandwidth | BW | 30 | | 6 | MHz |
| Supply Current | | | | | |
| 27 MHz, 5.0 V, 25° C | | | 190 | | mA |
| 30 MHz, 5.25 V, 0° C | | | | 255 | mA |
| 30 MHz, 5.25 V, 70° C | | | | 230 | mA |
| Supply Current during Power Down | | | 23 | | mA |
| RS0, RS1 Setup Time | 15 | 10 | | | ns |
| RS0, RS1 Hold Time | 16 | 5 | | | ns |
| RD* Asserted to Data Bus Driven | 17 | 3 | | | ns |
| RD* Asserted to Data Valid | 18 | | | 60 | ns |
| RD* Negated to Data Bus Three-stated | 19 | | | 60 | ns |
| Read Data Hold Time | 20 | 6 | | | ns |
| WR* Low Time | 21 | 40 | | | ns |
| Write Data Setup Time | 22 | 10 | | | ns |
| Write Data Hold Time | 23 | 5 | | | ns |
| RD*, WR* High Time | 24 | 50 | | | ns |

**Table 15. AC Characteristics** *(2 of 2)*

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| VTU_EN* or PIXEL_EN* Asserted to Data Bus Driven | 25 | 0 | | | ns |
| VTU_EN* or PIXEL_EN* Asserted to Data Valid | 26 | | | 60 | ns |
| VTU_EN* or PIXEL_EN* Negated to Data Bus Three-stated | 27 | | | 60 | ns |
| VTU_EN* or PIXEL_EN* Negated, Data Hold Time | 28 | 0 | | | ns |
| RESET* Low Time (CLOCKx1) | | 4 | | | Clocks |
| Pipeline Delay (CLOCKx1) (2) | | | 50 | | Clocks |

Notes: (1). Guaranteed By Characterization.
(2). The A/D converter samples on the falling edge of the clock. The pipeline delay is effectively 50.5 clock periods.
3. Test conditions (unless otherwise specified): “Recommended Operating Conditions.” TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0–D7 output load ≤ 60 pF. Pixel data output delay includes CAPTURE, HRESET*, VRESET*, FIELD_EVEN, FIELD_0, FIELD_1, ACTIVE, VALID, HACTIVE*, VACTIVE*, CbFLAG*, R0–R7, G0–G7, and B0–B7. Each has an output load ≤ 60 pF. VOUT_Y and VOUT_C output load ≤ 60 pF. See Figures 20–23.

**Figure 20. Clock Timing**




Note: Example using DESIRED_HCLOCK = (2/3) *HCLOCK. There are 2 valid pixels for every three samples.

**Figure 21. JTAG Timing**

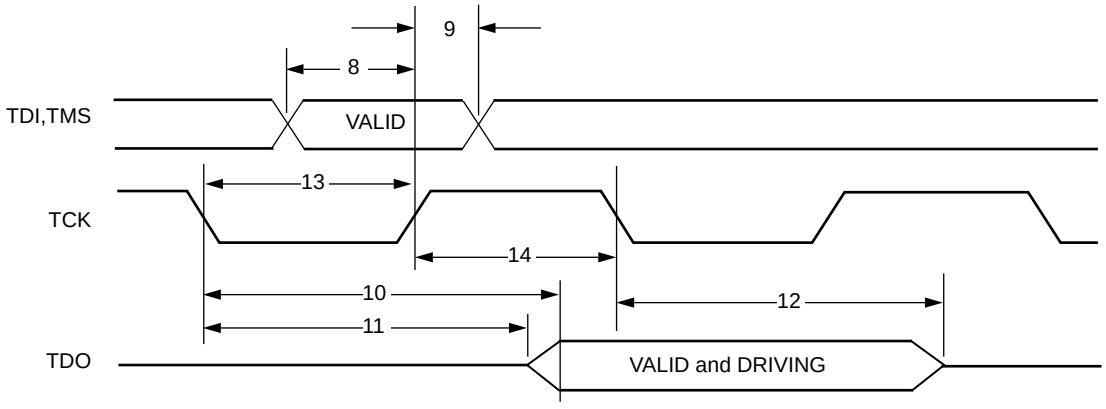


**Figure 22. MPU Port Timing**

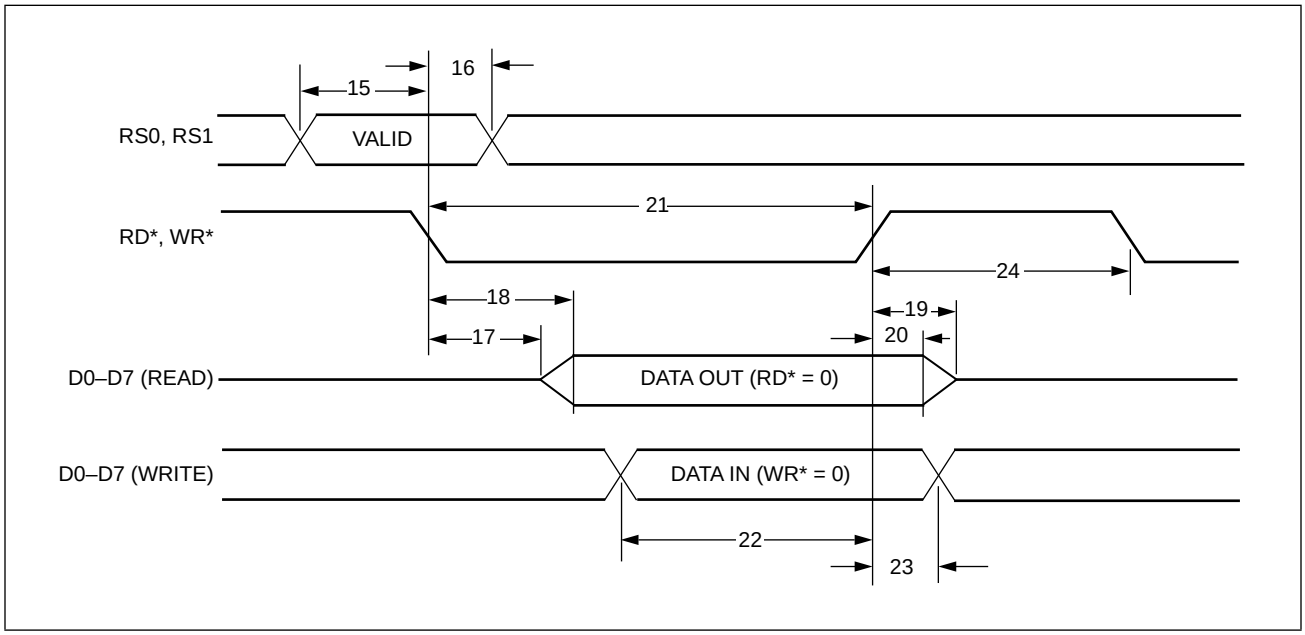
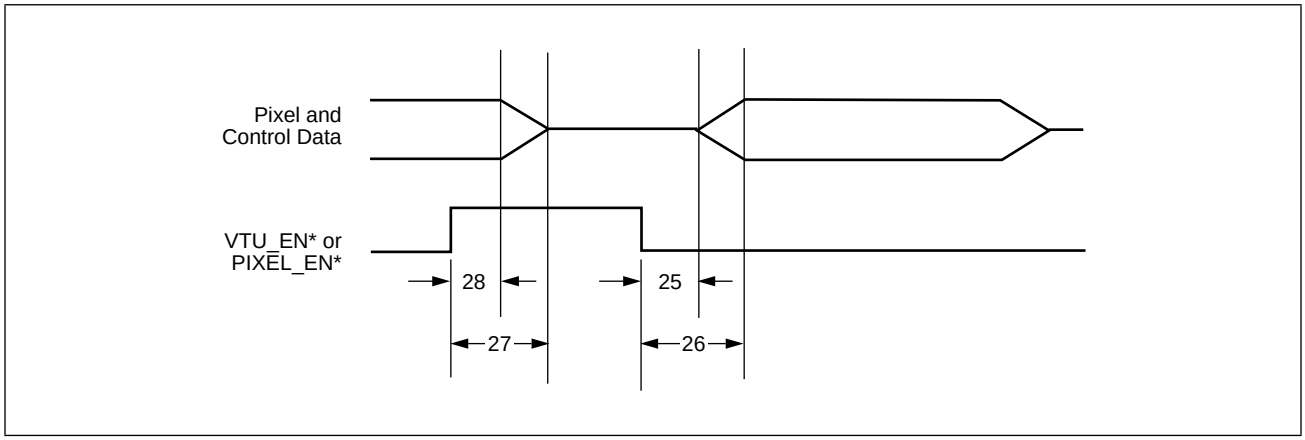
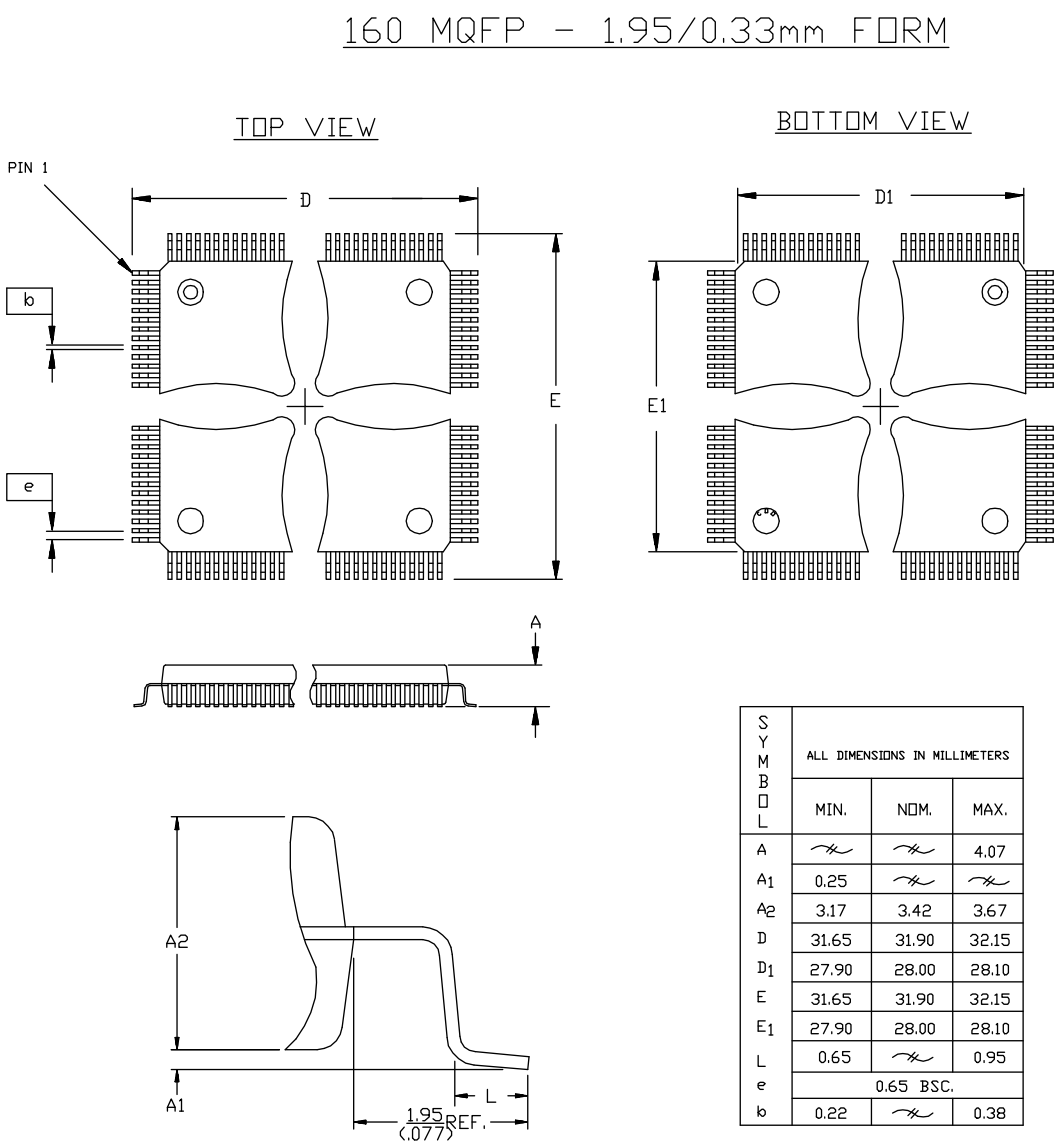



**Figure 23. Pixel and Control Data Three-State Timing**



# Package Drawing

## 160-pin Plastic Quad Flatpack (PQFP)




| SYMBOL | ALL DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | | | 4.07 |
| $A_1$ | 0.25 | | |
| $A_2$ | 3.17 | 3.42 | 3.67 |
| D | 31.65 | 31.90 | 32.15 |
| $D_1$ | 27.90 | 28.00 | 28.10 |
| E | 31.65 | 31.90 | 32.15 |
| $E_1$ | 27.90 | 28.00 | 28.10 |
| L | 0.65 | | 0.95 |
| e | 0.65 BSC. | | |
| b | 0.22 | | 0.38 |

# Revision History

| Revision | Change From Previous Revision |
|---|---|
| D & E | 1. External circuitry includes op-amp when implementing anti-aliasing filter between 4–1 multiplexer and A/D.<br>2. Polarity of CbFlag changed to CbFlag*.<br>3. Maximum speed changed to 30 MHz.<br>4. Suggested values for AGC delay changed.<br>5. Y/C separation filters added.<br>6. Documented CR2_6, Video Stability Status Register.<br>7. Documented CR1D, Video Timing Polarity Register.<br>8. HRESET* and VRESET* are offset by one clock of the beginning of an odd field. SPC “VRESET Generation” paragraph. Previous generations of the datasheet indicated these signals were coincident.<br>9. The following timing parameters have been pulled in:<br>Symbol — Name<br>7 — Clock x 1 to Data Delay (Min)<br>26 — VTU_EN*, Valid<br>27 — VTU_EN*, Three-State<br>1 — Power<br>16 — RS0, RS1 Hold Time<br>20 — Read Data Hold Time<br>10. The following timing parameters have been pushed out:<br>Symbol — Name<br>7 — Clock x 1 to Data (Max)<br>10 — JTAG, Valid<br>12 — JTAG, Three-State<br>18 — RD* to Data Valid<br>19 — RD* to Data Three-State<br>11. Incorporation of 5 clock requirement to TCK pin on power-up (see Power-On Initialization) |
| F | 1. Definition of video stability status bit inverted (CR2_6).<br>2. Note changes to latchup avoidance section in PC Board Layout Considerations section.<br>3. In Figure 3, the placement of the recommended diodes has changed and a 20 Ω series resistance was added.<br>4. The description of the internal color bars has changed (CR4_6).<br>5. The “Ambient Operating Temperature” specification has been removed.<br>6. The supply current for “30 MHz, 5.25 V, 70° C” has changed. In addition, the typographical errors in the supply current section have been corrected.<br>7. Moved suggested connection of SYNC_DET signal from before antialiasing filter to Y/composite signal. |

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