
BB401M

Build in Biasing Circuit MOS FET IC
VHF RF Amplifier

HITACHI

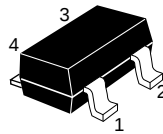
ADE-208-715A (Z)
2nd. Edition
Dec. 1, 1998

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics;
(NF = 1.3 dB typ. at f = 200 MHz)
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4R(SOT-143 var.)

Outline

MPAK-4R



1. Source
2. Drain
3. Gate2
4. Gate1

Notes: 1. Marking is "AX-".

2. BB401M is individual type number of HITACHI BBFET.

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Absolute Maximum Ratings (Ta = 25°C)

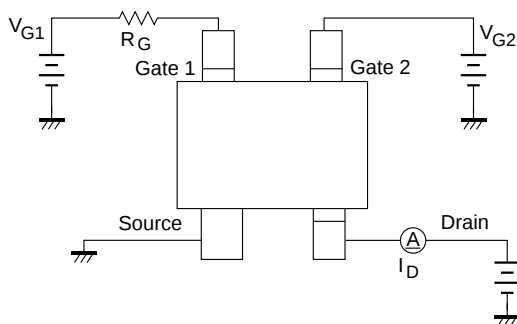
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 – 0	V
Gate 2 to source voltage	V_{G2S}	±6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

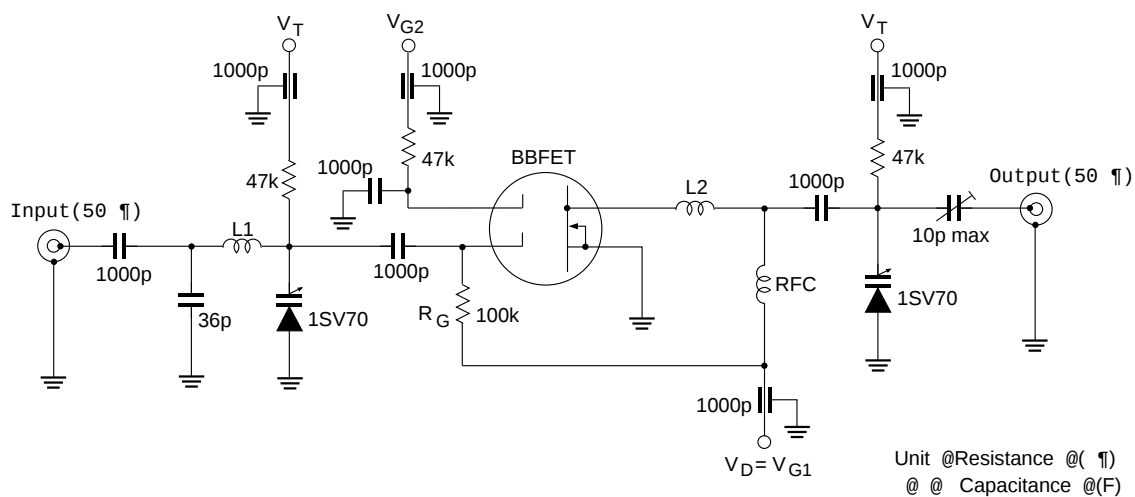
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	$I_{G2} = \pm 10\mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0$
Gate2 to cutoff current	I_{G2SS}	—	—	±100	nA	$V_{G2S} = \pm 5V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.4	0.7	1.0	V	$V_{DS} = 5V$, $V_{G2S} = 4V$, $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	0.7	1.0	V	$V_{DS} = 5V$, $V_{G1S} = 5V$, $I_D = 100\mu A$
Drain current	$I_{D(op)}$	10	15	20	mA	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$, $R_G = 100k\Omega$
Forward transfer admittance	$ Y_{fs} $	15	20	—	mS	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$ $R_G = 100k\Omega$, $f = 1kHz$
Input capacitance	C_{iss}	2.2	3.0	3.9	pF	$V_{DS} = 5V$, $V_{G1} = 5V$
Output capacitance	C_{oss}	0.9	1.2	1.6	pF	$V_{G2S} = 4V$, $R_G = 100k\Omega$
Reverse capacitance	C_{rss}	—	0.018	0.04	pF	$f = 1MHz$
Power gain	PG	22	26	—	dB	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$
Noise figure	NF	—	1.3	1.9	dB	$R_G = 100k\Omega$, $f = 200MHz$

Main Characteristics

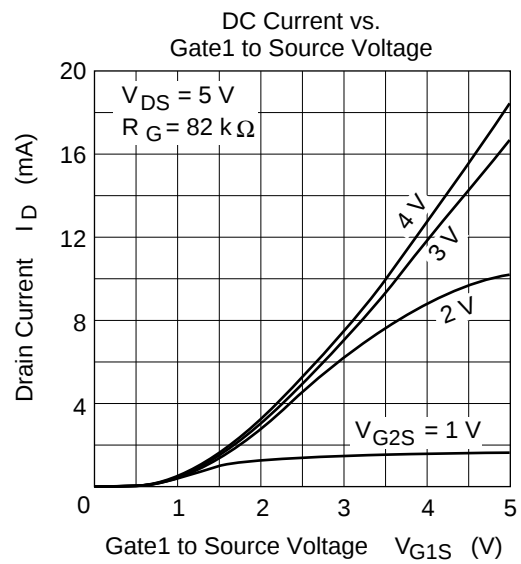
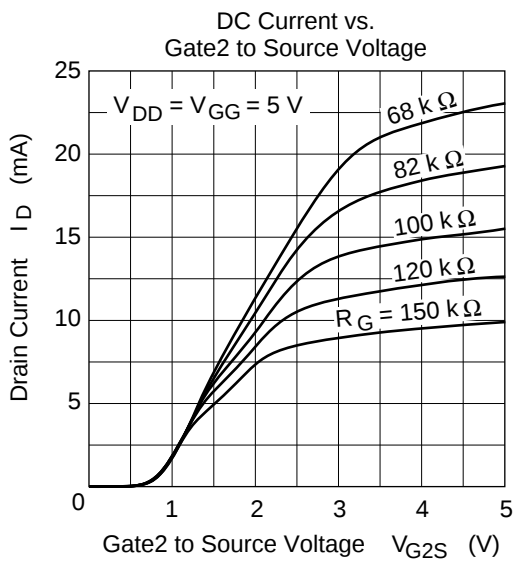
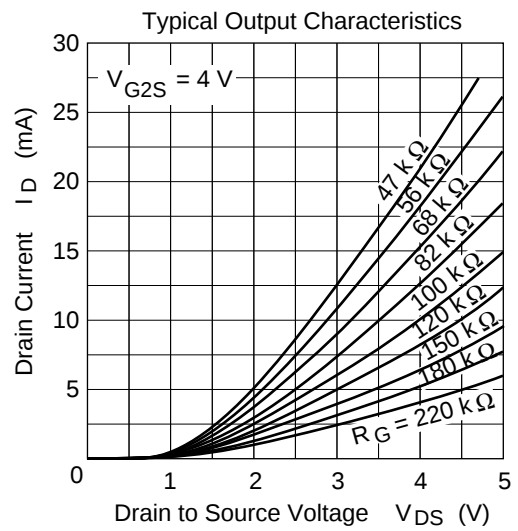
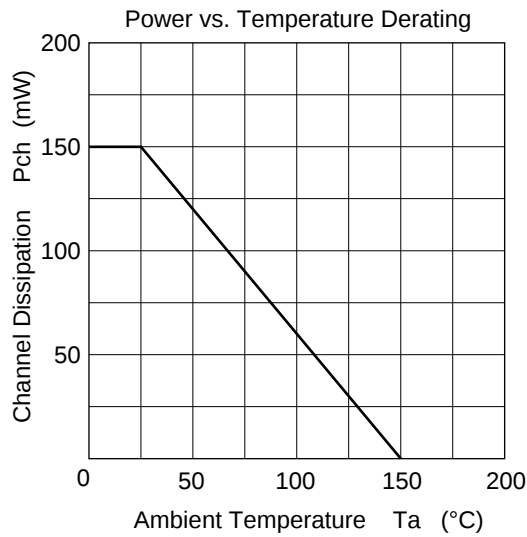
Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)

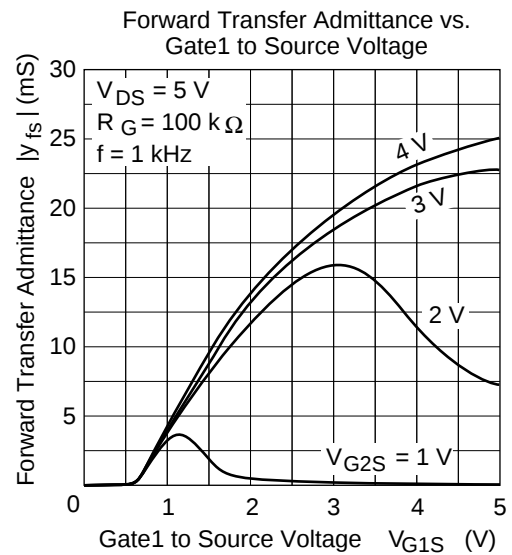
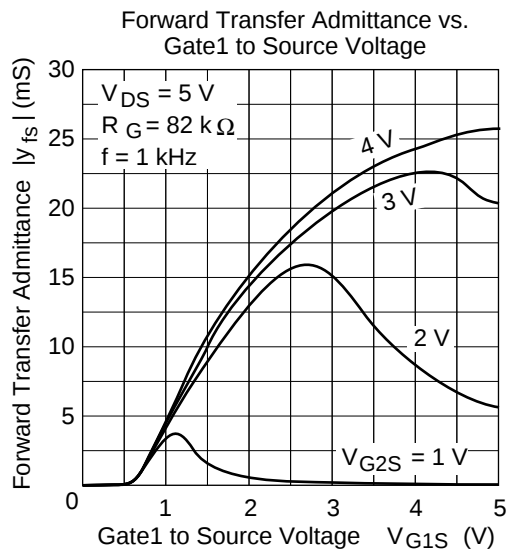
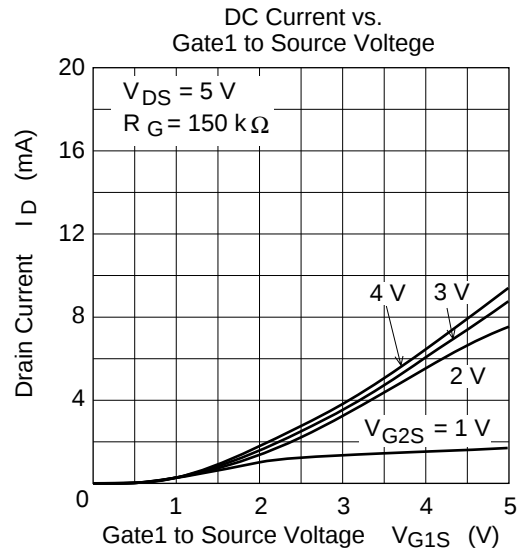
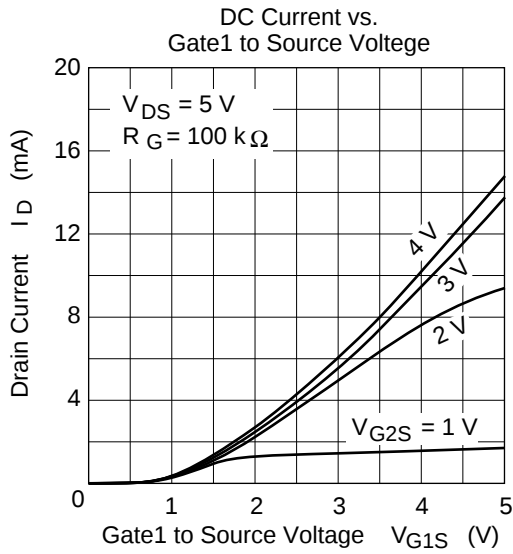


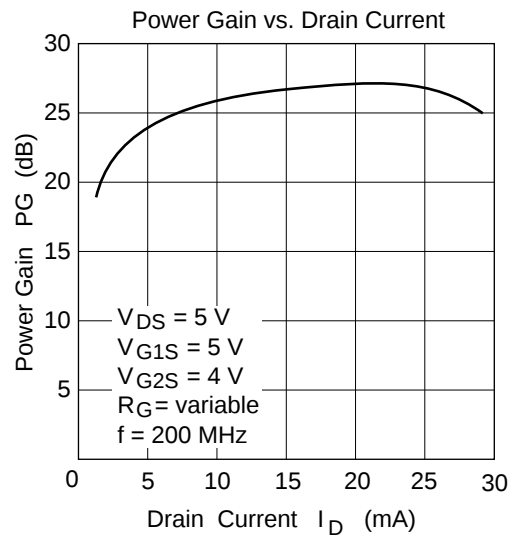
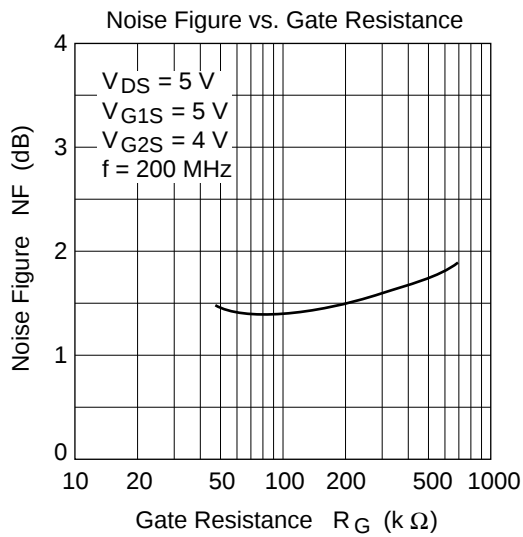
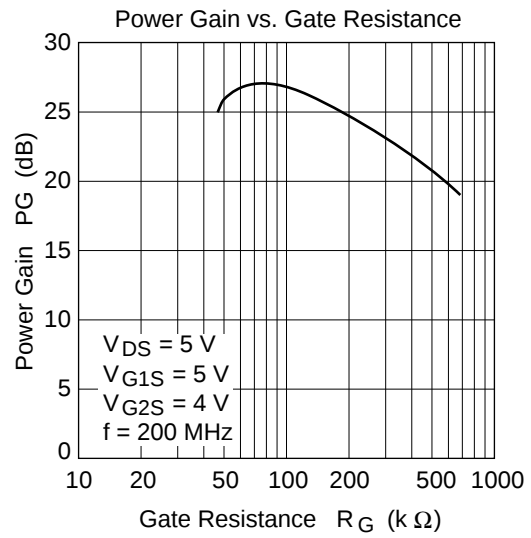
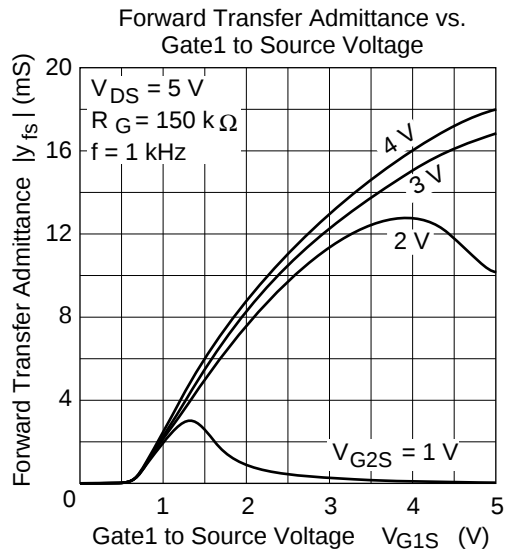
Power Gain, Noise Figure Test Circuit

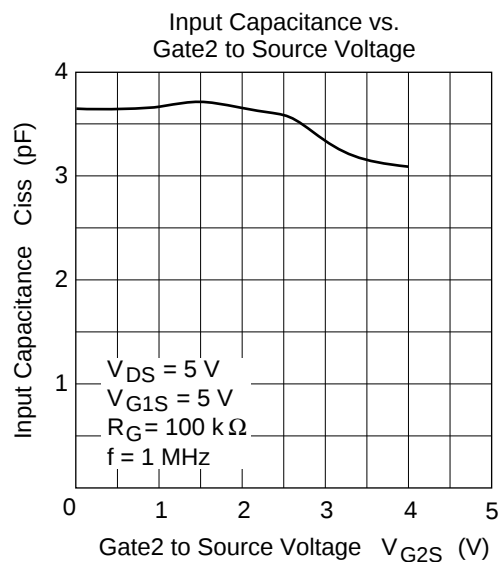
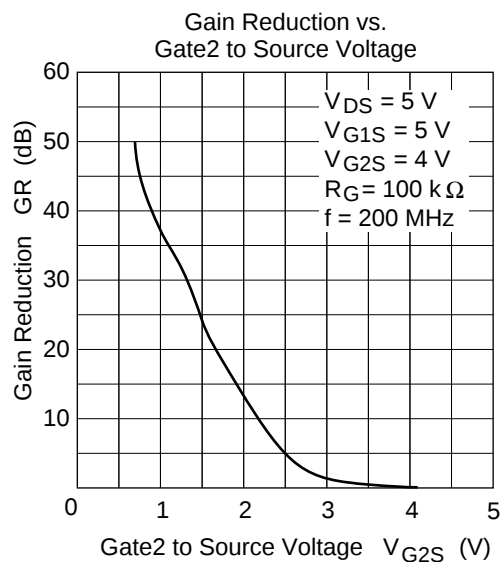
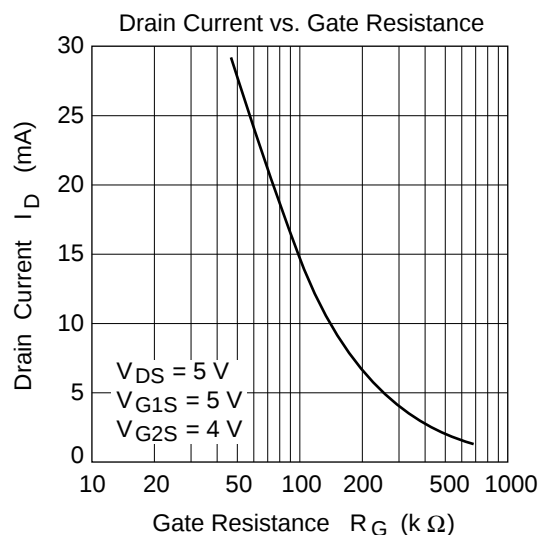
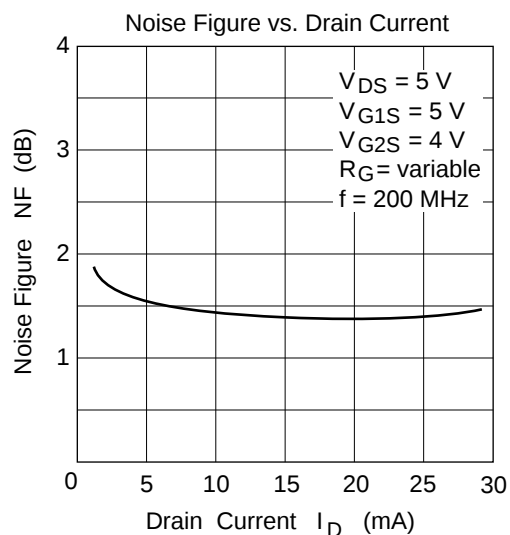


L1 : ϕ 1mm Enameled Copper Wire, Inside dia 10mm, 2Turns
 L2 : ϕ 1mm Enameled Copper Wire, Inside dia 10mm, 2Turns
 RFC : ϕ 1mm Enameled Copper Wire, Inside dia 5mm, 2Turns



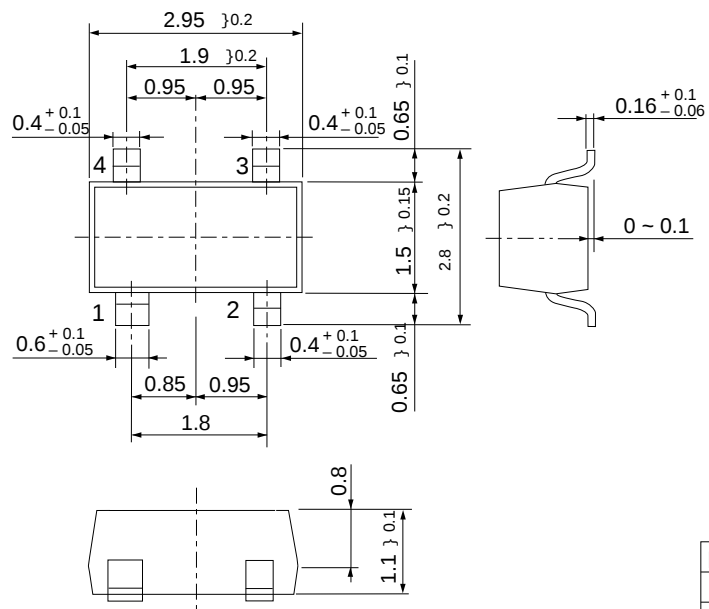






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Package Dimensions (Unit: mm)



Hitachi Code	MPAK-4R
EIAJ	—
JEDEC	—

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