

# Rechargeable Alkaline Charge/Discharge Controller IC

#### **Features**

- ➤ Safe charge of three or four rechargeable alkaline batteries such as Renewal® from Rayovac®
- ➤ Pulsed charge terminated with maximum voltage limit
- ➤ LED outputs indicate charge
- ➤ Selectable end-of-discharge voltage prevents overdischarge and improves cycle life
- Optional external FET drive allows high current loads
- Pre-charge qualification indicates fault conditions
- ➤ Automatic charge control simplifies charger design
- ➤ Available in 14-pin 300-mil DIP or 150-mil SOIC

### **General Description**

The bq2903 is a cost-effective charge controller for rechargeable alkaline batteries such as Renewal batteries from Rayovac. The bq2903 combines sensitive, full-charge detection for three to four rechargeable alkaline cells, with a low-battery cut-off for over-discharge protection.

Designed for integration into a threeor four-cell system, the bq2903 can improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge. The bq2903 requires a voltage-limited current source to generate the proper charge pulses for the Renewal cell. Each cell is individually monitored to ensure full charge without a damaging overcharge.

Charge completion is indicated when the average charge rate falls below

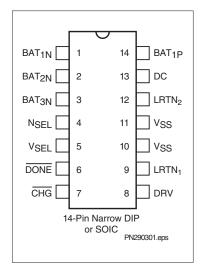
approximately 6% of the fast charge rate. Status outputs are provided to indicate charge in progress, charge complete, or fault condition.

The bq2903 avoids over-depleting the battery by using the internal end-of-discharge control circuitry. The bq2903 also eliminates the external power switching transistors needed to separately charge individual Renewal cells.

To reduce external component count, the discharge and charge control FETs are internal to the bq2903; however, if the discharge load is greater than 400mA, a DRV pin is provided to drive an external N-FET, reducing the effective discharge path resistance for the system.

For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is less than 0.4V when not charging (open-circuit voltage).

#### **Pin Connections**



#### **Pin Names**

DC	Charging supply input	BAT <sub>1N</sub>	Battery 1 negative input
$\overline{\text{CHG}}$	Battery status output 1	BAT <sub>2N</sub>	Battery 2 negative input
DONE	Battery status output 2	BAT <sub>3N</sub>	Battery 3 negative input
N <sub>SEL</sub>	Number of cells input	$V_{SS}$	Battery 4 negative input/
$V_{SEL}$	End of discharge		IC ground
	voltage select input	$LRTN_{1,2}$	System load returns
BAT <sub>1P</sub>	Battery 1 positive input	DRV	External FET drive output

## **Pin Descriptions**

#### DC DC supply input

This input is used to recharge the rechargeable alkaline cells and power the bq2903 during charge. This input must be connected to a voltage-limited current source.

#### CHG Charge status

This open-drain output is used to signify the battery charging status and is valid only when DC is applied. See Figure 4 and Table 1.

#### **DONE** Charge done

This open-drain output is used to signify charge completion and is valid only when DC is applied.

#### $N_{SEL}$ Number of cells input

This input selects whether the bq2903 charges 3 or 4 cells.  $N_{\rm SEL}$  = BAT<sub>1P</sub> selects 4 cells, and  $N_{\rm SEL}$  = V<sub>SS</sub> selects 3 cells.

#### V<sub>SEL</sub> End-of-discharge select input

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2903.  $V_{\rm SEL}$ 

= BAT\_{1P} selects an EDV of 1.10V.  $V_{\rm SEL}$  floating selects EDV = 1.0V.  $V_{\rm SEL}$  =V\_SS selects EDV = 0.9V.

#### BAT<sub>1P</sub> Battery 1 positive input

This input connects to the positive terminal of the battery designated BAT<sub>1</sub> (see Figure 3). This pin also provides power to the bq2903 when DC is not present.

#### BAT<sub>1N</sub> Battery 1 negative input

This input connects to the negative terminal of the battery designated  $BAT_1$  (see Figure 3).

#### BAT<sub>2N</sub> Battery 2 negative input

This input connects to the negative terminal of the battery designated  $BAT_2$  (see Figure 3).

#### BAT<sub>3N</sub> Battery 3 negative input

This input connects to the negative terminal of the battery designated  $BAT_3$  (see Figure 3).

#### V<sub>SS</sub> Battery 4 negative input/IC ground

This input connects to the negative terminal of the battery designated BAT<sub>4</sub> (see Figure 3).

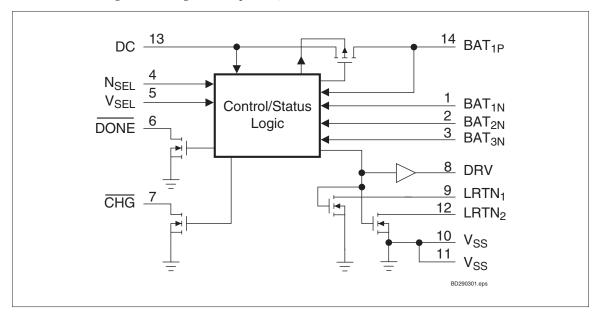


Figure 1. Functional Block Diagram

#### LRTN1, 2 Load returns

These open-drain pull-down outputs are typically used as low-side load switches. High-side load switching is also possible with the addition of an external P-FET

#### DRV External FET drive output

This push-pull output drives an optional external N-FET (see Figure 4). See page 5 for a full description.

## **Functional Description**

Figure 1 is a block diagram outlining the major components of the bq2903. Figure 2 illustrates the charge control and display status during a bq2903 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

#### **DC Input**

This input is used to charge the rechargeable alkaline cells and power the bq2903 during a charge. To charge the batteries, this input should be connected to a current source limited to 300mA. If the DC input current is greater than 300mA, the power dissipation limits of the package will be exceeded. The DC input should also be capable of supplying a minimum of 2.0V\*N, where N is the number of cells to be charged. The DC input should not exceed 10V.

#### **Charge Pre-Qualification**

After DC is applied, the bq2903 checks the open-circuit voltage (Vocv) of each cell for an undervoltage condition

 $(V_{OCV}<0.4V)$ . If the  $V_{OCV}$  of any cell is below  $V_{MIN}$ , the bq2903 enters a charge-pending mode and indicates a fault (see Table 1).

If all cells are above  $V_{MIN}$  and the minimum operating voltage VOP(min)=2.7V at the DC pin is met, the bq2903 will initiate a charge cycle. A charge cycle consists of pulse charging the battery and then checking for a termination condition.

#### **Charge Termination**

Once a charge cycle begins, the bq2903 terminates charge when the average charge rate falls below 6% of the maximum charge rate. The bq2903 also terminates charge when the closed-circuit voltage (V $_{\rm CCV}$ ) of any cell exceeds 3.0V (V $_{\rm FLT}$ ) during charge and indicates a fault condition on the  $\overline{\rm CHG}$  output (see Table 1).

#### **Charge Re-Initiation**

If DC remains valid, the bq2903 will suspend all charge activity after full-charge termination. A charge cycle is reinitiated when all cell potentials fall below 1.4V. The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal cells is typically 4% per year at room temperature.

#### Charge Status Indication

Table 1 and Figure 2 outline the various charge action states and the associated  $BAT_{1P}, \overline{CHG},$  and  $\overline{DONE}$  output states. The charge status outputs are designed to work with individual or tri-color LED indicators. In all cases, if the voltage at the DC pin is less than the voltage at the  $BAT_{1P}$  pin,  $\overline{CHG}$  and  $\overline{DONE}$  outputs are held in a high-impedance condition.

Table 1. bg2903 Operational Summary

Charge Action State	Conditions	BAT <sub>1P</sub> Input	CHG Output	DONE Output
DC absent	$V_{\rm DC} < V_{\rm BAT1P}$	-	Z	Z
Charge initiation	DC applied	-	-	-
Charge pending/ fault	$V_{\rm OCV}$ < $0.4 V^1$ or $V_{\rm CCV}$ > $3.0 V^2$	-	½ sec = Low ½ sec = Z	Z
Charge pulse	V <sub>OCV</sub> ≤ 1.63V before pulse	Charge pulsed @ 100Hz per Figure 1	Low	Z
Pulse skip	$V_{\rm OCV} > 1.63 V$ before pulse	Pulse skipped per Figure 1	Low	Z
Charge complete	Average charge rate falls below 6% of the fast charge rate	Charge complete	Z	Low

Notes:

- 1.  $V_{OCV}$  = Open-circuit voltage of each cell between positive and negative leads.
- 2.  $V_{CCV} = Closed$ -circuit voltage.

#### Charging

The bq2903 controls charging by periodically connecting the DC current source to the battery stack, not to the individual battery cells. The charge current is pulsed from the internal clock at approximately a 100 Hz rate on the BAT $_{1P}$  pin.

The bq2903 pulse charges the battery for approximately 7.5ms of every 10ms, when conditions warrant. The bq2903 measures the open circuit voltage (Vocv) of each battery cell during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (VMAX = 1.63V  $\pm 3\%$ ), the following pulses are skipped until all cell potentials fall below the VMAX limit. Charging is terminated when the average charge rate falls below approximately 6% of the maximum charge rate. Once charging is terminated, the internal charging FET remains off, and the  $\overline{\rm DONE}$  output becomes active per Table 1 and Figure 2. With DC applied, the internal discharge FET will always remain on, and the DRV output will remain high.

#### **End-of-Discharge Control**

When DC is less than the voltage on BAT1P, the bq2903 is powered by the battery at BAT1P. In this state, the batteries discharge down to the level determined by the  $V_{\rm SEL}$  pin. The end-of-discharge voltage ( $V_{\rm EDV}$ ) is selectable by connecting the  $V_{\rm SEL}$  pin as outlined in Table 2. If the voltage across any cell is below the voltage specified by the  $V_{\rm SEL}$  input, the bq2903 disconnects the battery stack from the load by turning the internal discharge FET off. The DRV output is also driven low, disabling the external FET. After disconnecting power (the battery stack) to the load, the standby current in the bq2903 is reduced to less than  $1\mu A$ . Typically, higher discharge loads (>200mA) should use a lower discharge voltage cut-off to maximize battery capacity.

After disconnecting the battery stack from the load, the internal discharge FET remains off, and the DRV output remains low until the batteries are replaced or DC is reapplied, initiating a new charge cycle.

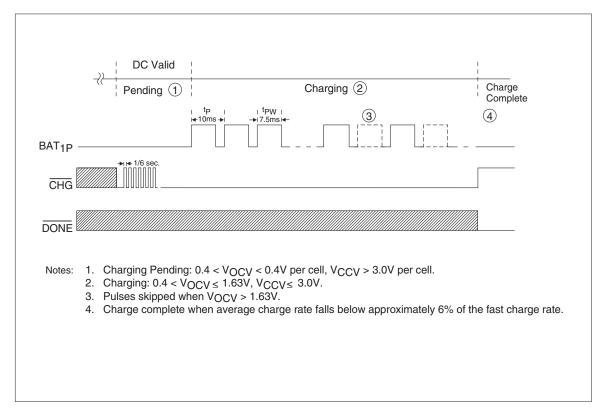


Figure 2. bq2903 Example of Charge Action Events

Table 2. bq2903 EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{\rm SEL}$ = BAT <sub>1P</sub>
1.00V	$V_{\mathrm{SEL}} = Z$
0.90V	$V_{\mathrm{SEL}} = V_{\mathrm{SS}}$

#### **Number-of-Cell Selection**

 $N_{\rm SEL}$  is used to select whether the bq2903 will charge 3 or 4 cells. Figure 3 shows the proper connection for a 3-or 4-cell system. For 4 cell operation,  $N_{\rm SEL}$  = BAT $_{1P}$ . For 3 cell operation,  $N_{\rm SEL}$  =  $V_{\rm SS}$  and the BAT $_{2N}$  pin should be connected to the BAT $_{3N}$  pin.

#### **DRV Pin**

The bq2903 controls battery discharge with two internal FETs between LRTN1, LRTN2, and Vss. The current through each switch should be limited to 200mA. LRTN1 can be tied to LRTN2 for discharge current of up to 400mA. To reduce the effective discharge switch resistance, or for high current loads, the DRV pin can control an external N-FET, as shown in Figure 4. DRV is "high" when a valid charging voltage is applied to the DC pin and remains "high" during discharge. DRV goes "low" during discharge to turn off the external FET when an end-of-discharge condition is met. This pin should not be connected if the external FET option is not used.

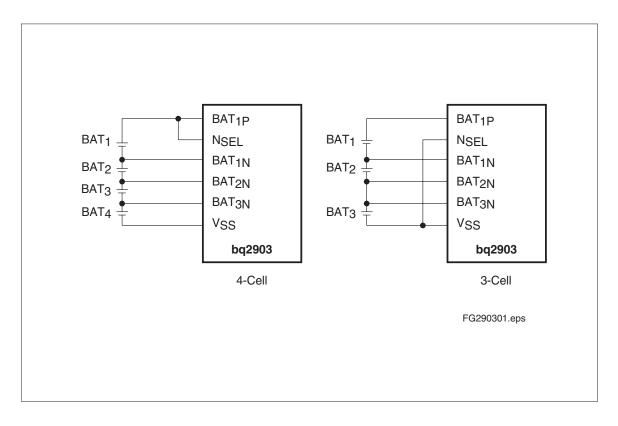


Figure 3. NSEL Connection Diagram

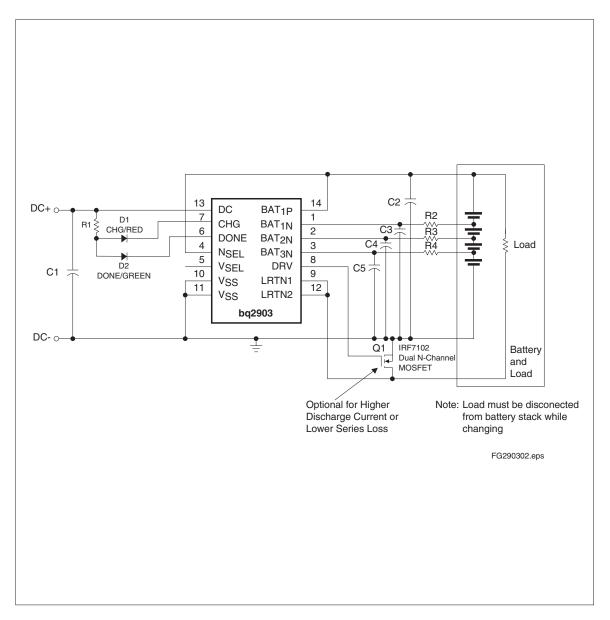


Figure 4. bq2903 Application Example, 4–Cell and 1.0V EDV

## **Absolute Maximum Ratings**

Symbol	Parameter	Minimum	Maximum	Unit	Notes
$\mathrm{DC_{IN}}$	$V_{ m DC}$	-0.3	11.0	V	
$V_{\mathrm{T}}$	DC threshold voltage applied on any pin, excluding DC pin	-0.3	11.0	V	
TOPR	Operating ambient temperature	0	+70	$^{\circ}\mathrm{C}$	Commercial
$T_{STG}$	Storage temperature	-40	+85	$^{\circ}\mathrm{C}$	
$T_{ m SOLDER}$	Soldering temperature	-	+260	°C	10 sec max.
$I_{DC}$	DC charging current	-	400	mA	
I <sub>LOAD</sub>	Discharge current	-	500	mA	No external FET
$I_{\mathrm{OL}}$	Output current	-	20	mA	$\overline{\text{CHG}},\overline{\text{DONE}}$

Note:

Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

# bq2903

## DC Thresholds (TA = 25°C; VDC =10V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V <sub>MAX</sub>	Maximum open-circuit voltage	1.63	±3%	V	$\label{eq:Vocv} V_{OCV} > V_{MAX} \ inhibits \ or \ terminates \\ charge \ pulses$
		0.90	±5%	V	$V_{ m SEL} = V_{ m SS}$
$V_{ m EDV}$	End-of-discharge voltage	1.00	±5%	V	$V_{ m SEL} = Z$
		1.10	±5%	V	$V_{\rm SEL} = {\rm BAT_{1P}}$
$V_{\mathrm{FLT}}$	Maximum closed-circuit voltage	3.00	±5%	V	$\label{eq:VCCV} V_{CCV} > V_{FLT} \ terminates \ charge, \ indicates fault$
V <sub>MIN</sub>	Minimum battery voltage	0.40	±5%	V	$V_{\rm OCV} < V_{\rm MIN}$ inhibits charge
$ m V_{CE}$	Charge enable	1.40	±5%	V	$V_{\rm OCV} < V_{\rm CE} \ on \ all \ cells \ re\text{-initiates}$ charge

Note:

Each parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$Tempco = \frac{ParameterRating}{1.63} * -0.5mV/^{\circ}C$$

The tolerance for these temperature coefficients is 10%.

## **Timing** $(T_A = 25^{\circ}C)$

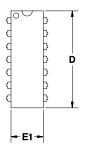
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$t_{\mathrm{P}}$	Pulse period	-	10	-	ms	See Figure 2
tpw	Pulse width	-	7.5	-	ms	See Figure 2

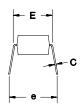
# DC Electrical Characteristics (TA = TOPR)

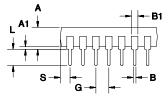
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$V_{\mathrm{IH}}$	Logic input high	V <sub>BAT1P</sub> - 0.1	-	$V_{\mathrm{BAT1P}}$	V	V <sub>SEL</sub> , N <sub>SEL</sub>
$V_{\rm IL}$	Logic input low	$ m V_{SS}$	-	$V_{\rm SS}$ + 0.1	V	V <sub>SEL</sub> , N <sub>SEL</sub>
$V_{ m OL}$	Logic output low	-	-	1.0	v	$\overline{\text{DONE}}, \overline{\text{CHG}},$ $I_{\text{OL}} = 5\text{mA}$
		-	-	0.4	V	I <sub>OL</sub> = 1.0mA, DRV
V <sub>OH</sub>	Gate drive output	(Greater of $V_{\rm BAT1P}$ or $V_{\rm DC}$ ) - 1.0	-	-	v	DRV, I <sub>OH</sub> = -1.0mA
$I_{ m OL}$	Output current	5	-	-	mA	$\frac{V_{OL} = V_{SS} + 1.0V, \overline{CHG}}{\overline{DONE}}$
	•	1	-	-	mA	$DRV = V_{SS} + 1.0V$
$I_{DC}$	Supply current	-	35	250	μА	Outputs unloaded, $V_{\rm DC} = 10.0 V$
$I_{\mathrm{SB1}}$	Standby current	-	25	40	μΑ	$\begin{aligned} V_{\mathrm{DC}} &= 0, V_{\mathrm{OCV}} > V_{\mathrm{EDV}}, \\ \mathrm{BAT}_{\mathrm{1P-3N}} \end{aligned}$
$I_{\mathrm{SB2}}$	End-of-discharge standby current	-	-	1	μΑ	$V_{DRV} = 0V, V_{DC} = 0$
${ m I_L}$	Input leakage	-	-	±1	μΑ	NSEL
$I_{OZ}$	Output leakage in high-Z state	-	-	±5	μА	$\overline{\mathrm{CHG}},\overline{\mathrm{DONE}}$
$R_{ m DSON}$	Discharge on resistance	-	0.5	-	Ω	
$I_{LOAD}$	Discharge current without external N-FET	-	-	400	mA	No external FET; LRTN1 (pin 9) must be tied to LRTN2 (pin 12).
$I_{\mathrm{IL}}$	Logic input low	-	-	70	μА	$V$ = GND to GND + 0.5V, $V_{\rm SEL}$
$I_{\mathrm{IH}}$	Logic input high	-70	-	-	μA	$V = V_{\rm DC}$ -0.5 to $V_{\rm DC},V_{\rm SEL}$
$I_{\rm IZ}$	Logic input float	-2	-	2	μА	$ m V_{SEL}$
$I_{DC}$	DC charging current	-	-	300	mA	
V <sub>OP</sub>	Operating voltage	2.7	-	10	V	

Note: All voltages relative to  $V_{\rm SS}$ .

PN: 14-Pin DIP (0.300")



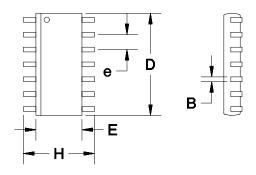


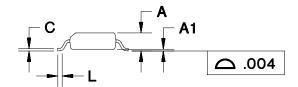


14-Pin PN (0.300" DIP)

	Incl	hes	Millimeters		
Dimension	Min. Max.		Min.	Max.	
A	0.160	0.180	4.06	4.57	
A1	0.015	0.040	0.38	1.02	
В	0.015	0.022	0.38	0.56	
B1	0.055	0.065	1.40	1.65	
C	0.008	0.013	0.20	0.33	
D	0.740	0.770	18.80	19.56	
E	0.300	0.325	7.62	8.26	
E1	0.230	0.280	5.84	7.11	
e	0.300	0.370	7.62	9.40	
G	0.090	0.110	2.29	2.79	
L	0.115	0.150	2.92	3.81	
S	0.070	0.090	1.78	2.29	

SN: 14-Pin SN (0.150" SOIC)





14-Pin SN (0.150" SOIC)

	Inc	hes	Millimeters			
Dimension	Min. Max.		Min.	Max.		
A	0.060	0.070	1.52	1.78		
A1	0.004	0.010	0.10	0.25		
В	0.013	0.020	0.33	0.51		
C	0.007	0.010	0.18	0.25		
D	0.335	0.350	8.51	8.89		
E	0.150	0.160	3.81	4.06		
e	0.045	0.055	1.14	1.40		
Н	0.225	0.245	5.72	6.22		
L	0.015	0.035	0.38	0.89		

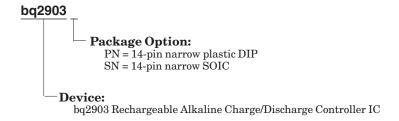
## **Data Sheet Revision History**

Change No.	Page No.	Description	Nature of Change
1	1	Pin connections	LRTN1 (pin 9) was LRTN, LRTN2 (pin 12) was LRTN
1	2	Functional block diagram	Updated block diagram
1	3	Pin description	Added descriptions for LRTN1 and LRTN2
1	5	DRV pin	Clarified LRTN1 and LRTN2 description
1	6	Application example	Corrected schematic
1	9	$R_{ m DSON}$ and $I_{ m LOAD}$ specification	Added notes on LRTN1 and LRTN2
2	7	$T_{\mathrm{OPR}}$	Deleted industrial temperature range

Notes: (

Change 1 = May 1999 B changes from July 1996. Change 2 = June 1999 C changes from May 1999 B

# **Ordering Information**



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