

## MULTI-RATE 10 Gbps 1:16 DEMUX WITH CDR

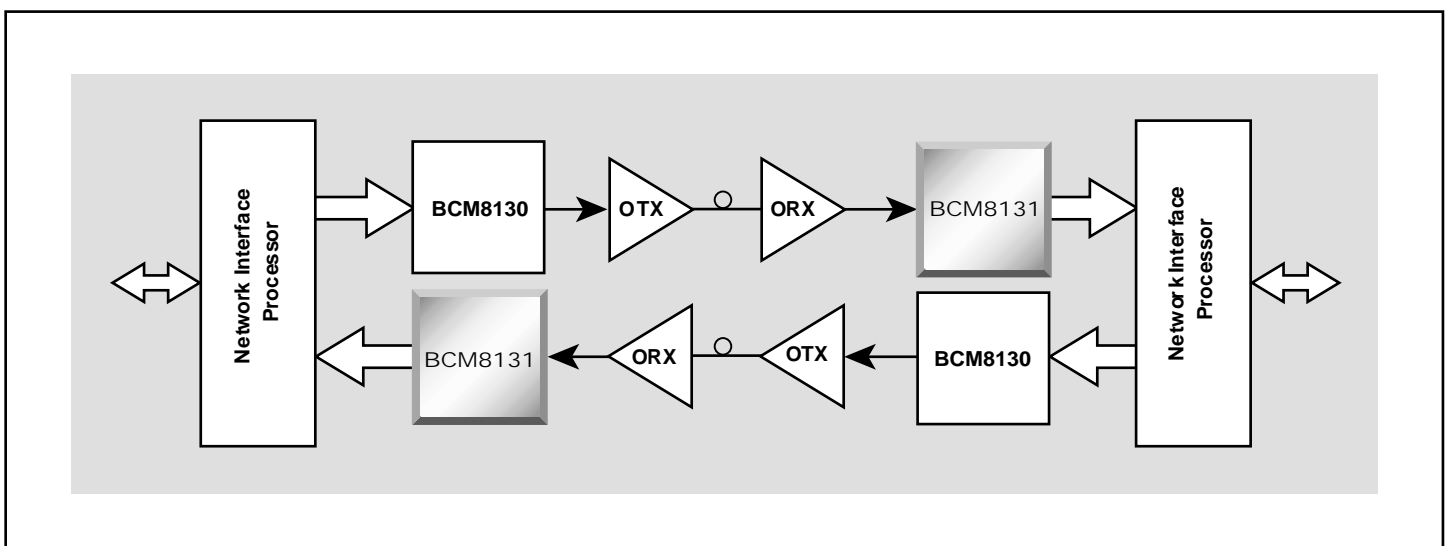
### BCM8131 FEATURES

- Fully integrated clock and data recovery (CDR) and demultiplexer (DEMUX)
- Support for multiple rates — OC-192: 9.953 Gbps, OC-192 FEC: 10.664 and 10.709 Gbps, 10G Ethernet: 10.3125 Gbps
- 1:16 demultiplexer with LVDS parallel data and clock outputs
- Lock detect
- Loss-of-signal detect
- Exceeds SONET jitter requirements
- Core power supply: 1.8V
- I/O power supply: CML, LVDS and LVPECL at 1.8V, CMOS at 1.8V or 3.3V
- Power consumption: 900 mW typical @ 1.8V
- Standard CMOS fabrication process
- 15 x 15 mm, 120-pin BGA package

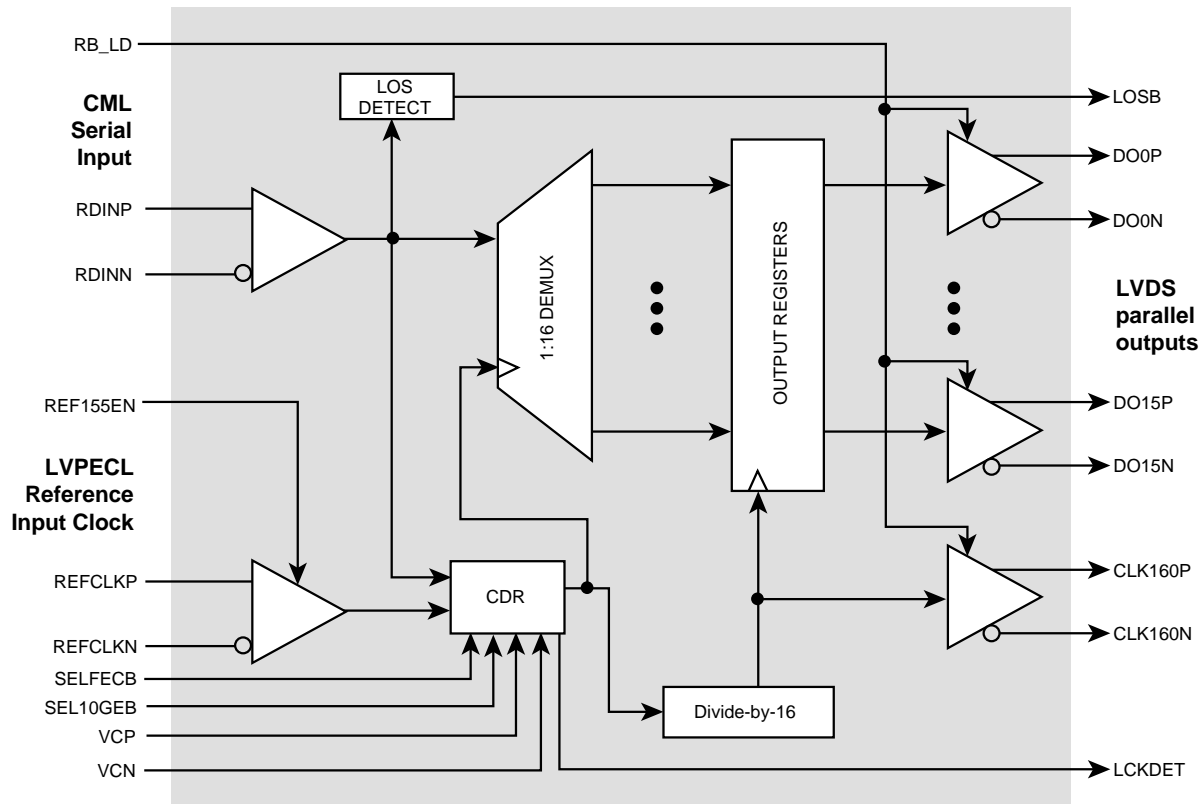
### SUMMARY OF BENEFITS

- Compliant with Optical Internetworking Forum (OIF), Telcordia, ITU-T, and IEEE 802.3ae industry standards.
- Reduces design cycle and time to market.
- High level of integration allows for higher port density solutions.
- CMOS-based device uses the most effective silicon economy of scale.
- Low power consumption eliminates the need for external cooling sources.
- Target applications:
  - Transmission equipment
  - Optical modules
  - ADD/DROP multiplexers
  - Digital cross-connects
  - ATM switch backbone
  - Test equipment
  - Terabit routers
  - Edge routers
  - LAN/WAN switch
  - Switch router backbone
  - Hubs and repeaters
  - Network Interface Cards (NIC)

Application Block Diagram



# Block Diagram



The **BCM8131** is a fully integrated multi-rate SONET/SDH/10GE receiver operating at the OC-192/STM-64 (9.953 Gbps), 10GE (10.3125 Gbps), and FEC (Forward Error Correction) data rates (10.664 and 10.709 Gbps) with deserializer, CDR, and loss-of-signal (LOS) detection circuitry.

The **BCM8131** provides high-jitter tolerance and low-jitter generation to comply with Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T standards.

The **BCM8131** reference clock frequency is user-selectable to either the line rate divided by 16 or the line rate divided by 64. The reference clock output and the LVDS receive parallel bus output can be squelched under user control.

The major receiver functions are:

- Configurable multi-rate CDR and data rates
- CML receive serial data input
- 16-bit parallel LVDS output
- Selectable reference clock frequencies
- Serial-to-parallel conversion
- Lock detect
- Loss of signal

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