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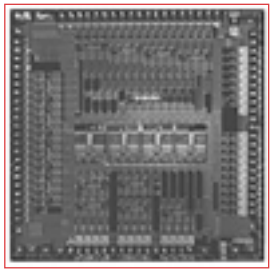
BCM8511B
PRODUCT Brief



10G DWDM TRANSPORT PROCESSOR

BCM8511B FEATURES

- Provides FEC statistics: total corrected bits, corrected bytes and uncorrectable blocks.
- Bi-directional SONET/SDH performance monitor
- Extracts and inserts OTU and SONET/SDH section and line overhead bytes.
- Extracts and inserts DCC and GCC bytes.
- Performs frame and byte alignment on received OTU and SONET/SDH frames.
- Scrambles and unscrambles OTU and SONET/SDH frames.
- Monitors and reports OOF/LOS/LOF/SD/SF/ LOM/OOM for OTU and SONET/SDH frames.
- Monitors K1/K2 to report APS/AIS/RDI conditions.
- Inserts AIS on SONET/SDH frames.
- Monitors M1 to report REI on SONET/SDH frames.
- Monitors S1 for mismatch and inconsistent values.
- Monitors and reports J0 byte messages.
- Monitors B1/B2 to report parity errors on SONET/SDH frames.
- Generates and inserts B1/B2 bytes on SONET/SDH frames.
- Includes integrated 10G transceiver (9.953, 10.037, 10.312, 10.664 and 10.709 Gbps).

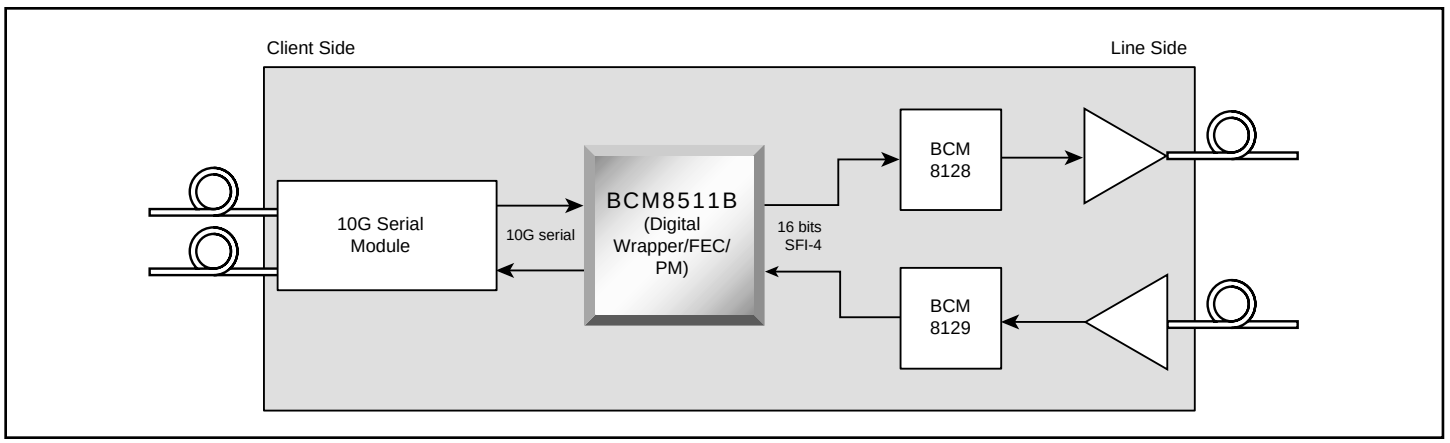
SUMMARY OF BENEFITS

- G.709 digital wrapper
- G.975 Reed-Solomon RS(255,239) FEC
- Ultra-low power consumption: 2.5W
- Industry's first and only 10G Digital Wrapper/FEC/PM chip with integrated 10G transceiver
- Bi-directional device with separate receive and transmit paths
- Transparent error correction and detection
- Integrated cleanup PLL with external VCXO
- Seamless connection to Broadcom MUX/DEMUX devices using SFI-4 interface
- Compact, low-profile package: 31mm x 31mm, HSBGA
- Standard 0.18µ CMOS process
- SFI-4 parallel interface (622, 627, 644, 666 and 669 Mbps)
- 16-bit microprocessor interface
- IEEE 1149.1 JTAG

KEY APPLICATIONS

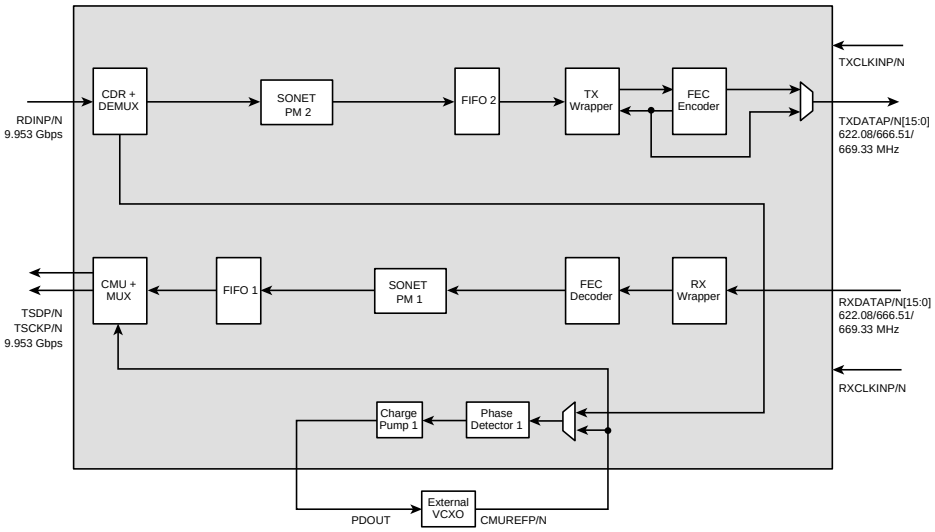
- DWDM long haul transport
- DWDM metro transport
- Next-generation SONET/SDH multiplexers
- Digital cross-connects
- Fiber optic terminators and test equipment

10G DWDM Transport Line Card



BCM8511B OVERVIEW

Top Level Block Diagram



The **BCM8511B** is a single-chip 10G DWDM transport processor that supports the following major functions on a DWDM line card:

- Integrated 9.953/10.664/10.709 Gbps transceiver
- G.709 Digital Wrapper (DW)
- G.975 Forward Error Correction (FEC), RS(255,239)
- SONET/SDH performance monitor (PM)

The device includes flexible data interface options. Both data inputs and outputs are independently programmable as 10G serial data or 16-bit (LVDS) parallel clock and data. The **BCM8511B** also has flexible modes of operation:

- Digital wrapper with FEC
- Optional SONET/SDH PM digital wrapper without FEC
- Optional SONET/SDH PM
- SONET/SDH PM with digital wrapper and FEC bypassed

The integrated transceiver performs the clock and data recovery (CDR) and the demultiplexing functions on the serial input data. It performs the clock multiplication (CMU) and the multiplexing functions to produce the serial output data. The transceiver is data-rate programmable to support the OC-192 SONET/SDH rate (9.953G), the G.975 FEC rate (10.664G), and the new G.709 FEC rate (10.709G).

The **BCM8511B** performs digital wrapper frame and byte alignment, overhead extraction, and performance monitoring on the input data. FEC and correction statistics are performed on the frame and byte aligned digital wrapper frames. SONET/SDH section and line overhead byte extraction/insertion and performance monitoring are performed on the FEC-corrected data.

All necessary performance monitor functions for SONET/SDH section and line overhead bytes are provided for Operations, Administration, Maintenance, and Provisioning (OAM&P). These functions include error checking, overhead data extraction, and insertion. Detected errors and accumulated error counts are accessible through a microprocessor port. Optionally, digital wrapper overhead bytes can be inserted into the data stream. Processed frames are FEC-encoded and serialized in the transceiver.

Related Documents and Collateral

- **BCM8511B** data sheet
- **BCM8511B** EVM user manual
- **BCM8511B** EVM quick start guide

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
FAX: 949-450-8710
Email: info@broadcom.com
Web: www.broadcom.com