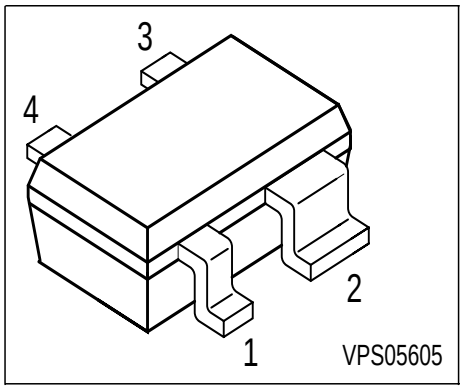
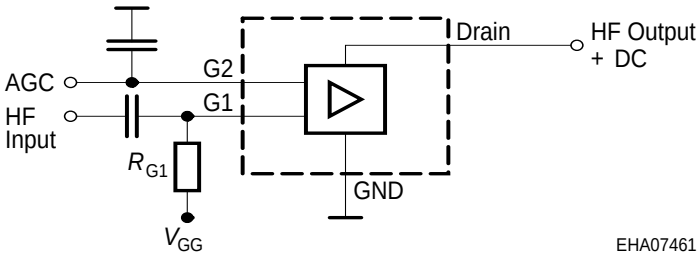
Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 5V





ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Class 2 (2000V - 4000V) pin to pin **H**uman **B**ody **M**odel

Type	Marking	Pin Configuration				Package
BF2030W	NEs	1 = D	2 = S	3 = G1	4 = G2	SOT343

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuos drain current	I_D	20	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	6	V
Total power dissipation, T_S = 94 °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point[1)]	R_{thchs}	≤280	K/W

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

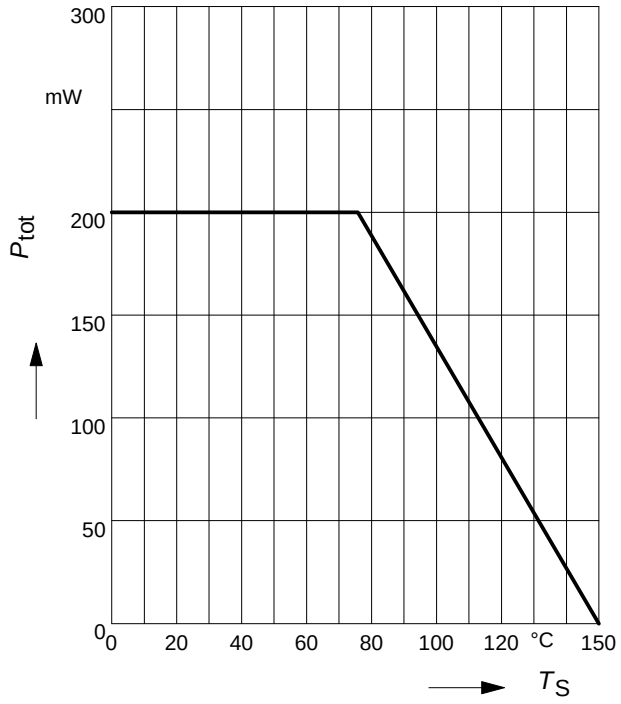
Electrical Characteristics at T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage I_D = 20 µA, V_{G1S} = 0 V, V_{G2S} = 0 V	$V_{(BR)DS}$	10	-	-	V
Gate 1 - source breakdown voltage $+I_{G1S}$ = 10 mA, V_{G2S} = 0 V, V_{DS} = 0 V	$+V_{(BR)G1SS}$	6	-	15	
Gate 2 - source breakdown voltage $+I_{G2S}$ = 10 mA, V_{G1S} = 0 V, V_{DS} = 0 V	$+V_{(BR)G2SS}$	6	-	15	
Gate 1 source leakage current V_{G1S} = 5 V, V_{G2S} = 0 V, V_{DS} = 0 V	$+I_{G1SS}$	-	-	50	nA
Gate 2 source leakage current V_{G2S} = 5 V, V_{G1S} = 0 V, V_{DS} = 0 V	$+I_{G2SS}$	-	-	50	nA
Drain current V_{DS} = 5 V, V_{G1S} = 0 V, V_{G2S} = 4 V	I_{DSS}	-		50	µA
Drain-source current V_{DS} = 5 V, V_{G2S} = 4 V, R_{G1} = 100 kΩ	I_{DSX}	-	12	-	mA
Gate 2-source pinch-off voltage V_{DS} = 5 V, I_D = 20 µA	$V_{G2S(p)}$	0.3	0.6	-	V
Gate 1-source pinch-off voltage V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 20 µA	$V_{G1S(p)}$	0.3	0.5	-	

Electrical Characteristics at T_A = 25 °C, unless otherwise specified.

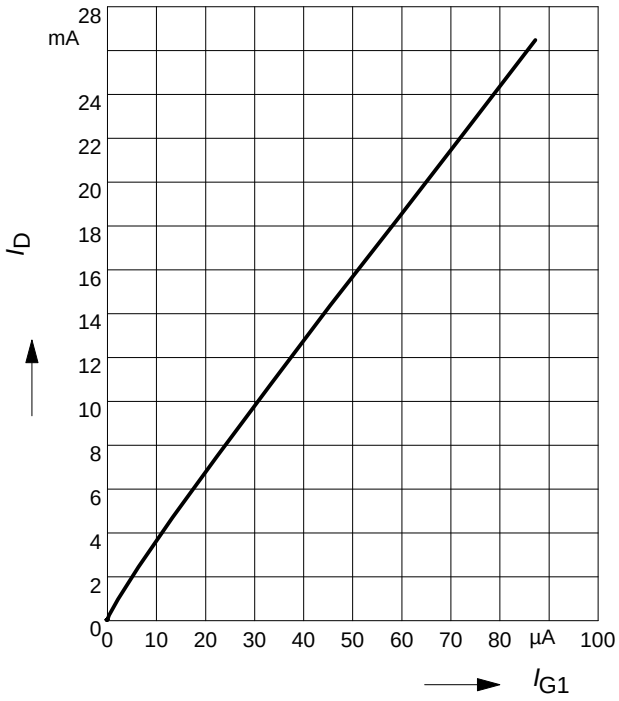
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics					
Forward transconductance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V	g_{fs}	-	31	-	mS
Gate 1 input capacitance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{g1ss}	-	2.4	-	pF
Output capacitance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{dss}	-	1.3	-	
Power gain V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800 MHz	G_{ps}	20	23	-	dB
Noise figure V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800 MHz	F	-	1.5	2.2	
Gain control range V_{DS} = 5 V, VG2S = 4 ... 0V, f = 800 MHz	ΔG_{ps}	45	50	-	

Total power dissipation $P_{tot} = f(T_S)$



Drain current $I_D = f(I_{G1})$

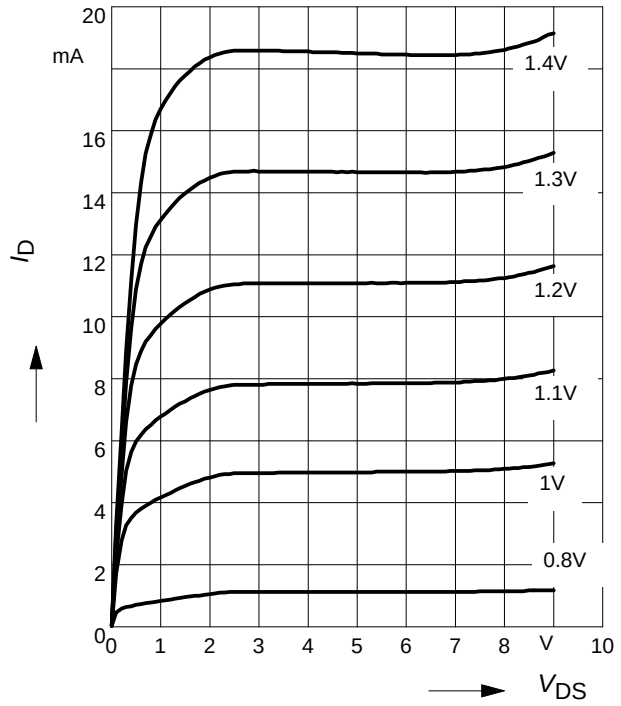
V_{G2S} = 4 V



Output characteristics $I_D = f(V_{DS})$

V_{G2S} = 4 V

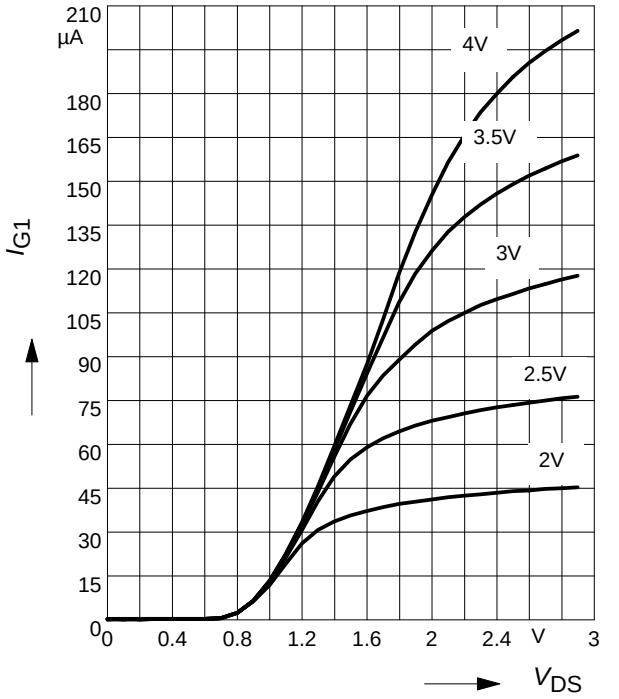
V_{G1S} = Parameter



Gate 1 current $I_{G1} = f(V_{G1S})$

V_{DS} = 5 V

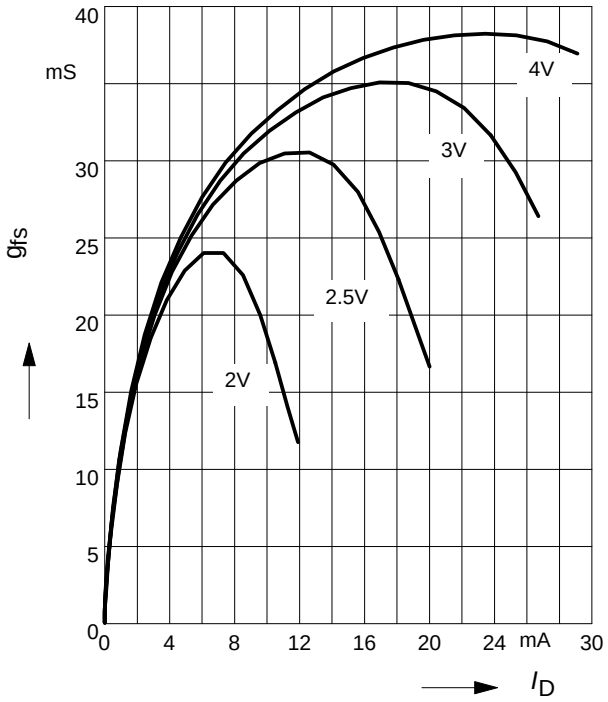
V_{G2S} = Parameter



Gate 1 forward transconductance

$g_{fs} = f(I_D)$

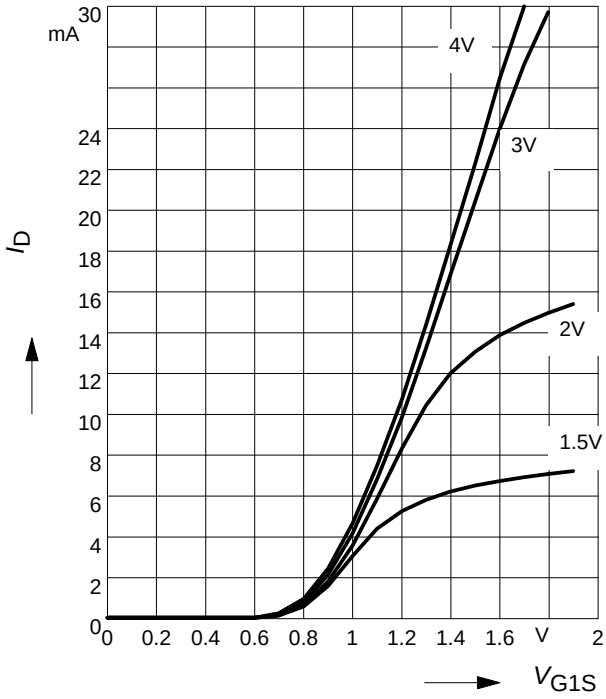
V_{DS} = 5 V, V_{G2S} = Parameter



Drain current $I_D = f(V_{G1S})$

V_{DS} = 5 V

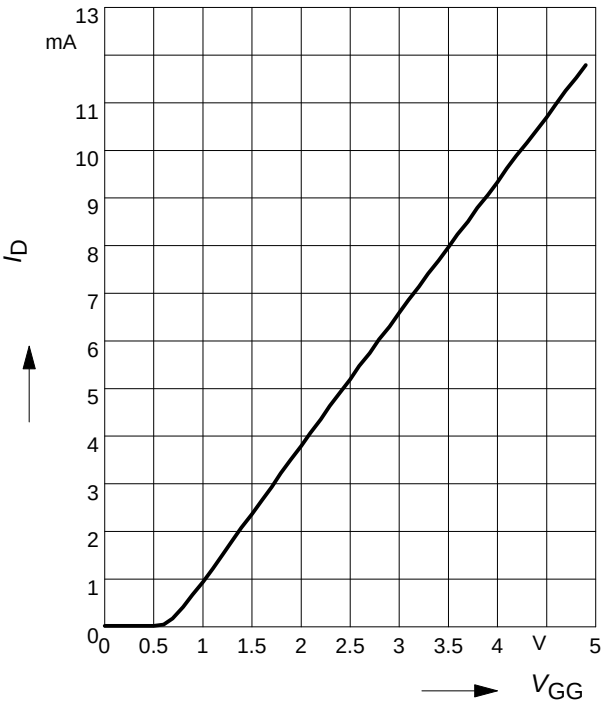
V_{G2S} = Parameter



Drain current $I_D = f(V_{GG})$

V_{DS} = 5 V, V_{G2S} = 4 V, R_{G1} = 100 kΩ

(connected to V_{GG}, V_{GG}=gate1 supply voltage)



Drain current $I_D = f(V_{GG})$

V_{G2S} = 4 V

R_{G1} = Parameter in kΩ