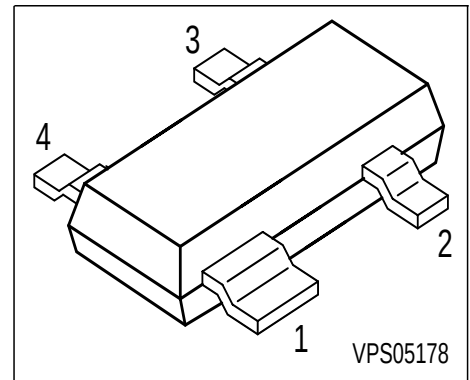
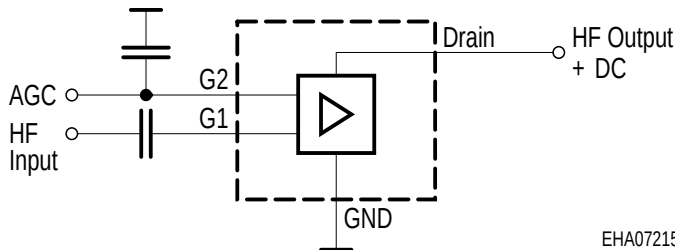


## Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 12V
- Integrated stabilized bias network



**ESD:** Electrostatic discharge sensitive device, observe handling precaution!

| Type    | Marking | Pin Configuration |       |        |        | Package |
|---------|---------|-------------------|-------|--------|--------|---------|
| BF1012S | NYS     | 1 = S             | 2 = D | 3 = G2 | 4 = G1 | SOT143  |

### Maximum Ratings

| Parameter                                            | Symbol           | Value       | Unit             |
|------------------------------------------------------|------------------|-------------|------------------|
| Drain-source voltage                                 | $V_{DS}$         | 16          | V                |
| Continuous drain current                             | $I_D$            | 25          | mA               |
| Gate 1/gate 2 peak source current                    | $\pm I_{G1/2SM}$ | 10          |                  |
| Gate 1 (external biasing)                            | $+V_{G1SE}$      | 3           | V                |
| Total power dissipation, $T_S \leq 76^\circ\text{C}$ | $P_{tot}$        | 200         | mW               |
| Storage temperature                                  | $T_{stg}$        | -55 ... 150 | $^\circ\text{C}$ |
| Channel temperature                                  | $T_{ch}$         | 150         |                  |

### Thermal Resistance

|                                         |             |            |     |
|-----------------------------------------|-------------|------------|-----|
| Channel - soldering point <sup>1)</sup> | $R_{thchs}$ | $\leq 370$ | K/W |
|-----------------------------------------|-------------|------------|-----|

<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

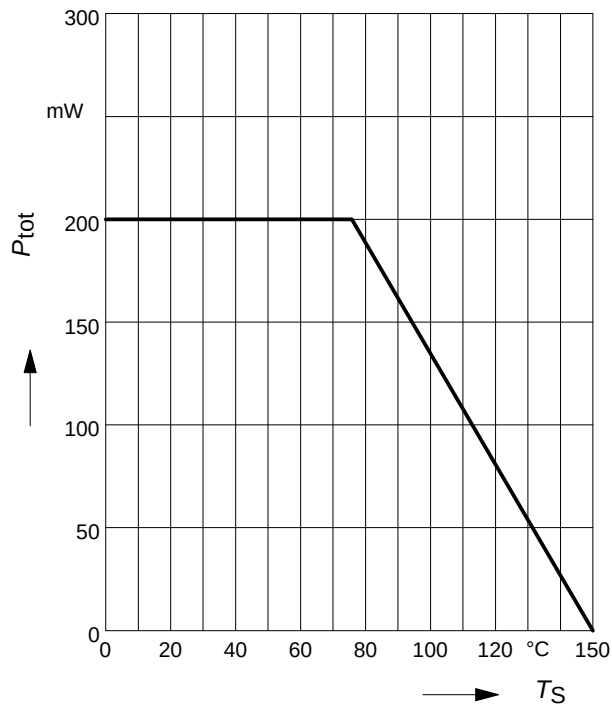
### Note:

It is not recommended to apply external DC-voltage on Gate 1 in active mode.

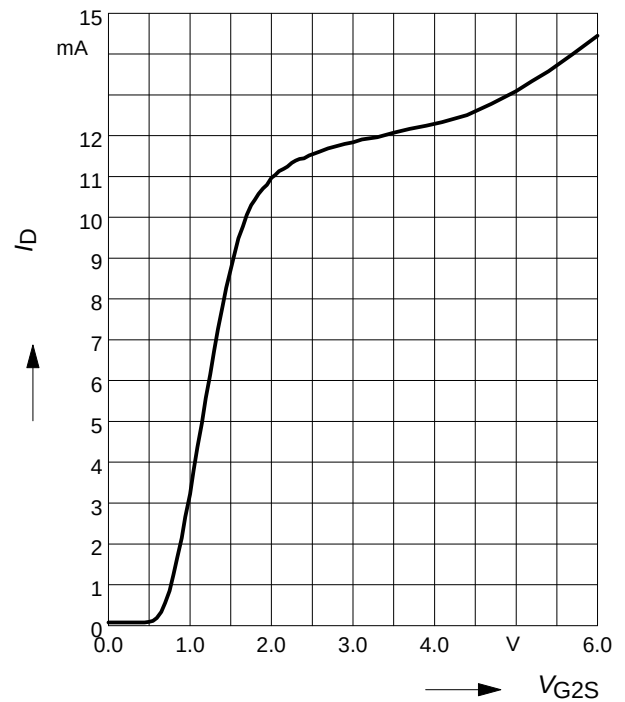
**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

| Parameter                                                                                                                         | Symbol                           | Values |      |      | Unit          |
|-----------------------------------------------------------------------------------------------------------------------------------|----------------------------------|--------|------|------|---------------|
|                                                                                                                                   |                                  | min.   | typ. | max. |               |
| DC characteristics                                                                                                                |                                  |        |      |      |               |
| Drain-source breakdown voltage<br>$I_D = 300\ \mu\text{A}$ , $V_{G1S} = 0\ \text{V}$ , $V_{G2S} = 0\ \text{V}$                    | $V_{(\text{BR})\text{DS}}$       | 16     | -    | -    | V             |
| Gate 1 - source breakdown voltage<br>$+I_{G1S} = 10\ \text{mA}$ , $V_{G2S} = 0\ \text{V}$ , $V_{\text{DS}} = 0\ \text{V}$         | $+V_{(\text{BR})\text{G1SS}}$    | 8      | -    | 12   |               |
| Gate 2 source breakdown voltage<br>$\pm I_{G2S} = 10\ \text{mA}$ , $V_{G1S} = 0\ \text{V}$ , $V_{\text{DS}} = 0\ \text{V}$        | $\pm V_{(\text{BR})\text{G2SS}}$ | 10     | -    | 16   |               |
| Gate 1 source current<br>$V_{G1S} = 6\ \text{V}$ , $V_{G2S} = 0\ \text{V}$                                                        | $+I_{\text{G1SS}}$               | -      | -    | 60   | $\mu\text{A}$ |
| Gate 2 source leakage current<br>$\pm V_{G2S} = 8\ \text{V}$ , $V_{G1S} = 0\ \text{V}$ , $V_{\text{DS}} = 0\ \text{V}$            | $\pm I_{\text{G2SS}}$            | -      | -    | 50   | nA            |
| Drain current<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G1S} = 0$ , $V_{G2S} = 6\ \text{V}$                                         | $I_{\text{DSS}}$                 | -      | -    | 500  | $\mu\text{A}$ |
| Operating current (selfbiased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6\ \text{V}$                                        | $I_{\text{DSO}}$                 | 8      | 12   | -    | mA            |
| Gate 2-source pinch-off voltage<br>$V_{\text{DS}} = 12\ \text{V}$ , $I_D = 100\ \mu\text{A}$                                      | $V_{\text{G2S(p)}}$              | -      | 0.9  | -    | V             |
| AC characteristics                                                                                                                |                                  |        |      |      |               |
| Forward transconductance (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6\ \text{V}$                                | $g_{\text{fs}}$                  | 26     | 30   | -    | mS            |
| Gate 1-input capacitance (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6$ , $f = 1\ \text{MHz}$                    | $C_{\text{g1ss}}$                | -      | 2.1  | 2.7  | pF            |
| Output capacitance (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6$ , $f = 1\ \text{MHz}$                          | $C_{\text{dss}}$                 | -      | 0.9  | -    |               |
| Power gain (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6$ , $f = 800\ \text{MHz}$                                | $G_{\text{ps}}$                  | 18     | 22   | -    | dB            |
| Noise figure (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{G2S} = 6$ , $f = 800\ \text{MHz}$                              | $F_{800}$                        | -      | 1.4  | -    | dB            |
| Gain control range (self biased)<br>$V_{\text{DS}} = 12\ \text{V}$ , $V_{\text{G2S}} = 6 \dots 0\text{V}$ , $f = 800\ \text{MHz}$ | $\Delta G_{\text{ps}}$           | 40     | 50   | -    |               |

**Total power dissipation  $P_{\text{tot}} = f(T_S)$**

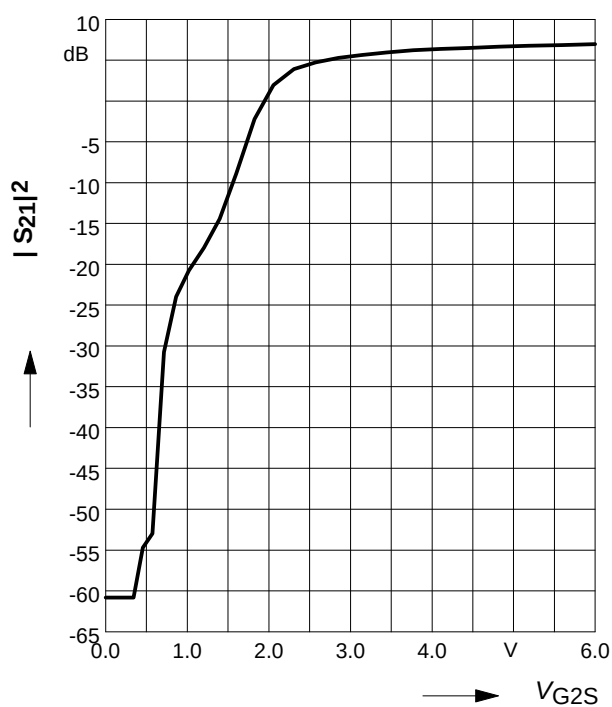


**Drain current  $I_D = f(V_{G2S})$**



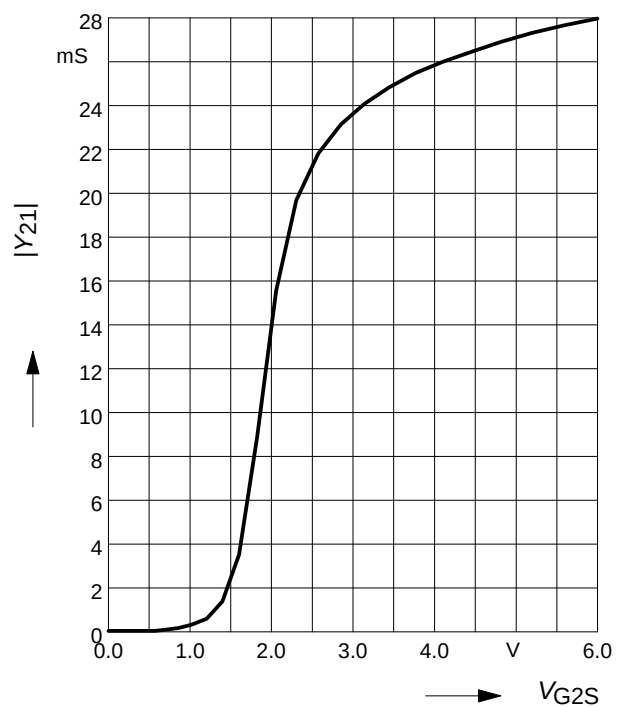
**Insertion power gain**

$|S_{21}|^2 = f(V_{G2S})$



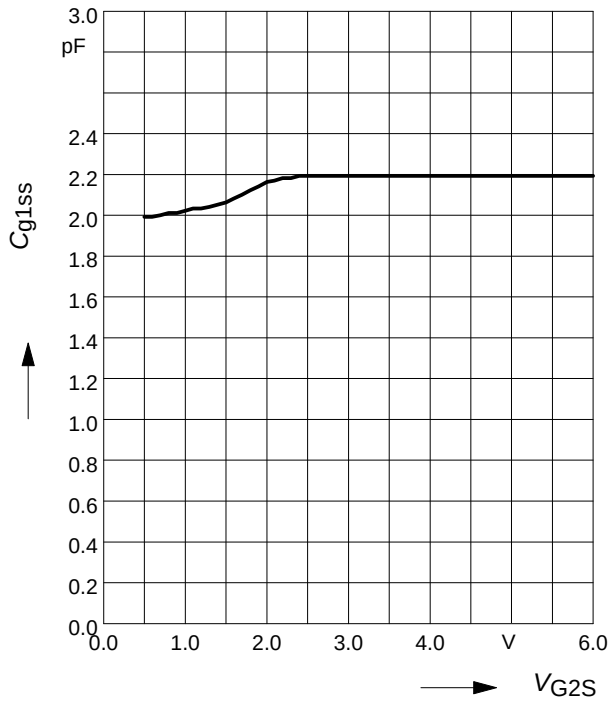
**Forward transfer admittance**

$|Y_{21}| = f(V_{G2S})$



**Gate 1 input capacitance  $C_{g1ss} = f(V_{G2S})$**

$f = 200\text{MHz}$



**Output capacitance  $C_{dss} = f(V_{G2S})$**

$f = 200\text{MHz}$

