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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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BB503C

Build in Biasing Circuit MOS FET IC UHF RF Amplifier



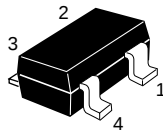
ADE-208-812C (Z)
4th. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise; NF = 1.8 dB typ. at $f = 900$ MHz
- High gain; PG = 22 dB typ. at $f = 900$ MHz
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at $C=200\text{pF}$, $R_s=0$ conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "CS-".
 2. BB503C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

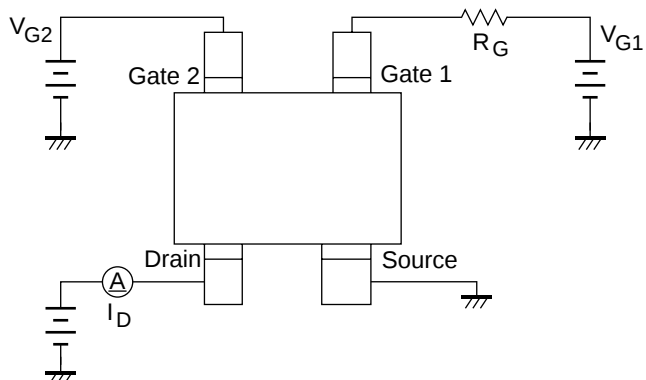
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	20	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Electrical Characteristics (Ta = 25°C)

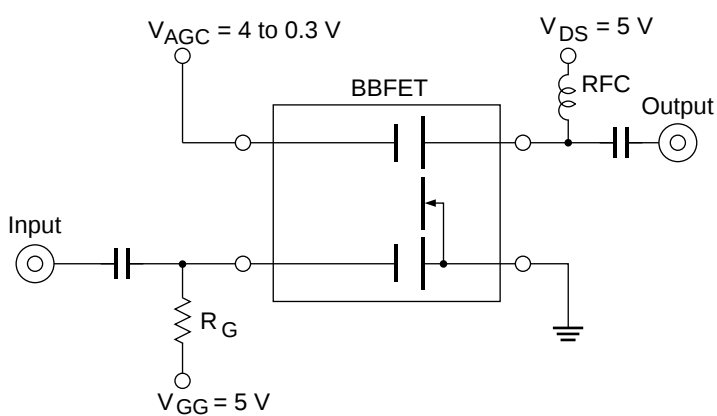
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$ $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$ $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\mu A$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5V, V_{G2S} = 4V$ $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5V, V_{G1S} = 5V$ $I_D = 100\mu A$
Drain current	$I_{D(op)}$	7	10	13	mA	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V, R_G = 47k\Omega$
Forward transfer admittance	$ y_{fs} $	19	24	29	mS	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V$ $R_G = 47k\Omega, f = 1kHz$
Input capacitance	C_{iss}	1.4	1.7	2.0	pF	$V_{DS} = 5V, V_{G1} = 5V$
Output capacitance	C_{oss}	0.7	1.1	1.5	pF	$V_{G2S} = 4V, R_G = 47k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.025	0.05	pF	$f = 1MHz$
Power gain	PG	17	22	—	dB	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V, R_G = 47k\Omega$
Noise figure	NF	—	1.8	2.4	dB	$f = 900MHz$

Main Characteristics

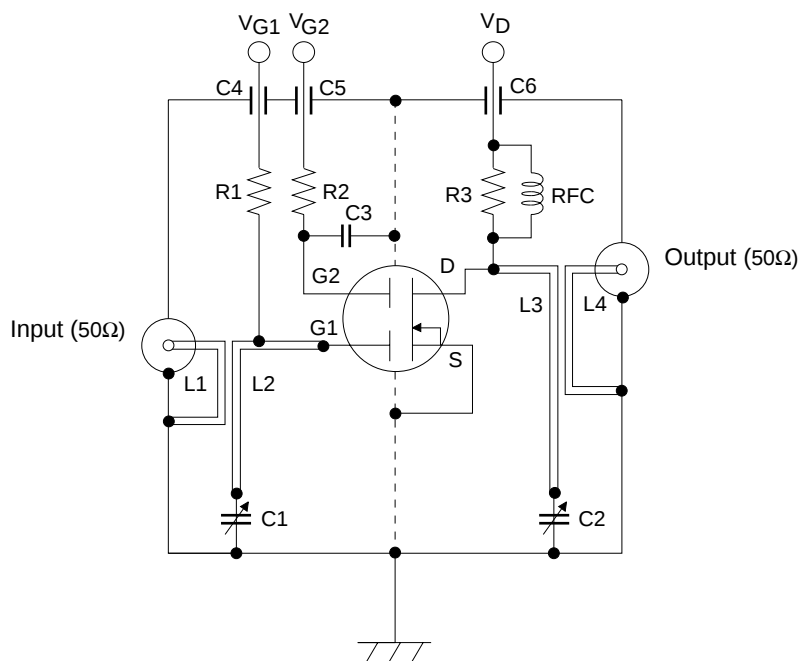
Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)



Application Circuit

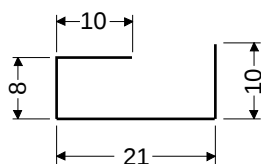


900MHz Power Gain, Noise Figure Test Circuit

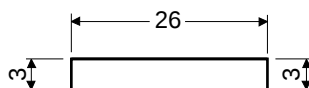


- C1, C2: Variable Capacitor (10pF MAX)
 C3: Disk Capacitor (1000pF)
 C4 to C6: Air Capacitor (1000pF)
 R1: 47 k Ω
 R2: 47 k Ω
 R3: 4.7 k Ω

L1:

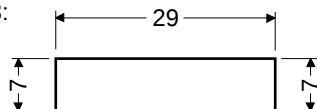


L2:

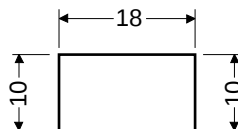


(ϕ 1mm Copper wire)
Unit: mm

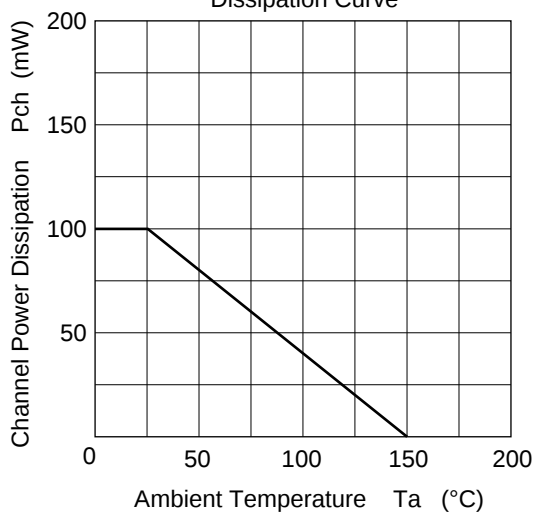
L3:



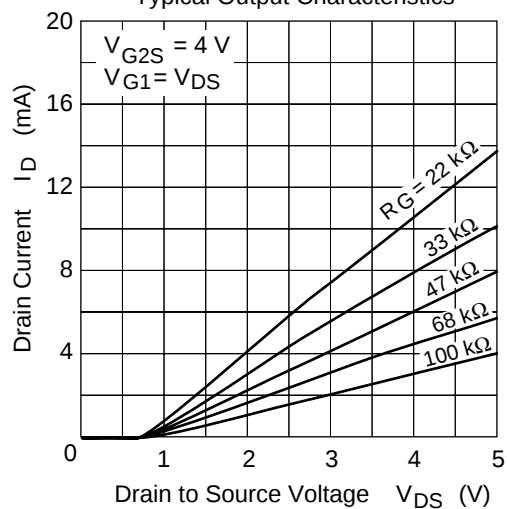
L4:



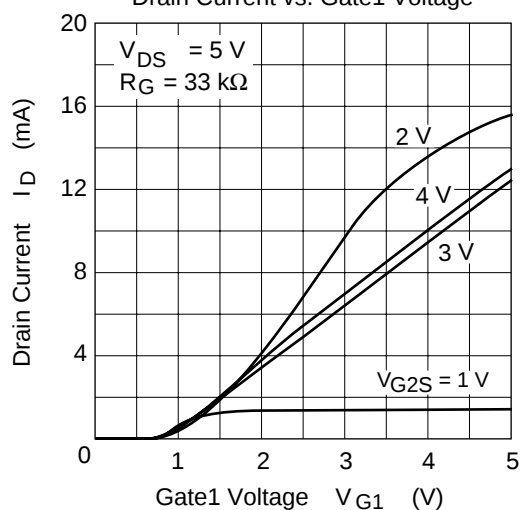
RFC: ϕ 1mm Copper wire with enamel 4 turns inside dia 6mm

Maximum Channel Power
Dissipation Curve

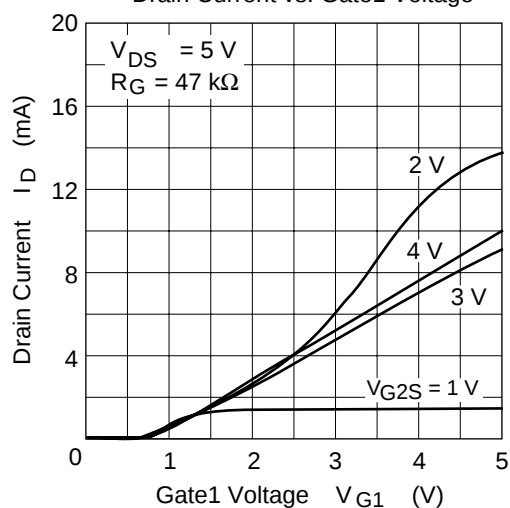
Typical Output Characteristics

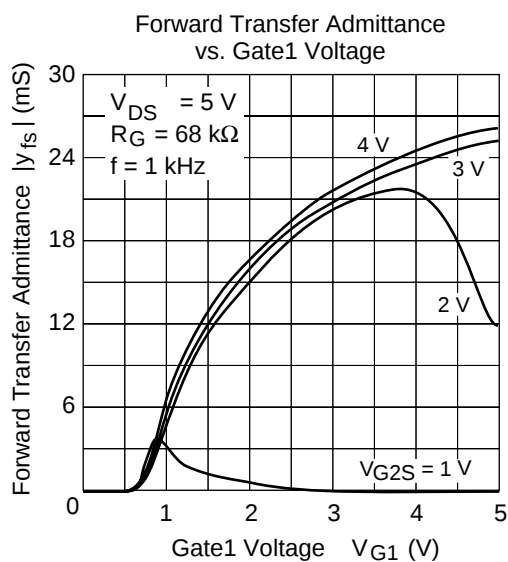
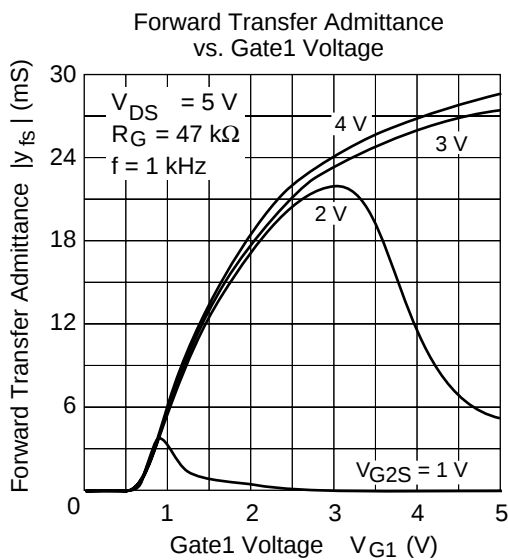
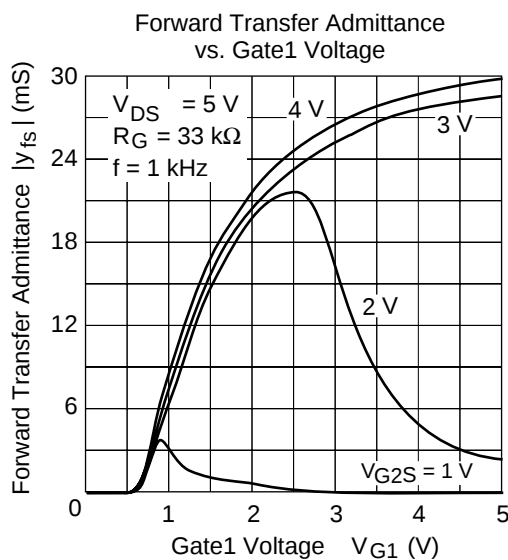
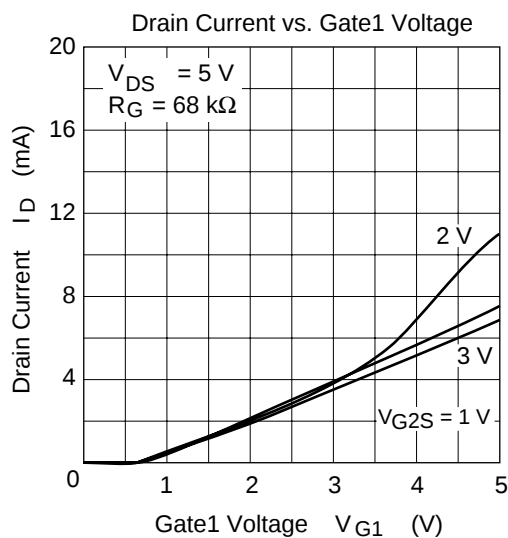


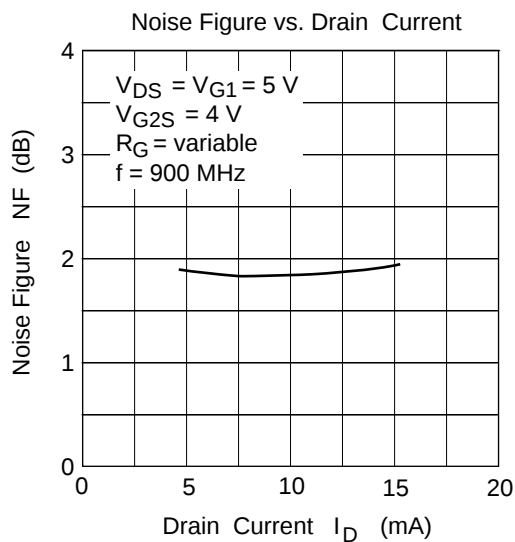
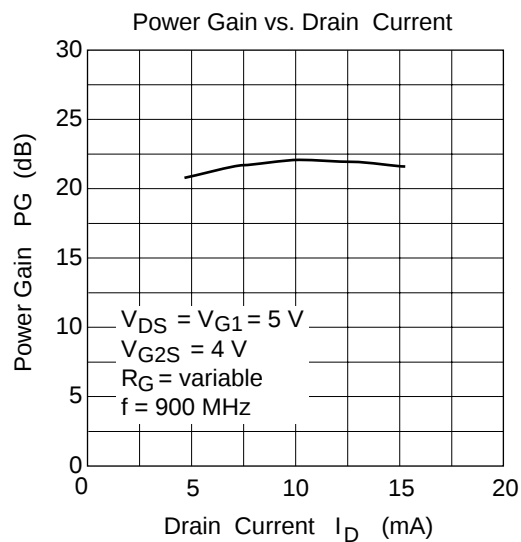
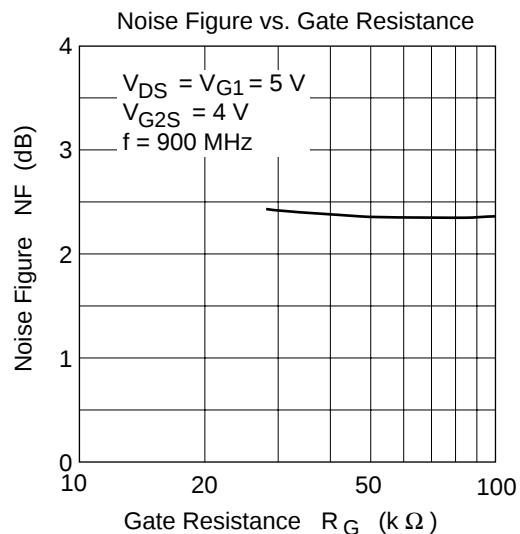
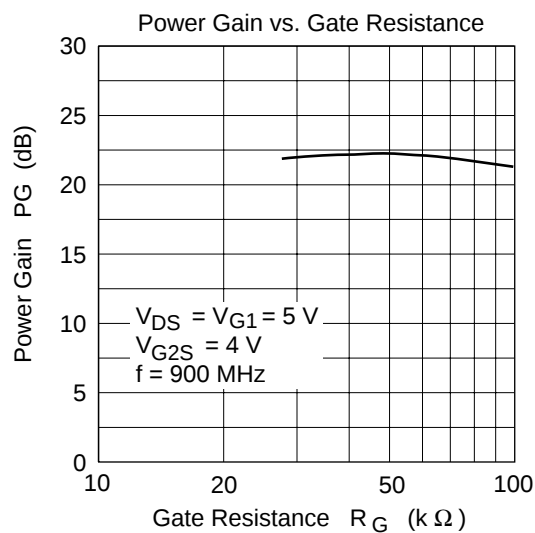
Drain Current vs. Gate1 Voltage

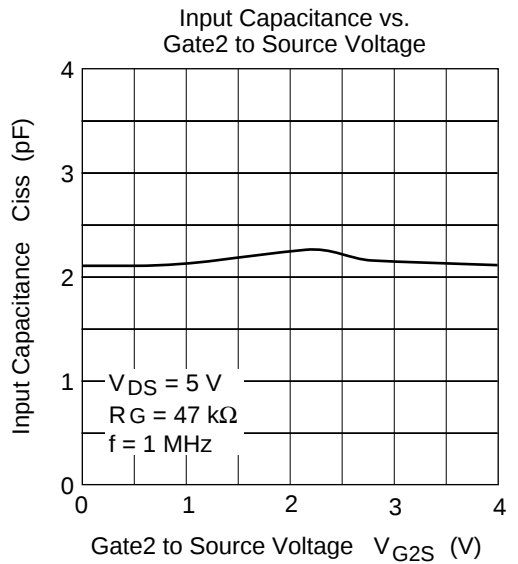
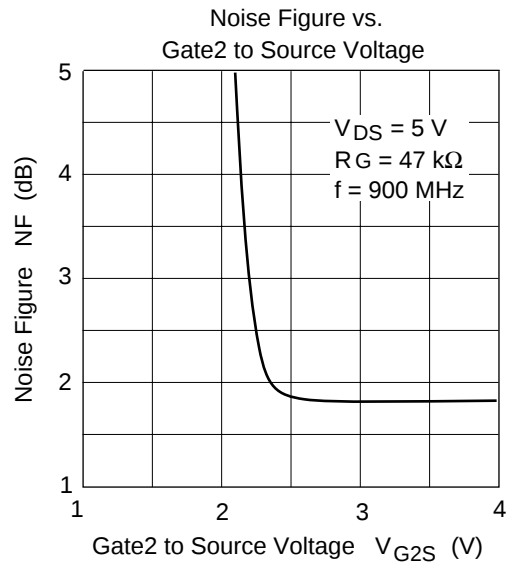
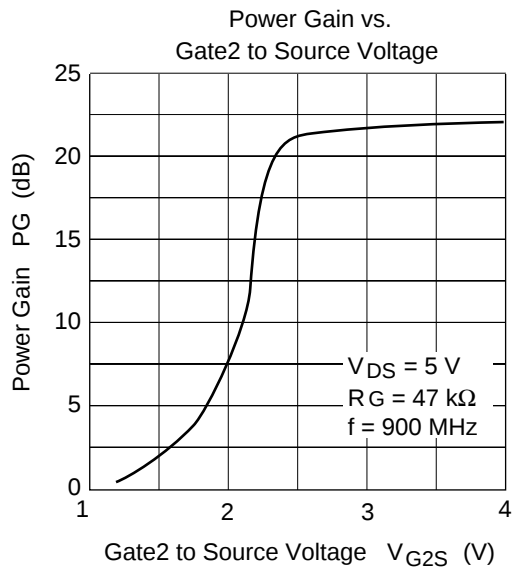
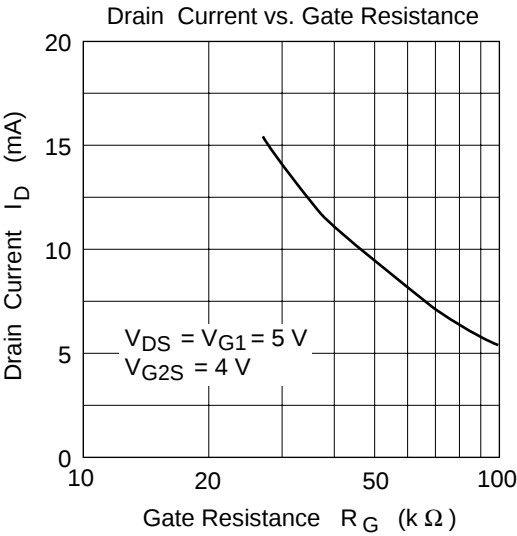


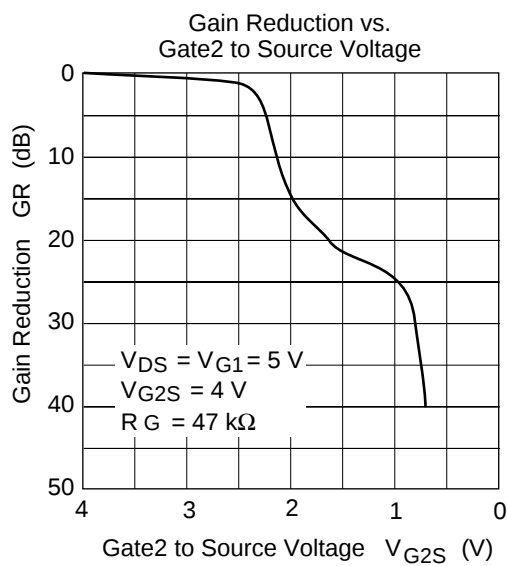
Drain Current vs. Gate1 Voltage



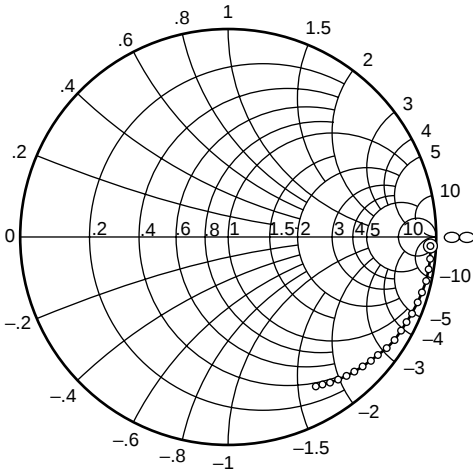








S11 Parameter vs. Frequency

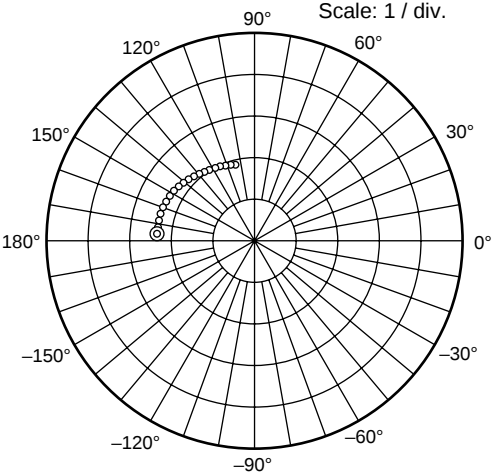


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 47\text{ k}\Omega$,
 $Z_0 = 50\text{ }\Omega$

50 to 1000 MHz (50 MHz step)



S21 Parameter vs. Frequency

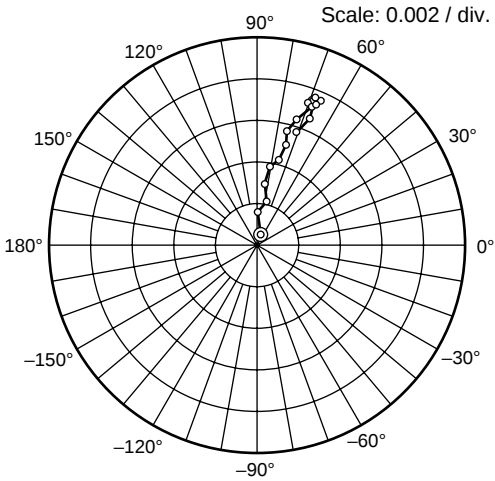


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 47\text{ k}\Omega$,
 $Z_0 = 50\text{ }\Omega$

50 to 1000 MHz (50 MHz step)



S12 Parameter vs. Frequency

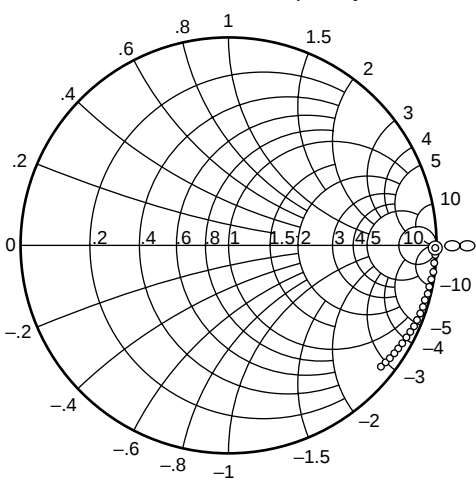


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 47\text{ k}\Omega$,
 $Z_0 = 50\text{ }\Omega$

50 to 1000 MHz (50 MHz step)



S22 Parameter vs. Frequency



Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 47\text{ k}\Omega$,
 $Z_0 = 50\text{ }\Omega$

50 to 1000 MHz (50 MHz step)

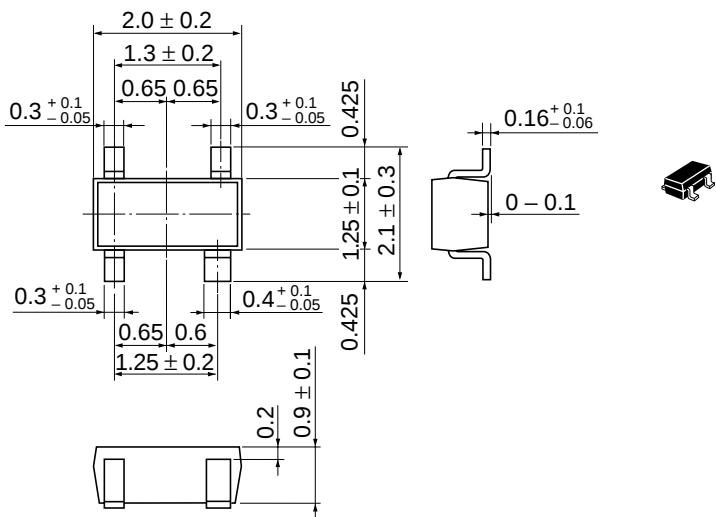


Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 47k\Omega$, $Z_0 = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.975	-2.6	2.37	176.1	0.00097	74.4	0.995	-1.9
100	0.977	-6.5	2.37	172.1	0.00162	89.8	0.998	-3.9
150	0.975	-9.1	2.36	168.0	0.00222	78.2	0.997	-5.8
200	0.972	-12.4	2.33	163.8	0.00282	83.8	0.996	-8.0
250	0.968	-15.6	2.32	159.9	0.00388	81.1	0.994	-10.0
300	0.963	-18.9	2.30	156.0	0.00437	76.0	0.993	-11.8
350	0.954	-22.2	2.28	151.8	0.00518	73.6	0.991	-13.9
400	0.946	-25.3	2.25	148.2	0.00567	75.6	0.989	-15.8
450	0.937	-28.2	2.22	144.1	0.00631	72.5	0.986	-17.8
500	0.930	-31.5	2.19	140.2	0.00637	72.7	0.984	-19.6
550	0.920	-34.7	2.16	136.3	0.00720	70.3	0.981	-21.6
600	0.914	-37.4	2.13	132.7	0.00747	67.0	0.978	-23.4
650	0.902	-40.4	2.09	129.3	0.00738	69.2	0.975	-25.4
700	0.886	-43.5	2.07	125.4	0.00758	68.6	0.972	-27.3
750	0.879	-46.1	2.03	122.0	0.00757	66.0	0.968	-29.0
800	0.873	-48.9	1.99	118.3	0.00729	67.5	0.966	-31.0
850	0.857	-52.0	1.96	114.9	0.00723	68.8	0.962	-32.9
900	0.845	-54.5	1.93	111.4	0.00706	68.3	0.959	-34.8
950	0.838	-57.2	1.90	108.1	0.00659	67.5	0.954	-36.6
1000	0.824	-59.6	1.86	104.9	0.00574	71.0	0.952	-38.5

Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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