

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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BB305C

Build in Biasing Circuit MOS FET IC UHF/VHF RF Amplifier

RENESAS

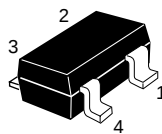
ADE-208-608D (Z)
5th. Edition
Mar 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Superior cross modulation characteristics.
- High gain; (PG = 28 dB typ. at $f = 200$ MHz)
- Wide supply voltage range;
Applicable with 5 V to 9 V supply voltage.
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at $C = 200$ pF, $R_s = 0$ conditions.
- Provide mini mold packages; CMPAK-4 (SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "EW –".
 2. BB305C is individual type number of HITACHI BBFET.

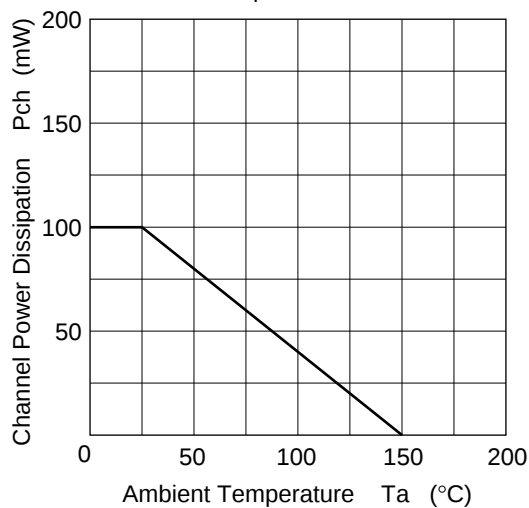
Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	12	V
Gate1 to source voltage	V_{G1S}	+10 −0	V
Gate2 to source voltage	V_{G2S}	+10	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

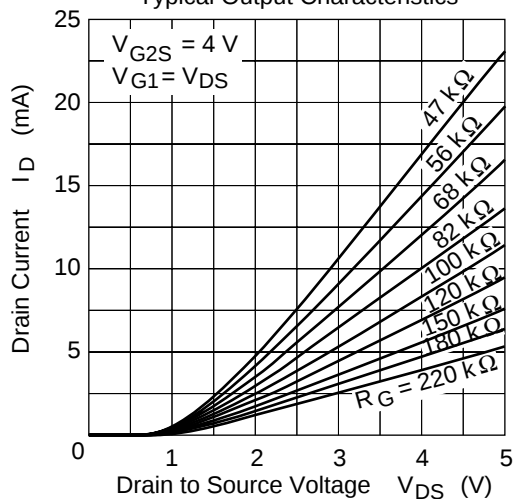
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	12	—	—	V	$I_D = 200\mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+10	—	—	V	$I_{G1} = +10\mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±10	—	—	V	$I_{G2} = \pm 10\mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +9V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	±100	nA	$V_{G2S} = \pm 9V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	$V_{DS} = 5V$, $V_{G2S} = 4V$, $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	$V_{DS} = 5V$, $V_{G1S} = 5V$, $I_D = 100\mu A$
Input capacitance	C_{iss}	2.3	2.8	3.5	pF	$V_{DS} = 5V$, $V_{G1} = 5V$
Output capacitance	C_{oss}	1.1	1.5	1.9	pF	$V_{G2S} = 4V$, $R_G = 82k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.017	0.04	pF	$f = 1MHz$
Drain current	$I_{D(op)1}$	10	15	20	mA	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$
	$I_{D(op)2}$	—	13	—	mA	$V_{DS} = 9V$, $V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 220k\Omega$
Forward transfer admittance	$ y_{fs} 1$	23	28	—	mS	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $f = 1kHz$
	$ y_{fs} 2$	—	28	—	mS	$V_{DS} = 9V$, $V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 220k\Omega$, $f = 1kHz$
Power gain	PG1	24	28	—	dB	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $f = 200MHz$
	PG2	—	28	—	dB	$V_{DS} = 9V$, $V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 220k\Omega$, $f = 200MHz$
Noise figure	NF1	—	1.3	1.8	dB	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $f = 200MHz$
	NF2	—	1.3	—	dB	$V_{DS} = 9V$, $V_{G1} = 9V$, $V_{G2S} = 6V$, $R_G = 220k\Omega$, $f = 200MHz$

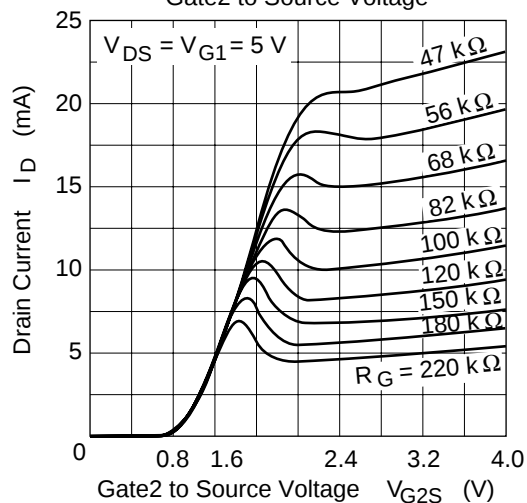
Maximum Channel Power
Dissipation Curve



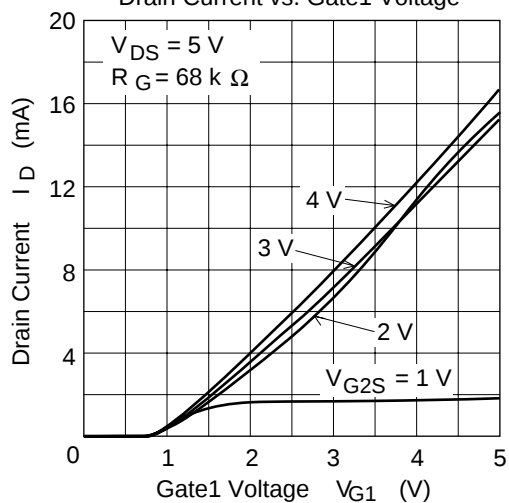
Typical Output Characteristics

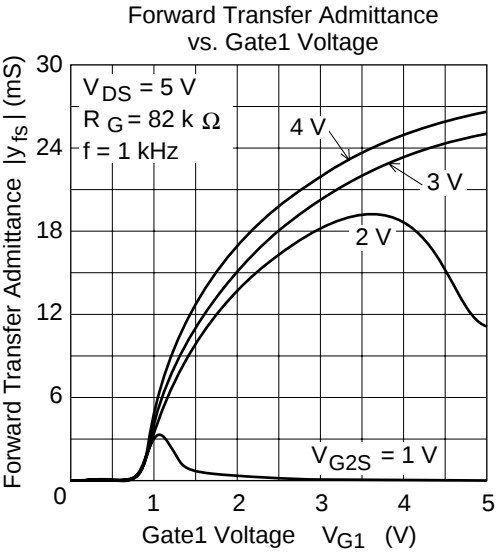
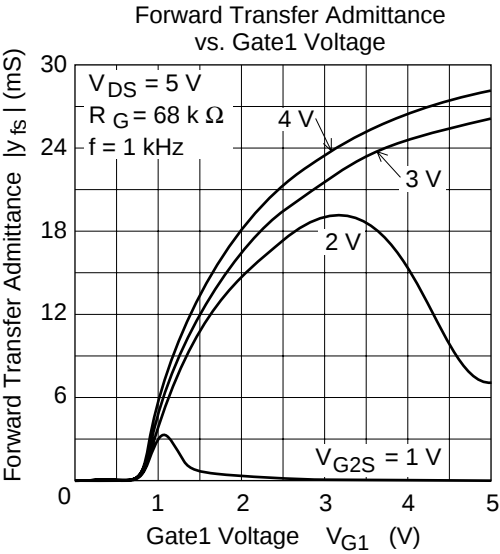
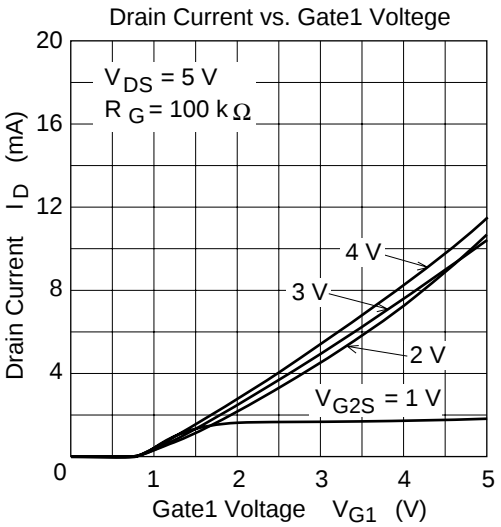
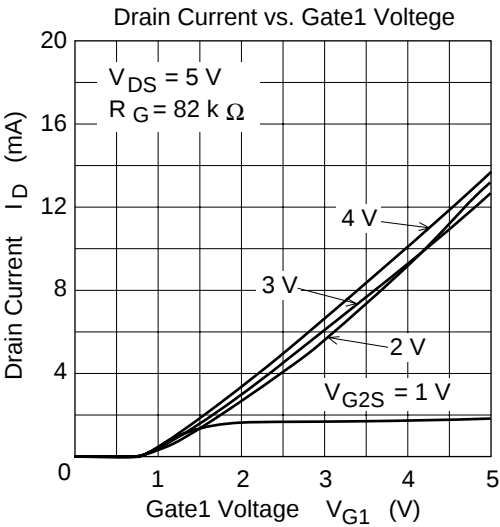


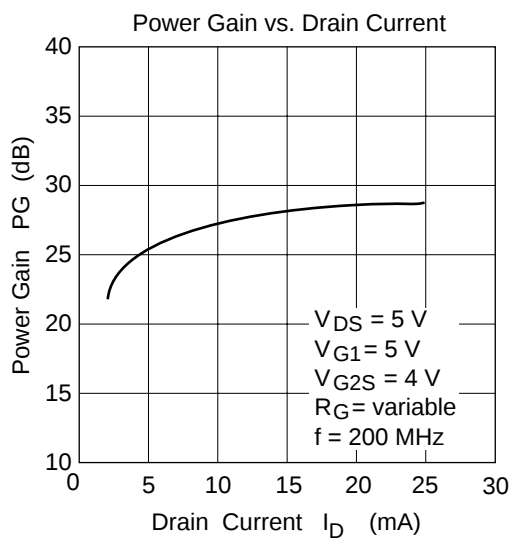
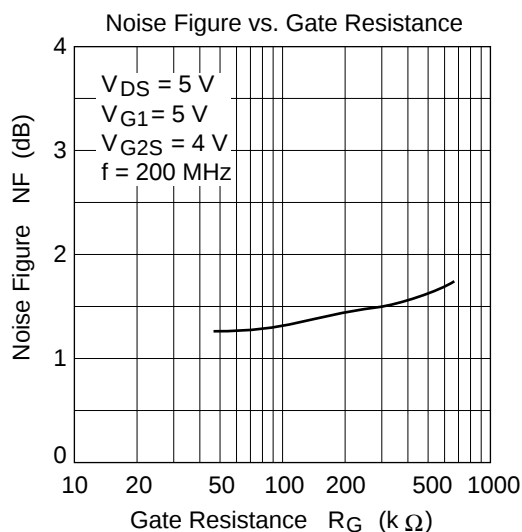
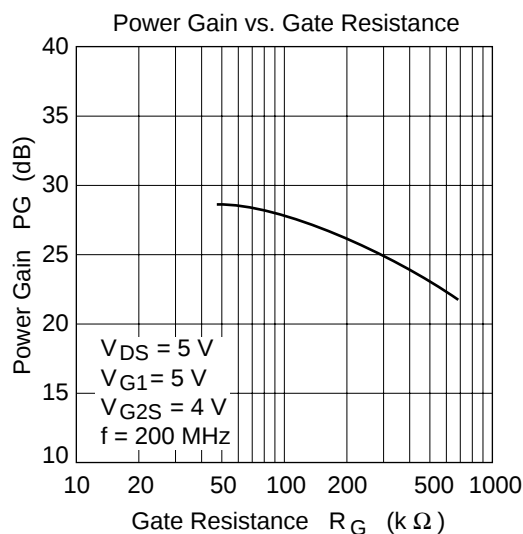
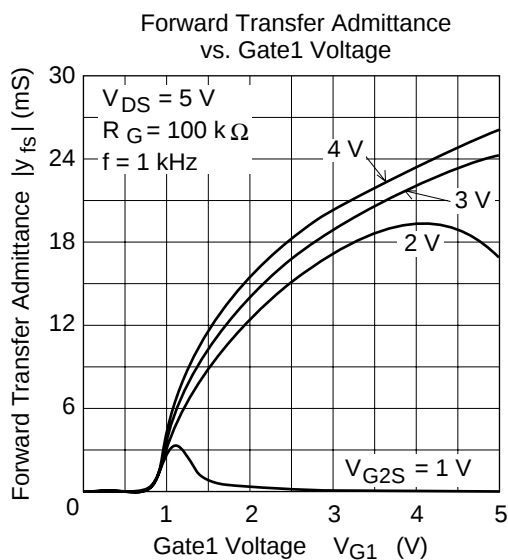
Drain Current vs.
Gate2 to Source Voltage

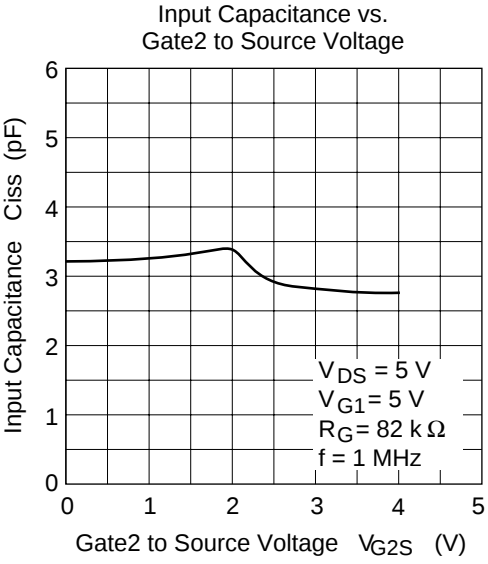
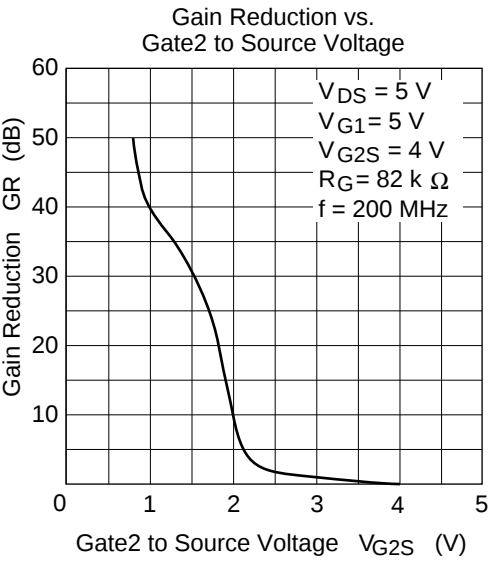
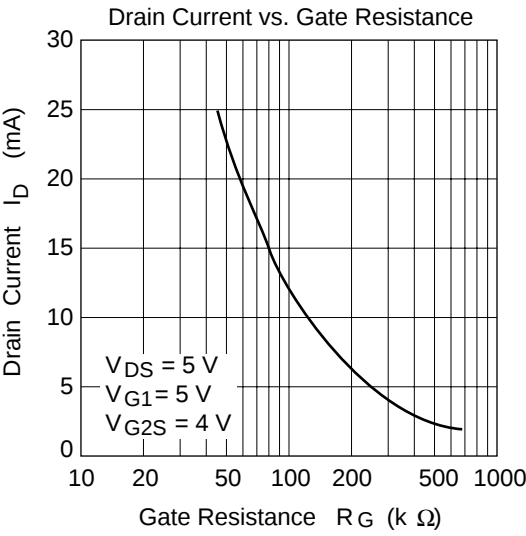
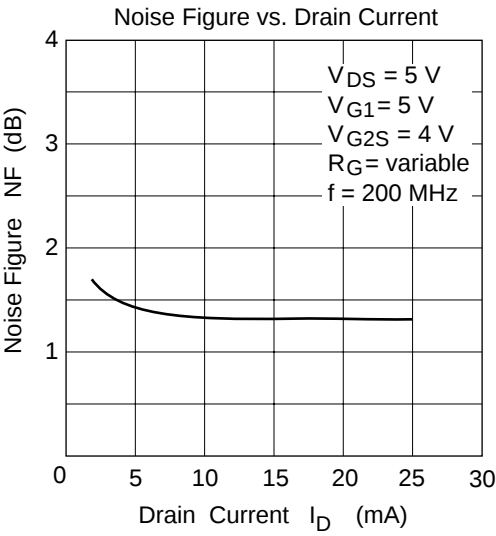


Drain Current vs. Gate1 Voltage

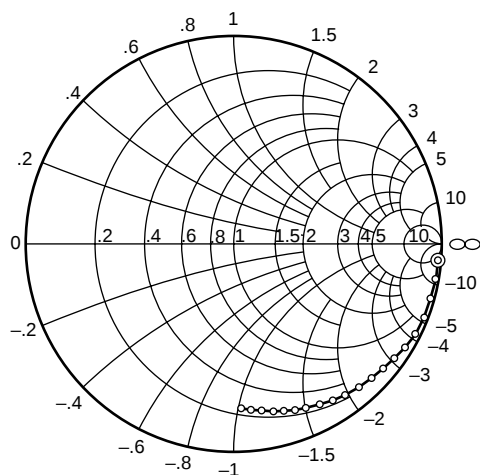








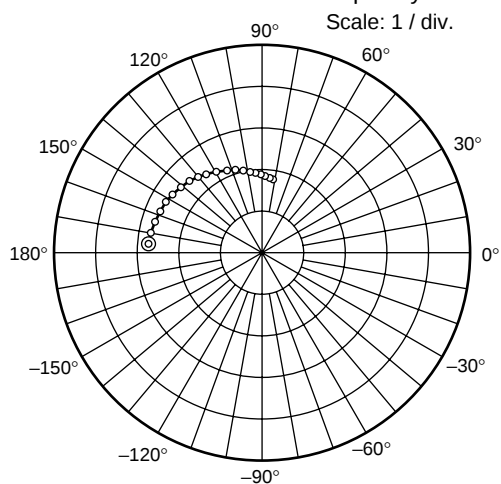
S11 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 — 1000 MHz (50 MHz step)

○ — ○

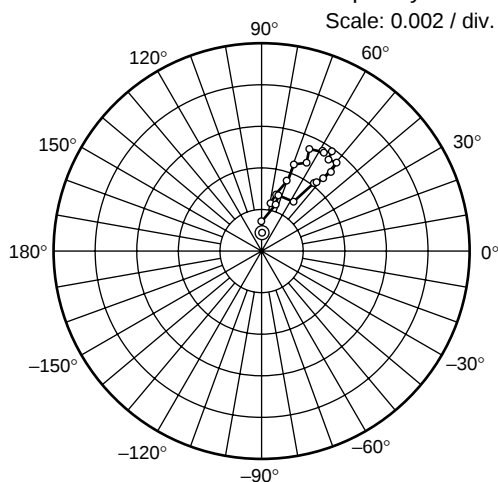
S21 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 — 1000 MHz (50 MHz step)

○ — ○

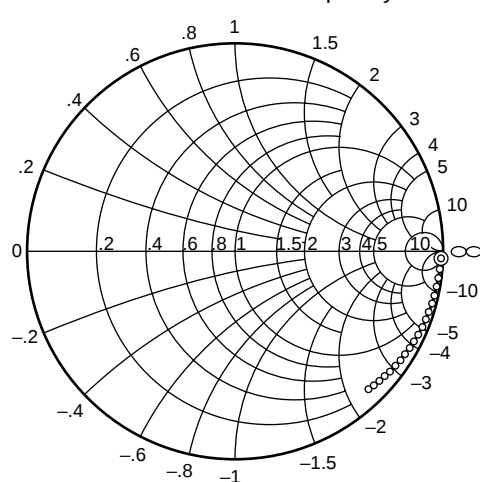
S12 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 — 1000 MHz (50 MHz step)

○ — ○

S22 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 50 — 1000 MHz (50 MHz step)

○ — ○

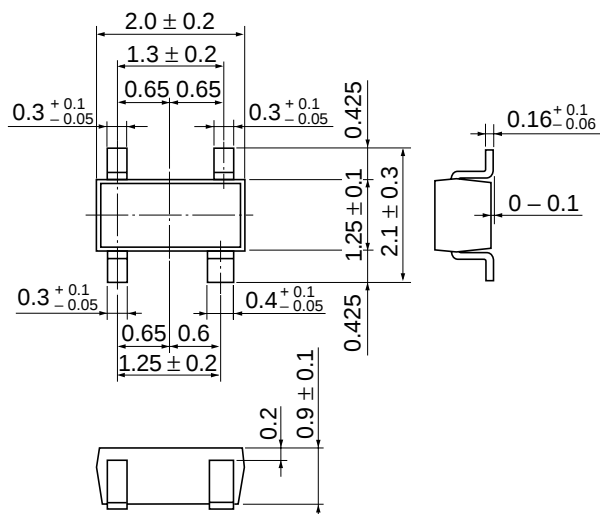
Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $Z_o = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.991	-4.8	2.69	174.9	0.00090	91.4	0.991	-2.2
100	0.991	-9.9	2.68	169.3	0.00153	90.5	0.992	-4.8
150	0.982	-15.4	2.66	163.4	0.00243	73.8	0.991	-7.5
200	0.975	-20.7	2.62	157.5	0.00293	74.9	0.989	-9.9
250	0.972	-25.6	2.60	152.0	0.00370	70.1	0.985	-12.6
300	0.956	-30.6	2.54	146.3	0.00444	69.0	0.981	-15.0
350	0.942	-35.5	2.47	140.9	0.00478	63.7	0.977	-17.3
400	0.928	-40.1	2.42	135.7	0.00535	64.8	0.973	-19.7
450	0.920	-44.9	2.38	130.5	0.00551	56.8	0.967	-22.0
500	0.906	-49.2	2.32	125.7	0.00549	58.6	0.962	-24.5
550	0.894	-53.6	2.25	120.8	0.00584	54.4	0.957	-26.9
600	0.880	-57.8	2.18	116.2	0.00542	53.3	0.952	-29.2
650	0.868	-62.1	2.12	111.5	0.00562	49.5	0.944	-31.5
700	0.854	-66.2	2.06	106.8	0.00509	48.6	0.939	-33.8
750	0.842	-70.3	2.00	102.5	0.00465	49.7	0.933	-36.1
800	0.835	-73.9	1.94	98.4	0.00427	51.6	0.927	-38.3
850	0.820	-77.7	1.89	94.0	0.00416	53.3	0.921	-40.5
900	0.802	-81.5	1.83	89.6	0.00289	57.9	0.915	-42.7
950	0.801	-84.7	1.78	85.6	0.00288	72.9	0.909	-44.9
1000	0.789	-87.9	1.73	82.1	0.00241	78.9	0.904	-47.1

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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