

BUK7L06-34ARC

TrenchPLUS standard level FET

Rev. 02 — 21 May 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, integral gate resistor, ESD protection diodes and clamping diodes that are guaranteed to prevent the MOSFET avalanching.

Product availability:

BUK7L06-34ARC in SOT78C (TO-220).

1.2 Features

- ESD and overvoltage protection
- Internal gate resistor
- Q101 compliant
- On-state resistance 5.1 mΩ (typ).

1.3 Applications

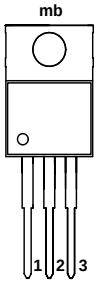
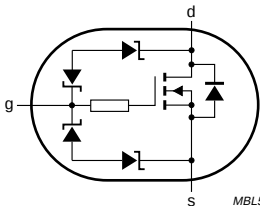
- 12 V loads
- Motors, lamps and solenoids.

1.4 Quick reference data

- $V_{DSR(CL)} = 41 \text{ V (typ)}$
- $I_D \leq 147 \text{ A}$
- $R_{DS(on)} = 5.1 \text{ m}\Omega \text{ (typ)}$
- $P_{tot} \leq 250 \text{ W}$.

2. Pinning information

Table 1: Pinning - SOT78C, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base, connected to drain (d)		

SOT78C (TO-220)

3. Limiting values

Table 2: Limiting values

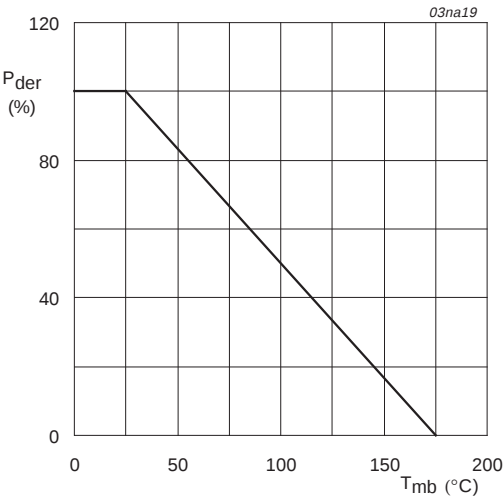
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		[1] -	34	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	[1] -	34	V
V_{GS}	gate-source voltage (DC)		[1] -	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	[2] -	147	A
			[3] -	75	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2	[2] -	103	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	590	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Figure 1	-	250	W
$I_{DG(CL)}$	drain-gate clamping current	$t_p = 5\text{ ms}$; $\delta = 0.01$	-	50	mA
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		$t_p = 5\text{ ms}$; $\delta = 0.01$	-	50	mA
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	[2] -	147	A
			[3] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	590	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A}$; $V_{DS} \leq 34\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$; starting $T_j = 25\text{ }^\circ\text{C}$	-	1.0	J
Electrostatic discharge					
V_{esd}	electrostatic discharge voltage; all pins	human body model; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$	-	8	kV
		human body model; $C = 250\text{ pF}$; $R = 1.5\text{ k}\Omega$	-	8	kV

[1] Voltage is limited by clamping.

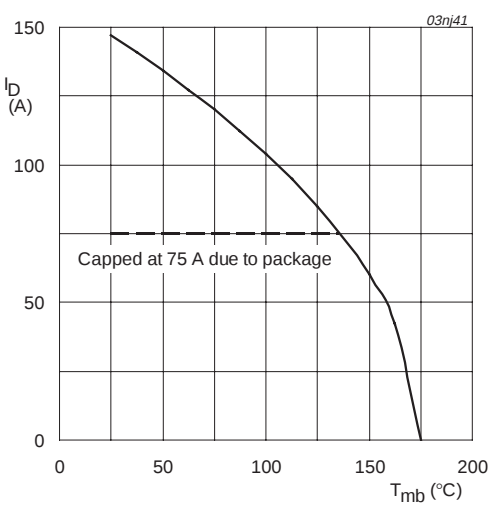
[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.



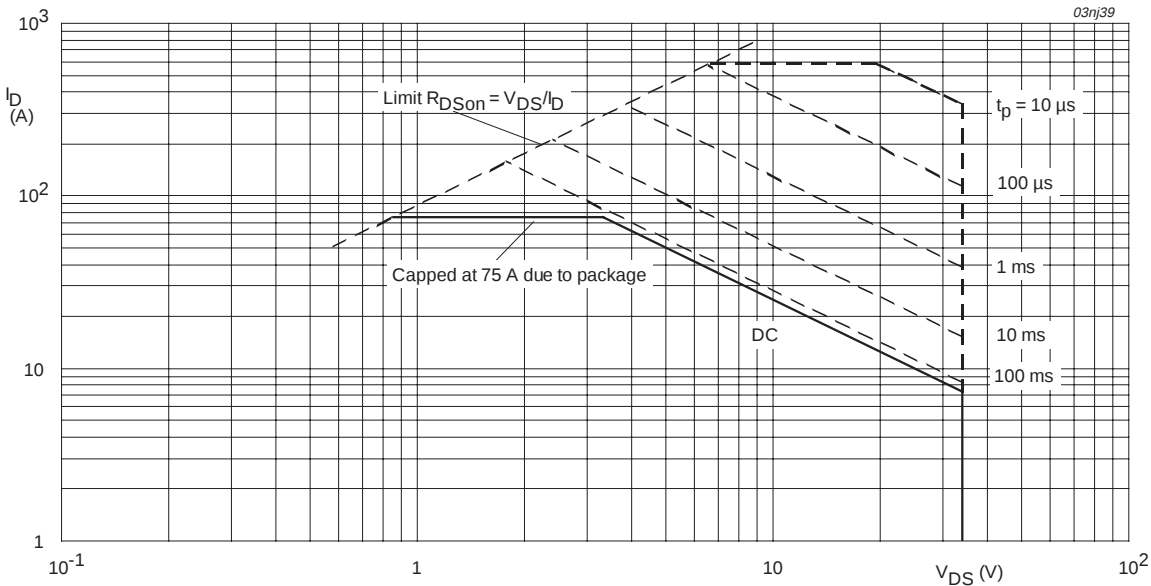
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	0.33	0.60	K/W

4.1 Transient thermal impedance

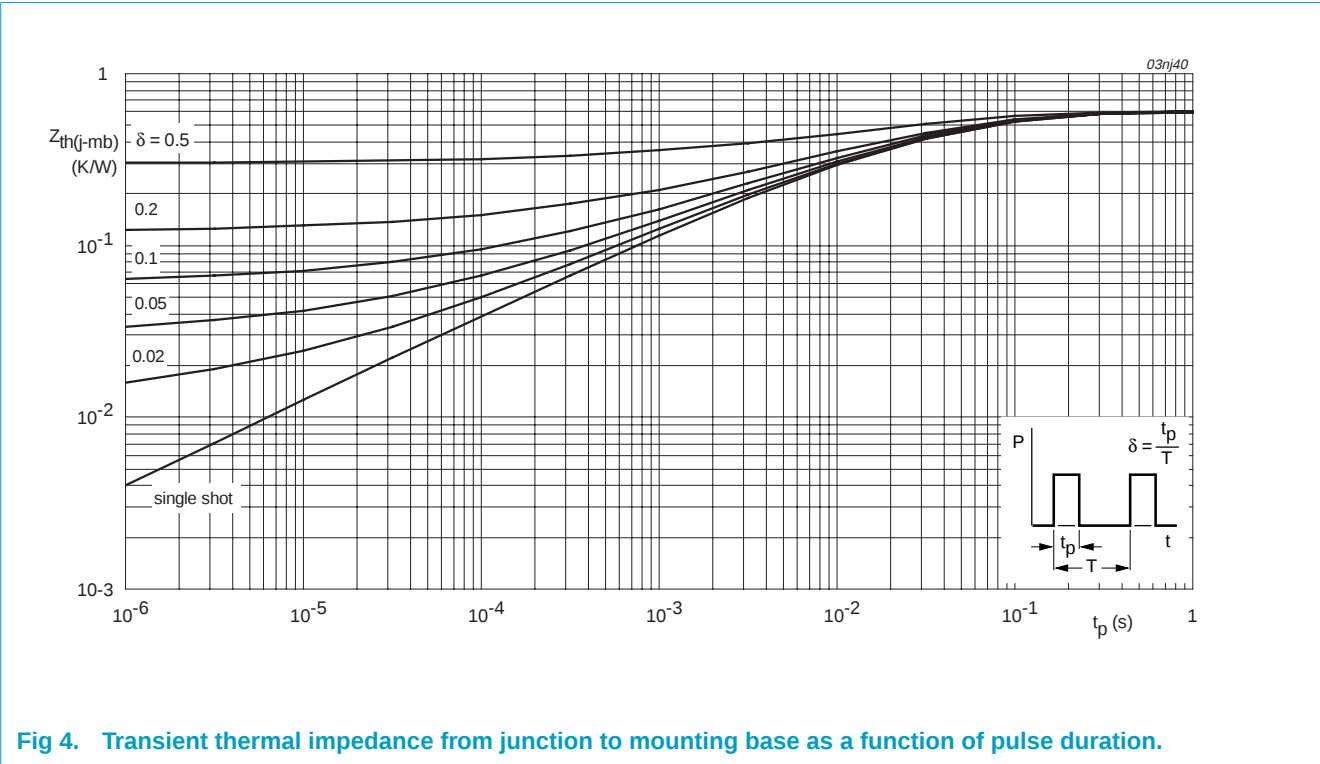


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

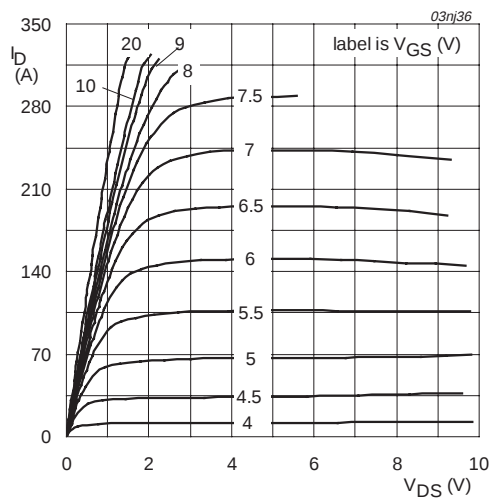
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DG}$	drain-gate zener breakdown voltage	$I_D = 2\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	34	-	45	V
		$T_j = -55\text{ °C}$	34	-	45	V
$V_{DSR(CL)}$	drain-source clamping voltage (DC)	$I_{GS(CL)} = -2\text{ mA}; I_D = 1\text{ A}$ [1] Figure 16 and 17	-	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	2.2	3	3.8	V
		$T_j = 175\text{ °C}$	1.2	-	-	V
		$T_j = 150\text{ °C}$	1.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 16\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.1	2	μA
		$T_j = 150\text{ °C}$	-	5	50	μA
		$T_j = 175\text{ °C}$	-	30	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $-55\text{ °C} < T_j < +175\text{ °C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	5	1000	nA
		$T_j = 175\text{ °C}$	-	-	50	μA
		$V_{GS} = 16\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 175\text{ °C}$	-	-	150	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 30\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	5.1	6.0	m Ω
		$T_j = 175\text{ °C}$	-	-	11.4	m Ω
		$V_{GS} = 16\text{ V}; I_D = 30\text{ A}$		4.0	5.3	m Ω
R_G	Internal gate resistor		-	11	-	Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DS} = 27\text{ V};$ $I_D = 25\text{ A};$ Figure 14	-	82	-	nC
Q_{gs}	gate-source charge		-	15	-	nC
Q_{gd}	gate-drain (Miller) charge		-	31	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ Figure 12	-	3400	4533	pF
C_{oss}	output capacitance		-	1080	1296	pF
C_{rss}	reverse transfer capacitance		-	660	904	pF

Table 4: Characteristics...continued $T_j = 25^\circ\text{C}$ unless otherwise specified.

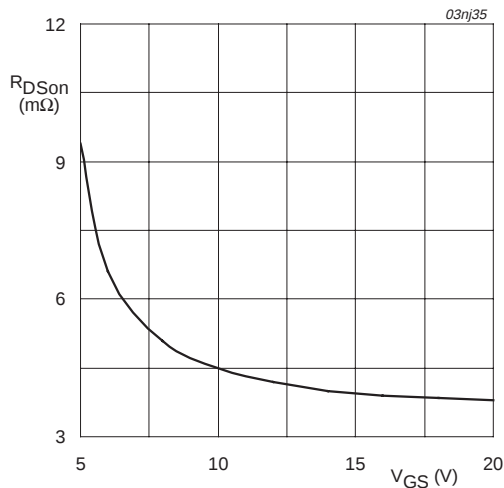
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\ \Omega;$ $V_{GS} = 10\text{ V}; R_G = 10\ \Omega$	-	27	-	nS
t_r	rise time		-	108	-	nS
$t_{d(off)}$	turn-off delay time		-	196	-	nS
t_f	fall time		-	167	-	nS
L_d	internal drain inductance	measured from drain lead 6 mm from package to center of die	-	4.5	-	nH
		measured from contact screw on mounting base to center of die SOT78C	-	3.5	-	nH
L_s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V};$ Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}$	-	62	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}; V_{DS} = 30\text{ V}$	-	44	-	nC

[1] Independent testing of MOSFET and clamping diodes guarantees against avalanche.



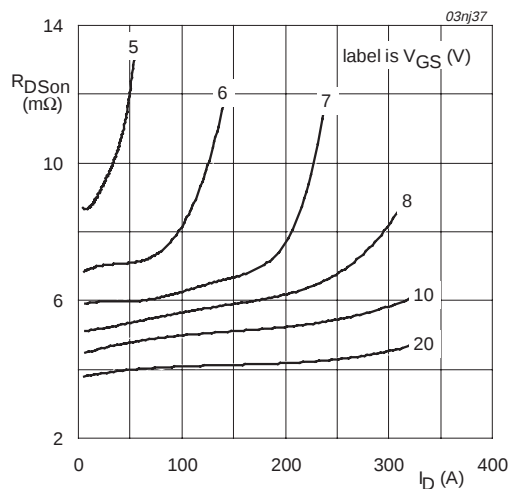
$T_J = 25\text{ }^{\circ}\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



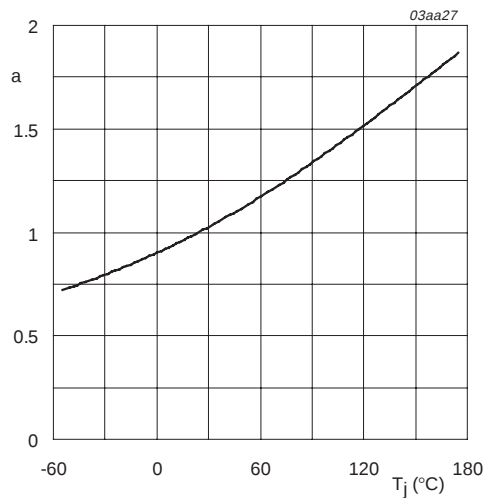
$T_J = 25\text{ }^{\circ}\text{C}$; $I_D = 30\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



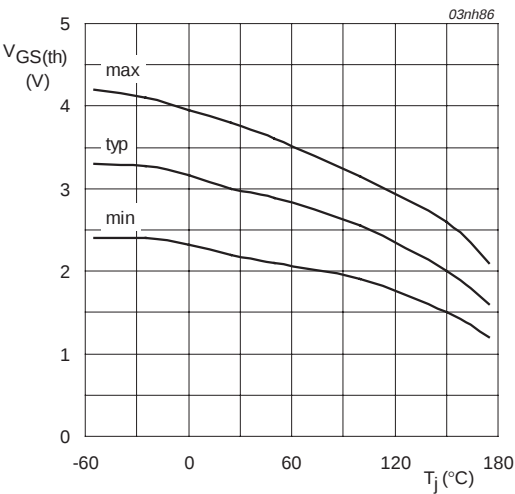
$T_J = 25\text{ }^{\circ}\text{C}$; $t_p = 300\mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



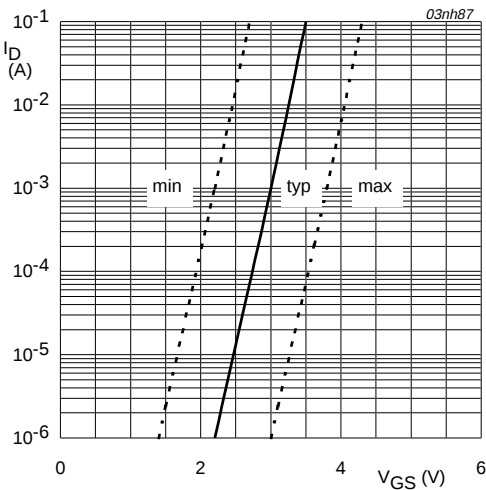
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



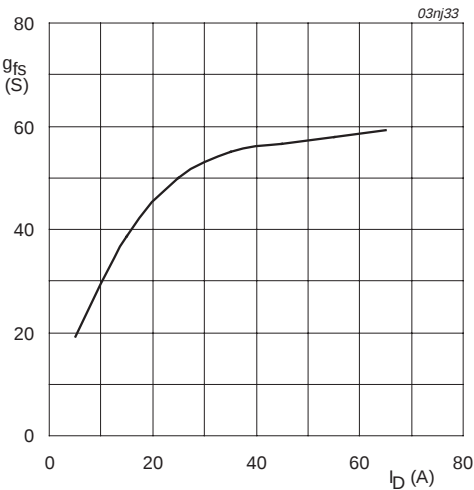
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



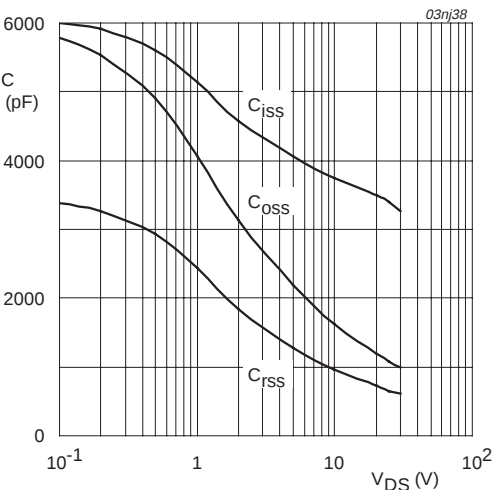
$T_j = 25 \text{ °C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



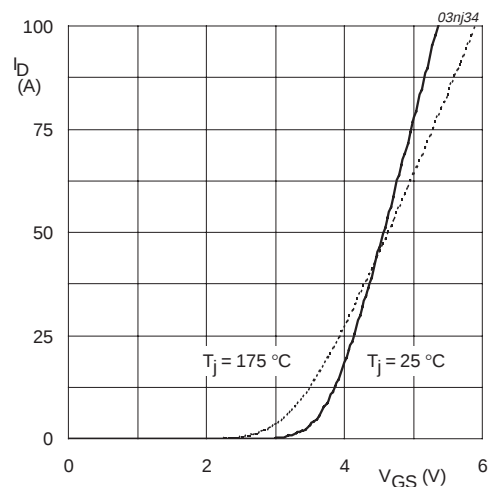
$T_j = 25 \text{ °C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



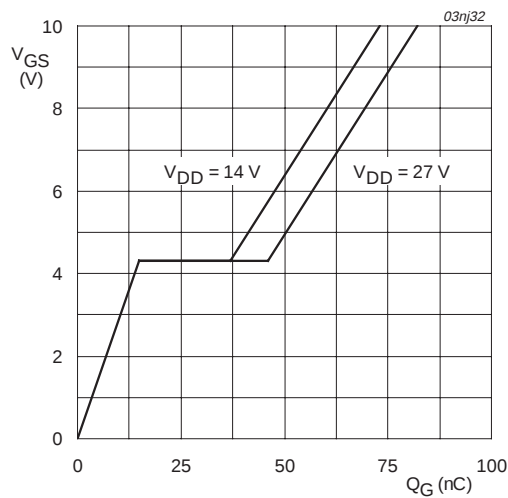
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



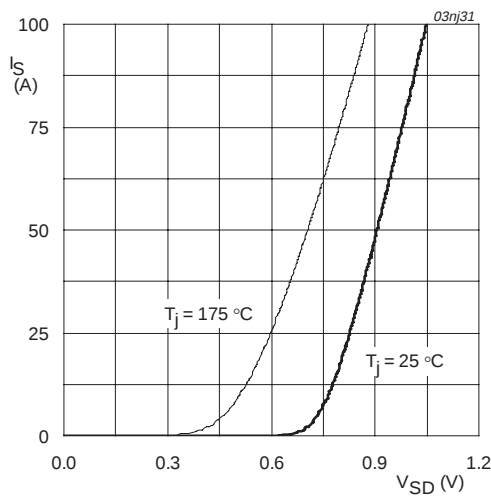
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



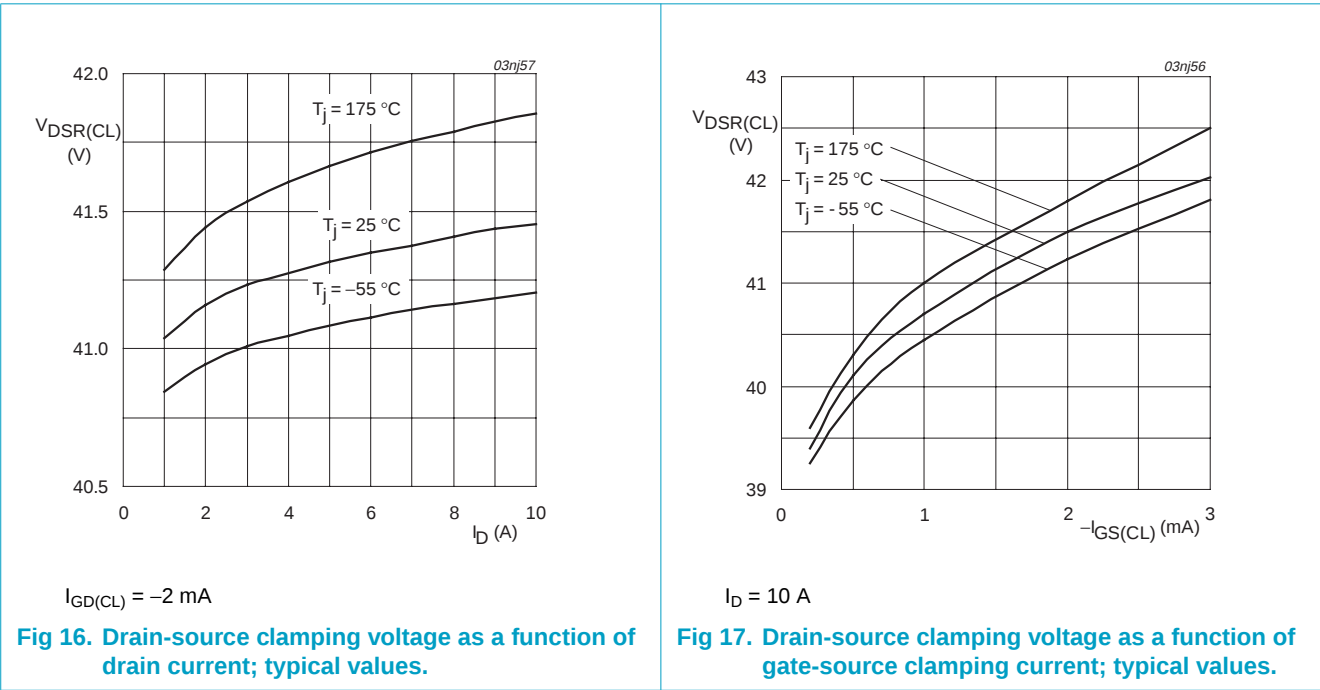
$T_J = 25\text{ °C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads

SOT78C

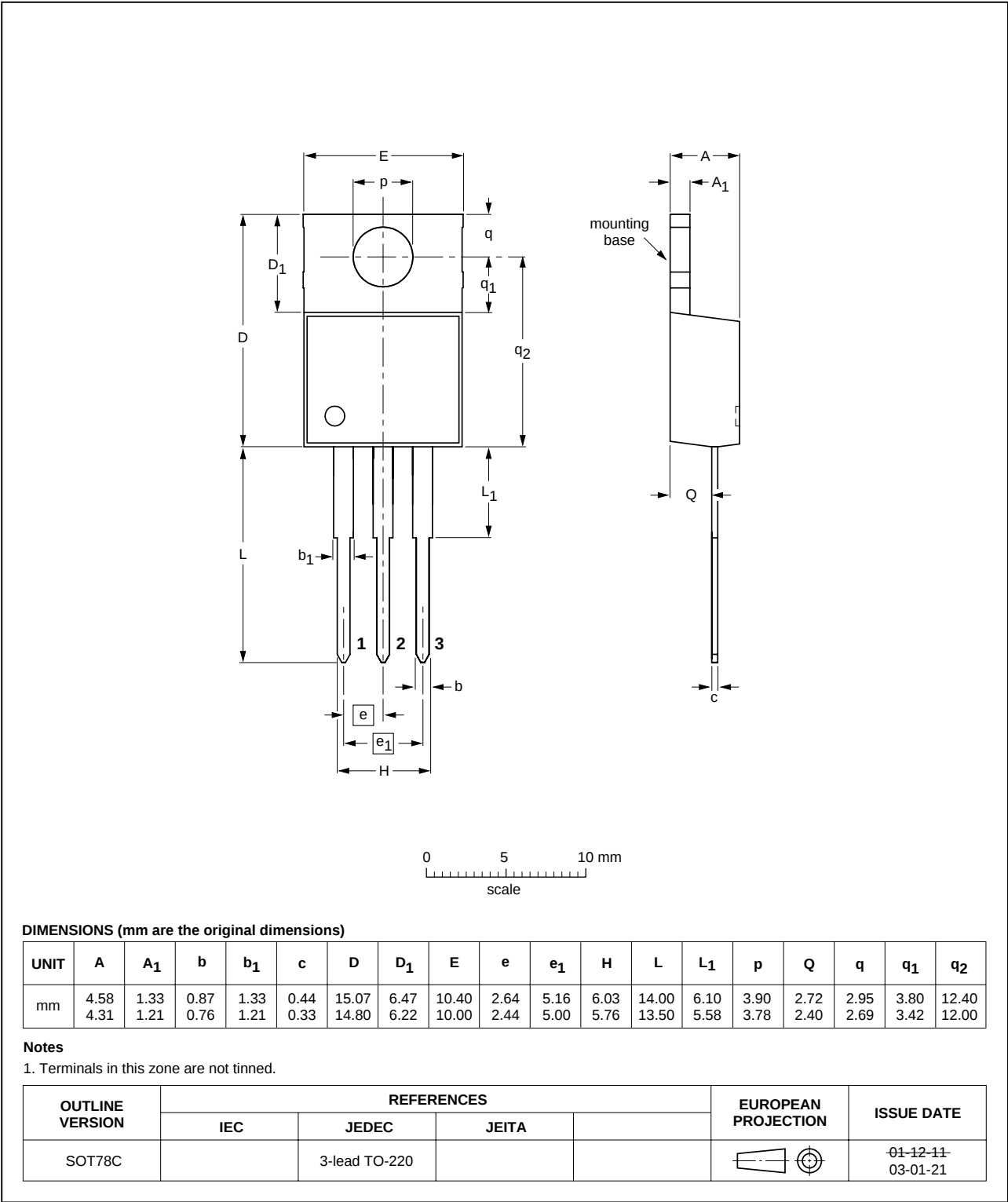


Fig 18. SOT78C (TO-220).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20030521	-	Product data (9397 750 11471) • Typical values of I_{DSS} added to characteristics table, Section 5.
01	20030414	-	Product data (9397 750 11177)

8. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

9. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

11. Trademarks

— TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

10. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1 **Product profile** 1

1.1 Description 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data. 1

2 **Pinning information** 1

3 **Limiting values** 2

4 **Thermal characteristics** 4

4.1 Transient thermal impedance 4

5 **Characteristics** 5

6 **Package outline** 11

7 **Revision history** 12

8 **Data sheet status** 13

9 **Definitions** 13

10 **Disclaimers** 13

11 **Trademarks** 13



PHILIPS

Let's make things better.