36.0-43.0 GHz GaAs MMIC Buffer Amplifier

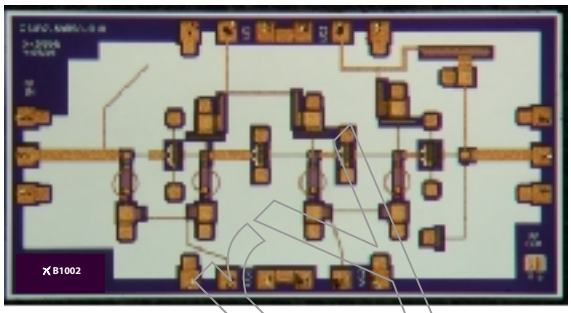
July 2001 - Rev 7/27/01

B1002

Features

- 36.0-43.0 GHz Frequency Range
- 25.0 dB Typical Small Signal Gain
- 4.0 dB Typical Noise Figure
- +14 dBm Typical Compression Point
- Operates at +3.0 to +5.5 VDC
- 2.90 mm X 1.50 mm Die Size
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

Chip Device Layout



General Description

Mimix Broadband's four stage 36.0-43.0 GHz GaAs MMIC gain block amplifier has a typical small signal gain of 25.0 dB with a typical noise figure of 4.0 dB across the band. Gain increases with frequency to compensate for other component roll-off factors common in 38.0-40.0 GHz systems. This MMIC uses Mimix Broadband's 0.15 µm GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Absolute Maximum Ratings

Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	250 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (Pin)	0 dBm
Storage Temperature (Tstg)	-65 to +165 °C
Operating Temperature (Ta)	-55 to +75 °C
Channel Temperature (Tch)	150 °C [3]
Heat Rise @ Nominal Bias	31 °C or 103 °C

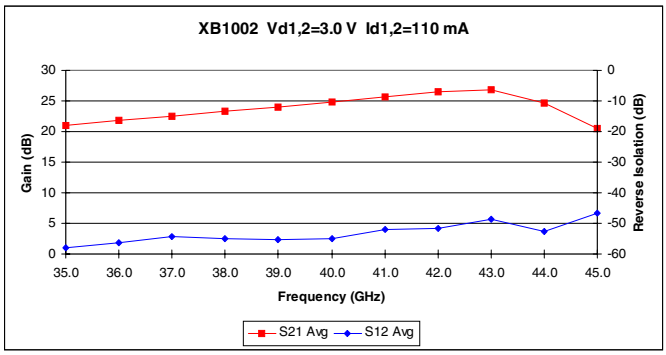
(3) Channel temperature effects a device's MTBF. It is recommended to keep channel temperature as low as possible for maximum life.

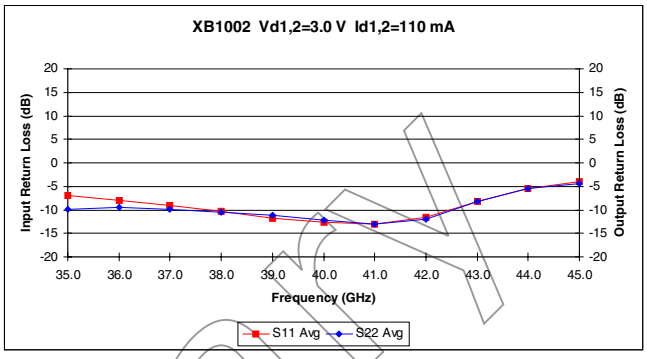
Electrical Characteristics (Ambient Temperature T = 25 °C)

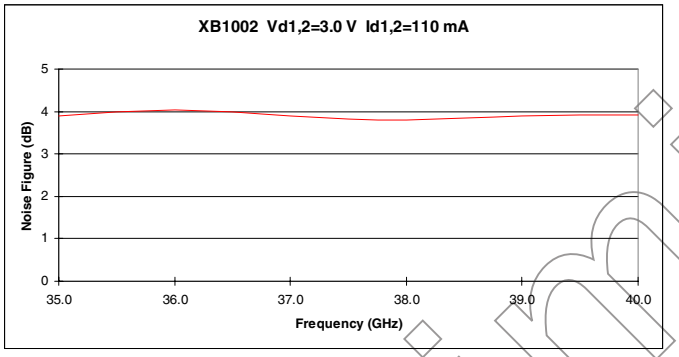
Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	36.0	-	43.0
Input Return Loss (S11)	dB	-	10.0	-
Output Return Loss (S22)	dB	-	9.0	-
Small Signal Gain (S21)	dB	-	25.0	-
Gain Flatness (ΔS21)	dB	-	+/-2.5	-
Reverse Isolation (S12)	dB	40.0	50.0	-
Noise Figure (NF)	dB	-	4.0	4.5
Output Power for 1 dB Compression (P1dB) [1,2]	dBm	+12.0	+14.0	-
Output Third Order Intercept (IP3) [1,2]	dBm	-	+26.0	-
Drain Bias Voltage (Vd1 & Vd2)	VDC	-	+3.0	+5.5
Gate Bias Voltage (Vg1 & Vg2)	VDC	-1.0	-0.5	0.0
Supply Current (Id) (Vd=3.0V, Vg=-0.3V Typical)	mA	-	110	220

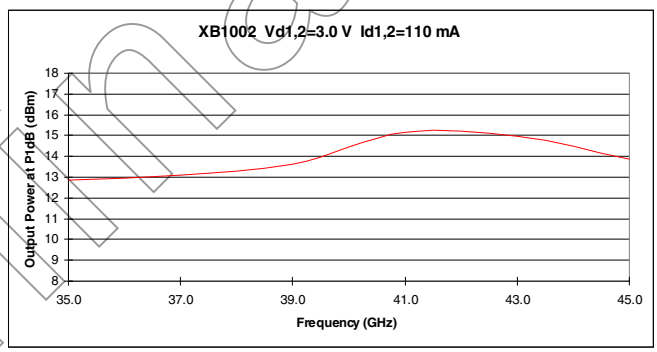
(1) Optional power bias Vd1,2=5.5V, Id=220mA will typically yield 3-6dB improved P1dB.
(2) Measured using constant current.

Power Amplifier Measurements

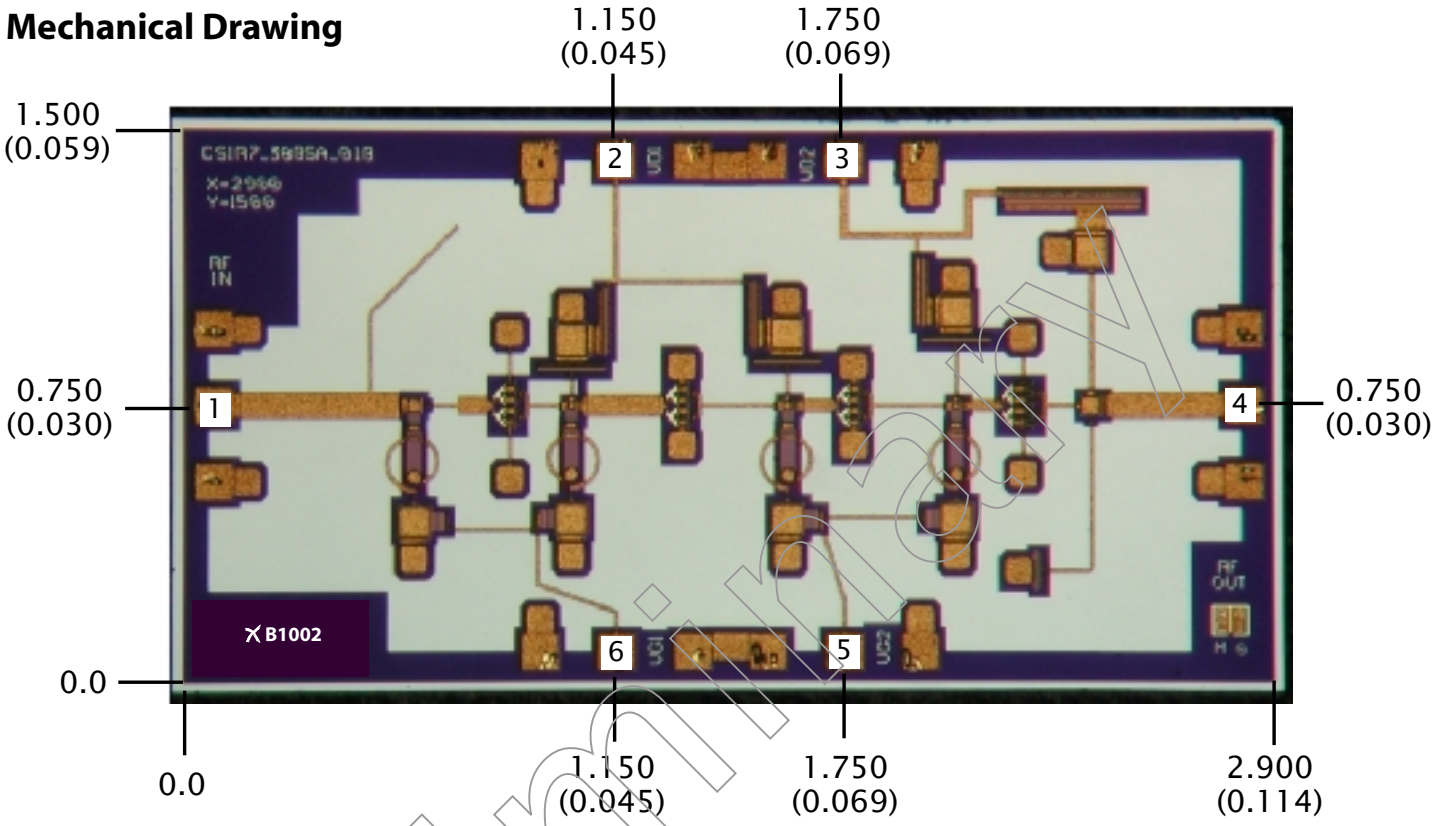








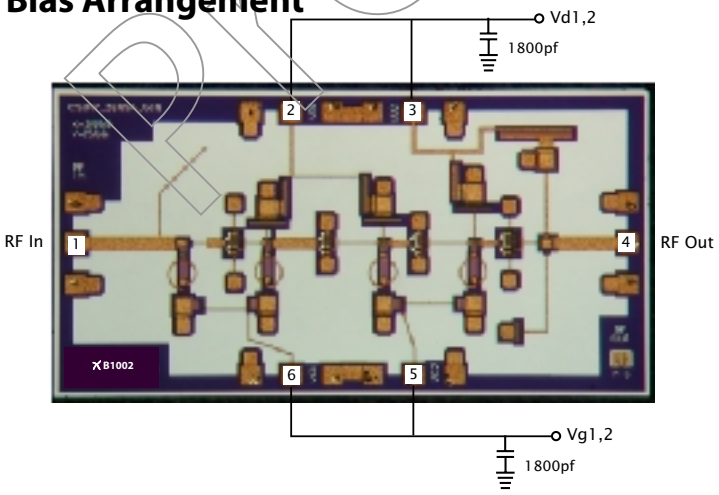
Mechanical Drawing



Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.100 (0.004) (for reference only), Backside is ground, Bond Pad/Backside Metallization: Gold
All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).

Bond Pad #1 (RF In)
Bond Pad #2 (Vd1)
Bond Pad #3 (Vd2)
Bond Pad #4 (RF Out)
Bond Pad #5 (Vg2)
Bond Pad #6 (Vg1)

Bias Arrangement



Bypass Capacitors - Recommended Capacitors can be found at Presidio Components (www.presidiocomponents.com)

For Individual Stage Bias:
4EA Single Element P/N - SL3535X7R182M16VG5
or
2EA Multiple Element P/N - SL3535X7R182M16VG1X25

For Parallel Stage Bias:
2EA Single Element P/N - SL3535X7R182M16VG5

App Note [1] Biasing - As shown in the bonding diagram, this device can be operated with all four stages in parallel, and can be biased for low noise performance or high power performance. Low noise bias is nominally Vd=3V, Id=110mA. More controlled performance will be obtained by separately biasing Vd1 and Vd2 each at 3.0V, 55mA. Power bias may be as high as Vd=5.5V, Id=220mA with all stages in parallel, or most controlled performance will be obtained by separately biasing Vd1 and Vd2 each at 5.5V, 110mA. It is recommended to use active biasing to keep the currents constant as the RF power and temperature vary, this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.5V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Handling and Assembly Information

CAUTION! - Mimix Broadband MMIC Products contain *gallium arsenide (GaAs)* which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- *Do not ingest.*
- *Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by products are dangerous to the human body if inhaled, ingested, or swallowed.*
- *Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.*

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from Mimix Broadband are 0.100 mm (0.004) thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001^2 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium should be avoided). The work station temperature should be 310°C $\pm$10°C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003 x 0.0005) 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001) diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.