Product Data Sheet

Device Features

- Bluetooth™ v1.1 Compliant
- Transmit Power 0dBm (Class 2)
- 2.7V to 3.3V Operation
- Full Bluetooth data rate over UART and USB
- Supports Device Firmware Upgrade (DFU) over USB and UART
- Four low power modes: Park, Sniff, Hold and Deep Sleep
- Piconet and Scatternet Capability
- Support for up to seven slaves

BC01MOD2B

Bluetooth Module

Production Information Data Sheet
Class 2 Reference Module

September 2001

General Description

BC01MOD2B is a class 2 surface mountable Bluetooth Module. It provides a fully compliant system for data and voice communications.

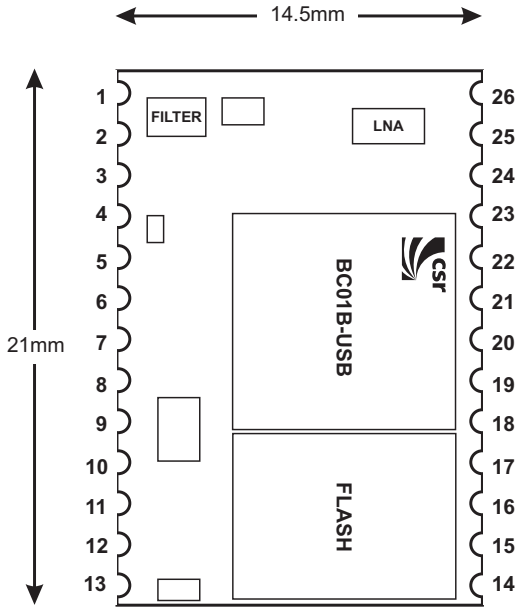
The physical interfaces to a host (UART and USB) can support full Bluetooth data rate of 723.2k/57.6kbps. A 13 bit PCM, 8k sample/sec, synchronous bidirectional audio interface is also available.

Applications

(Prototyping and development of)

- Laptop and Desktop PCs
- Mobile Phones
- Cordless Headsets
- Personal Digital Assistants (PDAs)
- Domestic and Industrial Appliances

Component Layout and Device Pinout Diagram



Module Height: 2.3mm

Figure 1: BC02MOD2B component layout

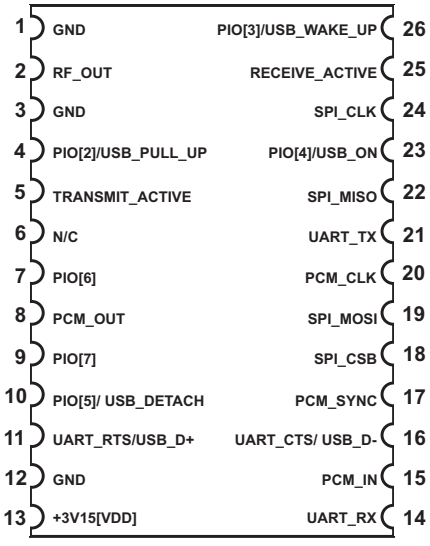


Figure 2: BC02MOD2B Pinout Diagram

Key Features

Radio

- Utilises BlueCore01b, CSR's single chip Bluetooth solution
- 0dBm output power for class 2 operation
- -84dBm receive sensitivity

Firmware

- Delivered with an HCI level stack
- Other stack options available by firmware upgrade: RFCOMM, On chip profiles and applications
- Firmware upgradable via USB or UART
- Extensive power saving modes, including Park, Hold, Sniff and Deep Sleep

Baseband

- All packet types supported. Piconet and Scatternet support
- Multiple physical application interfaces:
  - **UART:** Data and voice to 1.5Mbs^{-1}
  - **PCM:** Programmable, for voice13-bit 8kss^{-1} synchronous, bidirectional, serial audio interface
  - **USB:** Data and voice. V1.1 Compliant Supports OHCI and UHCI
- Trancoders for A-law, μ-law and CVSD for HCI voice traffic
- Support for up to seven slaves

Block Diagram

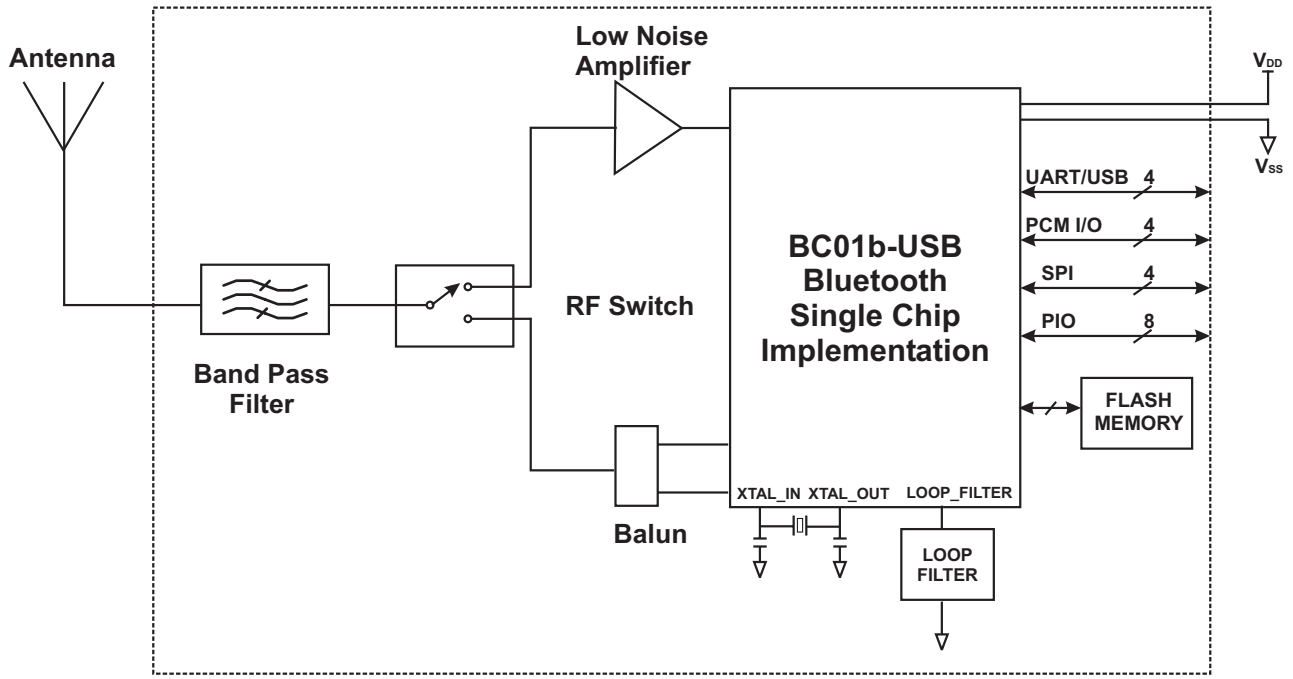


Figure 3: BC02MOD2B Block Diagram

Device Terminal Functions

Terminal Name	Terminal	Type	Description
GND	1	0V	RF ground
RF_OUT	2	Bidirectional	Antenna RF port (50Ω)
GND	3	0V	RF ground
PIO[2]/USB_PULL_UP	4	Bidirectional pulled down	Input /Output port or USB Pull-Up (via external 1.5kΩ resistor to D+)
TRANSMIT_ACTIVE	5	CMOS output	Output active high when data is transmitted over RF link
N/C	6	-	Not connected
PIO[6]	7	Bidirectional pulled down	Input /Output port
PCM_OUT	8	CMOS output, tristatable	Synchronous 8kss^{-1} data output
PIO[7]	9	Bidirectional pulled down	Input /Output port
PIO[5]/USB_DETACH	10	Bidirectional pulled down	Input/Output port or USB detach. Module detaches from USB when this line is high
UART_RTS/USB_D+	11	CMOS output	UART ready to send / USB D+
GND	12	GND	Module supply ground
+3V15[VDD]	13	VDD	Module supply positive, 3.15V Nominal
UART_RX	14	CMOS input, 5V tolerant pulled down	UART data input
PCM_IN	15	CMOS input pulled down	Synchronous 8kss^{-1} data output
UART_CTS/USB_D-	16	CMOS input	UART clear to send / USB D-
PCM_SYNC	17	Bidirectional pulled down	Synchronous data strobe
SPI_CSB	18	CMOS input, 5V tolerant pulled up	Serial Peripheral Interface chip select
SPI_MOSI	19	CMOS input, 5V tolerant pulled down	Serial Peripheral Interface data input
PCM_CLK	20	Bidirectional pulled down	Synchronous data clock
UART_TX	21	CMOS output	UART data output
SPI_MISO	22	CMOS output, tristatable	Serial Peripheral Interface data output
PIO[4]/USB_ON	23	Bidirectional pulled down	Input /Output port or USB on. (USB_ON senses when input is high and wakes BC01MOD2B)
SPI_CLK	24	CMOS input 5V tolerant pulled down	Serial Peripheral Interface clock
RECEIVE_ACTIVE	25	CMOS output	Output active high when module receives data over RF link
PIO[3]/USB_WAKE_UP	26	Bidirectional pulled down	Input /Output port or output goes high to wake up PC pulled down when in USB mode

Electrical Characteristics

Power Consumption

VDD = 3.15V Temperature = 20˚C, HCIStack1.1 v12

Mode	Avg	Peak	Unit
SCO connection HV3 (1s interval sniff mode) (Slave)	44	-	mA
SCO connection HV3 (1s interval sniff mode) (Master)	45	-	mA
SCO connection HV1 (Slave)	74	-	mA
SCO connection HV1 (Master)	68	-	mA
ACL data transfer 115.2kbps UART (Master)	23	-	mA
ACL data transfer 720kbps USB (Slave)	84	-	mA
ACL data transfer 720kbps USB (Master)	85	-	mA
Peak current during RF burst	-	135	mA
ACL connection, no data, Sniff Mode 40ms interval, 38.4kbps UART	5.5	-	mA
ACL connection, no data, Sniff Mode 1.28s interval, 38.4kbps UART	1.0	-	mA
Simultaneous Inquiry Scan and Page Scan 1.28s interval	2.1	-	mA
Simultaneous Inquiry Scan and Page Scan 2.56s interval	1.3		mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.85	-	mA
Deep Sleep Mode	80		µA

Radio Characteristics

VDD = 3.15V Temperature=20°C Frequency = 2.45GHz

Receiver	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER(1)	-	-84	-	≤-70	dB
Maximum received signal(1)	-	-20	-	≥-20	dB
C/I Co-channel(1)	-	9	-	≤11	dB
Adjacent channel selectivity C/I 1 MHz(1)	-	-2	-	≤0	dB
Image rejection C/I(1) (2)	-	-18	-	≤-9	dB
Transmitter	**Min**	**Typ**	**Max**	**Bluetooth specification**	**Unit**
Average RF transmit power(1)	-	0	-	-6 to +4	dBm
RF power control range(1)	-	40	-	≥16	dB
20dB bandwidth for modulated carrier	-	885	-	≤1000	KHz
2nd adjacent channel transmit power(1) (±2MHz)	-	-25	-	≤-20	dBm
3rd adjacent channel transmit power(1) (±3MHz)	-	-45	-	≤-40	dBm

Notes:
(1) Measured according to the Bluetooth specification with output power set to maximum.
(2) At carrier -3MHz.

Module Footprint

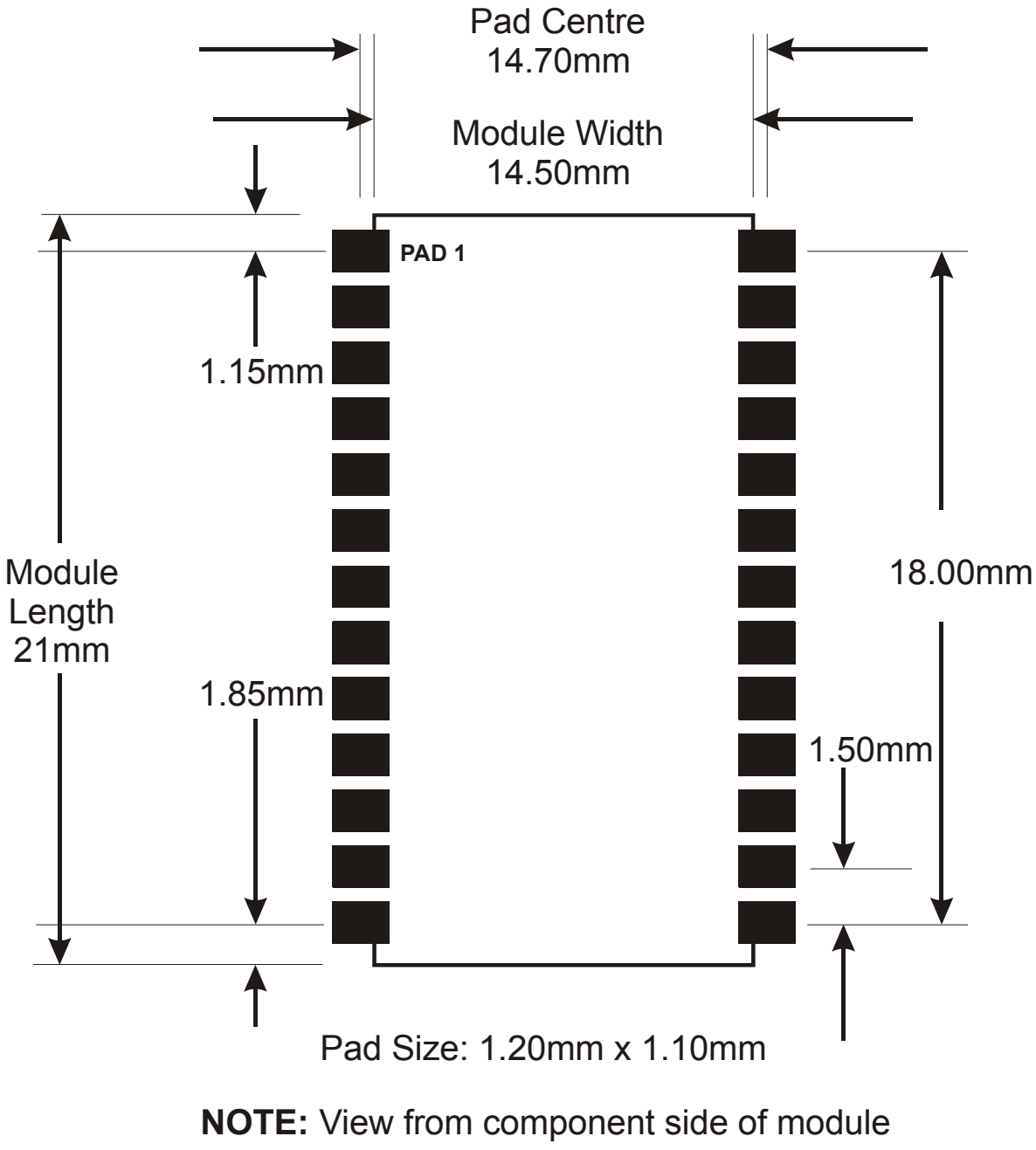


Figure 5: PCB Footprint Dimensions

Interface Descriptions

UART Interface

BC01MOD2B Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other digital devices using the RS232 standard.

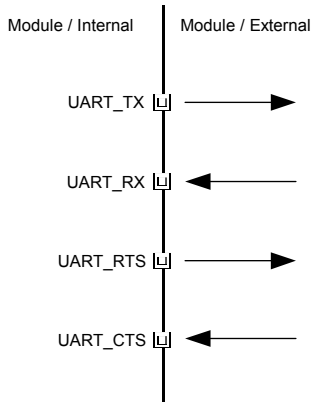


Figure 6: UART Interface

Four signals are used to implement the UART function, as illustrated above. When BC01MOD2B is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD (+3.15V nominal).

UART configuration parameters, such as Baud rate and packet format, are set using BC01MOD2B software. The following table details the possible settings.

Note: In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required.

Possible UART Settings

Parameter	Possible Values
Baud Rate	Min 1200 baud Max 1.382 Mbaud
Flow Control	RTS/CTS or None(1)
Parity	On or Off
Number of Stop Bits	1 or 2

The UART port also carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API and chip management. These channels are combined into a robust tunnelling protocol, where each channel has its own software flow control. (See separate documentation on BCSP).

The UART interface is capable of resetting BC01MOD2B upon reception of a Break signal. A Break is identified by a continuous logic low on the UART_RX terminal, as illustrated below. If ^{t}BRK is longer than a predefined constant, set by BC01MOD2B software, a reset will occur. This feature allows a host to initialise the system to a known state. Also, BC01MOD2B can emit a break character that may be used to wake the host.

Figure 7: Break Signal

Note:

(1) Software flow control is also provided. (See separate documentation on BCSP).

(2) The flash must be loaded through the Serial Peripheral Interface before the UART can be used.

Standard Baud Rates			
BaudRate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000A	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004F	79	0.45%
38400	0x009D	157	-0.18%
57600	0x00EC	236	0.03%
76800	0x013B	315	0.14%
115200	0x01D8	472	0.03%
230400	0x03B0	944	0.03%
460800	0x075F	1887	-0.02%
921600	0x0EBF	3775	0.00%
1382400	0x161E	5662	-0.01%

The Baud rate is set via a 2-byte Persistent Store Value according to the following formula:

$$\text{BaudRate} = \frac{\text{Persistent Store Value}}{0.004096}$$

Interface Descriptions (Continued)

USB Interface

BC01MOD2B contains its own full-speed (12Mbits/s) USB interface. The silicon is compliant with USB Specification 1.1, available from www.usb.org. Designers of circuits using the USB interface of BC01MOD2B are encouraged to read this specification, as it contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

BC01MOD2B operates as a peripheral USB device, responding to requests from a master host controller such as a PC. Both the Open Host Control Interface (OHCI) and the Universal Host Control Interface (UHCI) are supported (see Section H2 of the Bluetooth specification for more information).

The USB D+ and D- terminals are shared with UART terminals RTS and CTS. UART functionality is not available when the USB interface is operating. The mode of the terminals (USB or UART) is programmed by writing appropriate values to the Persistent Store.

USB 1.1 Compliance

Although BC01MOD2B is capable of meeting the USB 1.1 specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout, all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB 1.1 specification. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

BC01MOD2B has been independantly qualified to the USB 1.1 specification.

Power Supply

When supplying 20mA from a data line, the output voltage can fall to VDD -0.2V. Hence when operating from the recommended supply voltage of 3.15V, the USB data lines are driven to a minimum of 2.95V.

Bluetooth Compliance

BC01MOD2B implements a set of USB endpoints that behave as specified in the USB section of the Bluetooth Specification (H2). A suitable USB Bluetooth driver is required to provide an application interface to the Bluetooth communication system. CSR's USB driver for windows is available from *www.csr.com*.

USB Connections D+ and D-

The USB data lines emerge as D+ and D-. These terminals are connected to the internal USB Input/Output buffers of BC01MOD2B and, as such, have a low output impedance.

To match the connection to the characteristic impedance of the USB cable, series resistors must be included on both D+ and D-.

Detach and Wake_Up (Signalling)

The USB_DETACH and USB_WAKE_UP terminals provide extra signalling alongside the normal USB data lines. They are not part of the USB specification and full USB functionality can be attained without their use. Both functions can be separately enabled or disabled by setting values in the Persistent Store. USB_DETACH may be useful on its own. However, USB_WAKE_UP is unlikely to be used in isolation.

USB_DETACH (Disconnect Signalling)

USB_DETACH is an input when asserted high, which causes BC01MOD2B to put USB_PULL_UP, USB_D- and USB_D+ in a high-impedance state. This detaches the device from the bus and is logically equivalent to unplugging the device.

When USB_DETACH is taken low, BC01MOD2B will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP (Resume Signalling)

USB_WAKE_UP is an active high output, used only when USB_DETACH is active, to wake up the host and allow USB communication to recommence. It replaces the function of the USB WAKE_UP message, which cannot be sent while BC01MOD2B is effectively disconnected from the bus.

Power Modes

BC01MOD2B can operate in one of two power modes: self-powered or bus-powered.

Self-Powered Mode

In self-powered mode, the circuit is powered from its own independant power supply. It draws only a small leakage current (< 0.5mA) from VBUS on the USB cable. This is the easier mode to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BC01MOD2B via a resistor network (Rvb1 and Rvb2), so BC01MOD2B can detect when VBUS is powered up. BC01MOD2B will not pull D+ high when VBUS is off. Figure 8 demonstrates this connection.

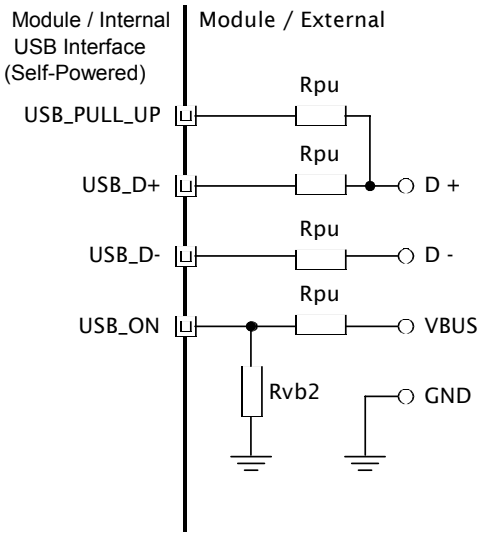


Figure 8: Connections to BC01MOD2B for Self-Powered Mode

Bus-Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BC01MOD2B negotiates with the PC during the USB enumeration stage about power consumption. It is recommended that the regulator used to derive 3.15V from VBUS is rated at 100mA average current and should be able to handle peaks of 200mA without foldback or limiting. In bus-powered mode, BC01MOD2B enumerates as a high power device, requesting 200mA.

When choosing a regulator, be aware that VBUS on the USB hub may go as low as 4.4V. The in rush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB v1.1 specification, section 7.2.4.1). Some applications may require soft-start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

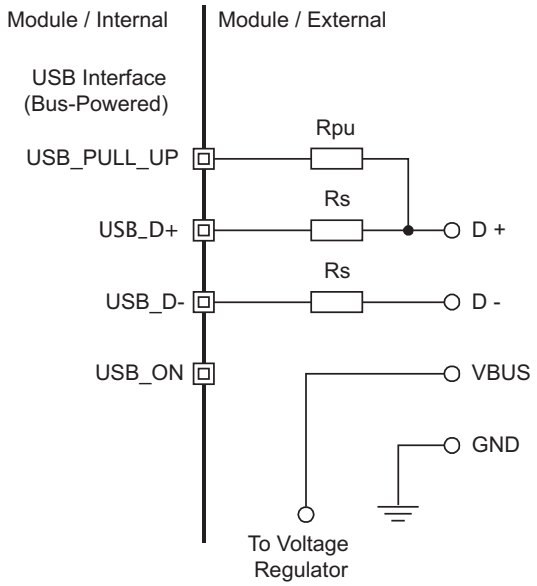


Figure 9: Connections to BC01MOD2B for Bus-Powered Mode

USB Interface Component Values

Identifier	Value	Description
R_{pu}	1.5kΩ 5% (see USB Spec 7.1.5)	USB Device speed identification
R_s	33Ω nominal (USB Spec 7.1.1.1) 1%	USB D+ data input/output
$R_{vb}1$	47kΩ 5%	VBUS ON sense divider
$R_{vb}2$	22kΩ 5%	VBUS ON sense divider

Note: USB_PULL_UP and USB_ON are shared with BC01MOD2B PIO terminals.

USB Timing Information

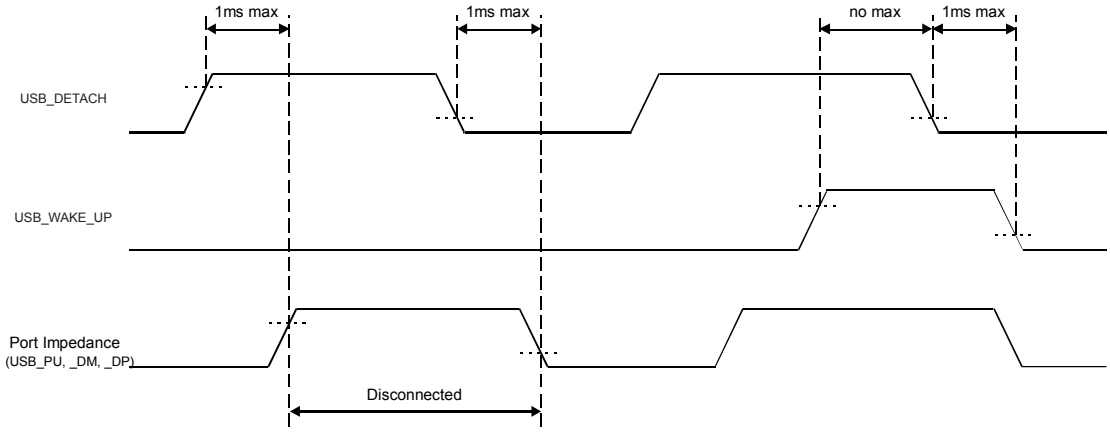


Figure 10 : USB_DETACH and USB_WAKE_UP Signal Timing

Additional Notes

USB Specification 2.0, (April 2000), does not make 1.1 obsolete: it merely defines a new higher-speed (480Mbit/s) addition to the USB protocol. Using USB 2.0 would offer no advantage to BC01MOD2B, as USB 1.1 12Mbit/s offers more than enough bandwidth to handle the Bluetooth data stream.

Terminals USB_D+ and USB_D- adhere to the USB Specification 1.1. For AC/DC specifications for terminals USB_DETACH, USB_WAKE_UP, USB_PULL_UP and USB_ON, refer to the PIO specification.

Interface Descriptions (Continued)

PCM Interface

Pulse Code Modulation (PCM) is the standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, BC01MOD2B provides hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for audio applications.

BC01MOD2B offers a bidirectional digital audio interface that routes directly into the Bluetooth baseband layer (it does not pass through the HCI protocol layer).

Hardware on BC01MOD2B allows the data to be sent to and received from a synchronous (SCO) connection. Only one SCO connection can be supported by the PCM interface at any one time. Any additional SCO connections must receive and transmit their data over the HCI protocol layer (i.e. over the UART or USB interfaces). The data format is 13-bit linear PCM. BC01MOD2B can operate either as a master (with an output clock of 256KHz) or as a slave (with the input clock varying between 128KHz and 512KHz).

When in slave mode and using higher clock rates BC01MOD2B can support Motorola's Synchronous Serial Interface (SSI) standard which allows multiple bidirectional audio channels to be multiplexed onto a single physical connection, although only one channel is utilised for BC01MOD2B. (See synchronous Serial Interface(SSI) section).

Generic PCM Interface

For a generic PCM interface there is one master and one slave device. The master generates the clock and synchronisation signals. The sync signal identifies the start of the sample data and has an 8KHz period. There are two types of frame sync: long and short. In long frame: sync mode PCM_SYNC going high, indicates the first (and most significant) bit of the sample. PCM_SYNC must remain high for at least two clock cycles, but this can be longer. In short frame: sync MSB start, is signalled by sync going low (normally it goes high only for one clock cycle).

The clock runs at a higher rate than sync (at least 8xbits per sample MHz, although higher rates are common). The standard uncompressed sample resolution is 13 bits per sample. The audio coding is linear. Several Motorola CODECs allow their output gain to be controlled via the addition of three extra data bits after the audio data. BC01MOD2B supports this feature, effectively raising the bits per sample to 16. Data from both the master and slave is clocked out on the rising clock edge and sampled on the falling edge.

Master mode is selected by setting a Persistent Store Value. In master mode BC01MOD2B generates a 256KHz clock signal (PCM_CLK) and the 8KHz long format synchronisation signal (PCM_SYNC). Short frame sync is not supported. See PCM Timing Diagrams for more information.

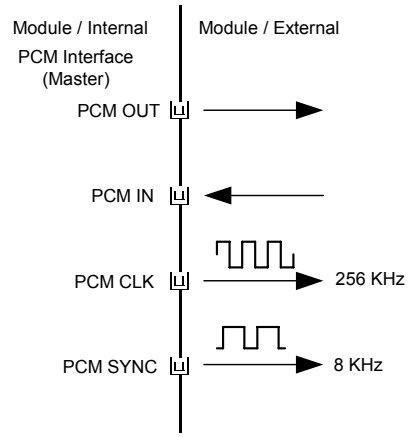


Figure 11: PCM Pinout, BC01MOD2B Master Mode Interface

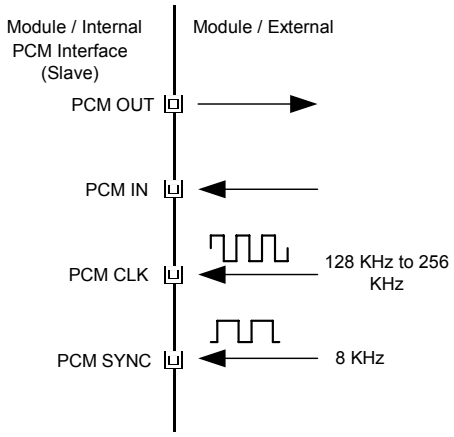


Figure 12: PCM Pinout, BC01MOD2B Slave Mode Interface

Interface Descriptions (Continued)

PCM Interface (Continued)

Synchronous Serial Interface

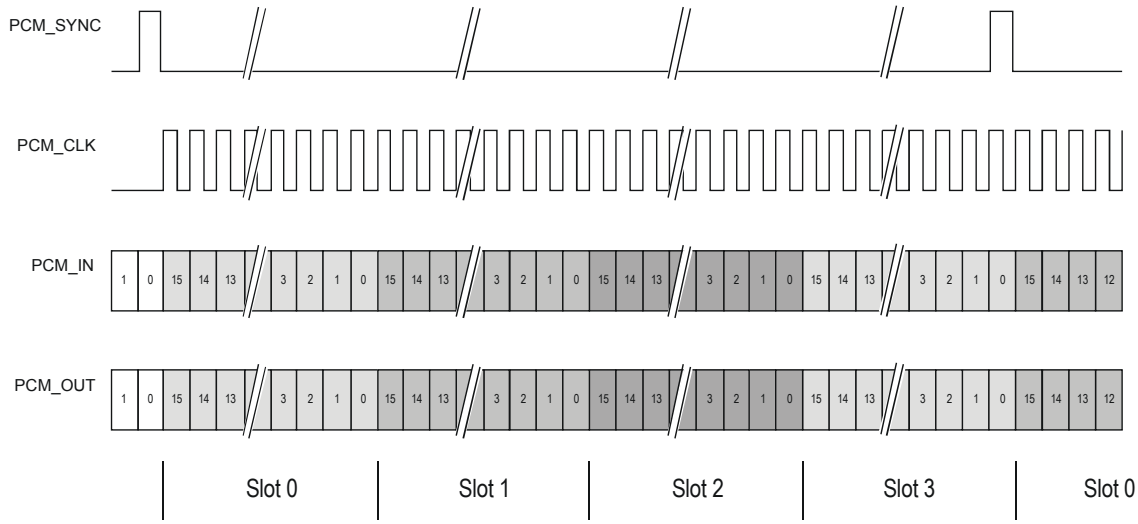


Figure 13 : SSI Mode Slot Timing

Synchronous Serial Interface (SSI) mode is selected by setting a Persistent Store Value. It is only available at 512KHz data rates with BC01MOD2B in slave mode and a short format frame sync pulse.

The concept is simple: four separate bidirectional channels (numbered 0 to 3) are time-division multiplexed onto one physical link. The data for channel 0 is sent first, followed immediately by that for channel 1, then channel 2 and finally channel 3. The sync pulse period remains at 8KHz and is sent at the start of the channel 0 slot. However, unlike the normal slave and master configurations, the sync format must be short frame.

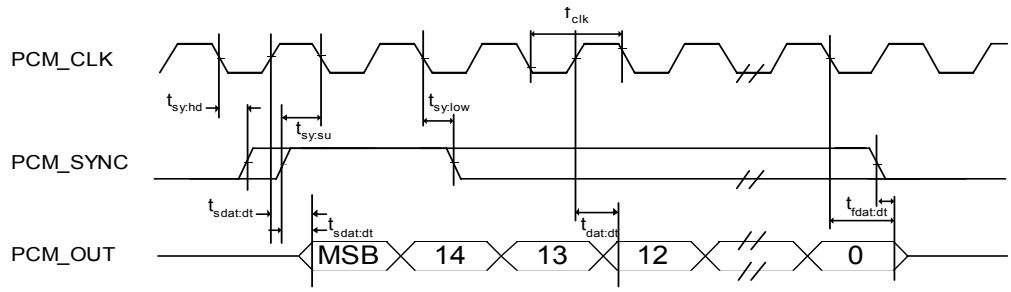
PCM_OUT is tristatable (i.e., goes to a high impedance state) shortly after the falling clock edge of the last bit in the active slot. This avoids conflict during the first bit of the next slot. If the SSI mode is configured to use slot 0, it may be considered a non-SSI mode device with short format frame sync, but it is restricted to operating at 512KHz.

PCM Timing Information

Master

Symbol	Parameter	Min	Typ	Max	Unit
$f_{clk=}$ $^{1/}$ t_{clk}	PCM clock frequency	-	256	-	KHz
(1)	Clock duty cycle	-	50	-	%
$t_{sy:hd}$	Hold time from CLK low to SYNC high	-	1.95	-	µs
$t_{sy:su}$	Set-up time for SYNC high to CLK low	-	1.95	-	µs
$t_{sdat:dt}$	Delay time from SYNC high or CLK whichever is later to valid MSB data	-	-	50	ns
$t_{dat:dt}$	Delay time from CLK high to PCM_OUT valid data	-	-	50	ns
$t_{fdat:dt}$	Delay time from SYNC or CLK, whichever is later, to PCM_OUT data line high impedance	-	-	300(1)	ns
$t_{sy:low}$	Hold time from 2nd CLK to SYNC low	-	-	300(1)	ns
$t_{dr:su}$	Set-up time for PCM_IN valid to CLK low	300(1)	-	-	ns
$t_{dr:hd}$	Hold time for CLK low to PCM_IN invalid	300(1)	-	-	ns

Note:(1) Assumes normal system clock operation. Figures may vary during low power modes when system clock speeds are reduced.



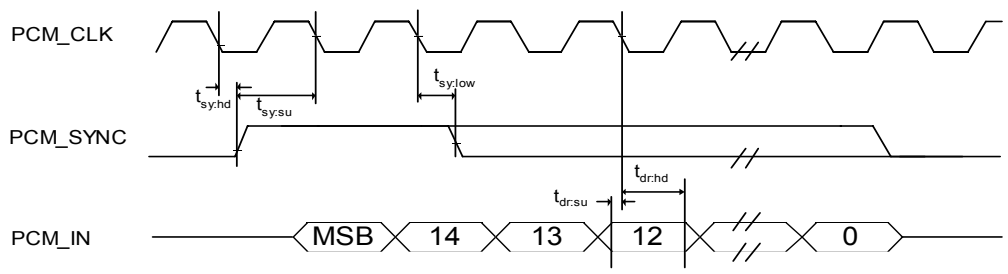


Figure 14: PCM Master Timing

Slave

Symbol	Parameter	Min	Typ	Max	Unit
$f_{clk} = {}^{1}/_{t_{clk}}$	PCM clock frequency (slave mode - input)	128	-	512	KHz
t_{low}	PCM clock low time	300	-	-	ns
t_{high}	PCM clock high time	300(1)	-	-	ns
t_r	PCM digital rise time	-	-	50	ns
t_f	PCM digital fall time	-	-	50	ns
$t_{sy:hd}$	Hold time from CLK low to SYNC high	300(1)	-	-	ns
$t_{sy:su}$	Set-up time for SYNC high to CLK low	300(1)	-	-	ns
$t_{sdat:dt}$	Delay time from SYNC or CLK, whichever is later, to valid MSB data	-	-	300(1)	ns
$t_{dat:dt}$	Delay time from CLK high to PCM_OUT valid data	-	-	300(1)	ns
$t_{fdat:dt}$	Delay time from SYNC or CLK, whichever is later, to PCM_OUT data line high impedance	-	-	300(1)	ns
$t_{sy:low}$	Hold time from 2nd CLK to SYNC low	300(1)	-	-	ns
$t_{dr:su}$	Set-up time for PCM_IN valid to CLK low	300(1)	-	-	ns
$t_{dr:hd}$	Hold time for CLK low to PCM_IN invalid	300(1)	-	-	ns

Note:(1) Assumes normal system clock operation. Figures may vary during low power modes when system clock speeds are reduced.

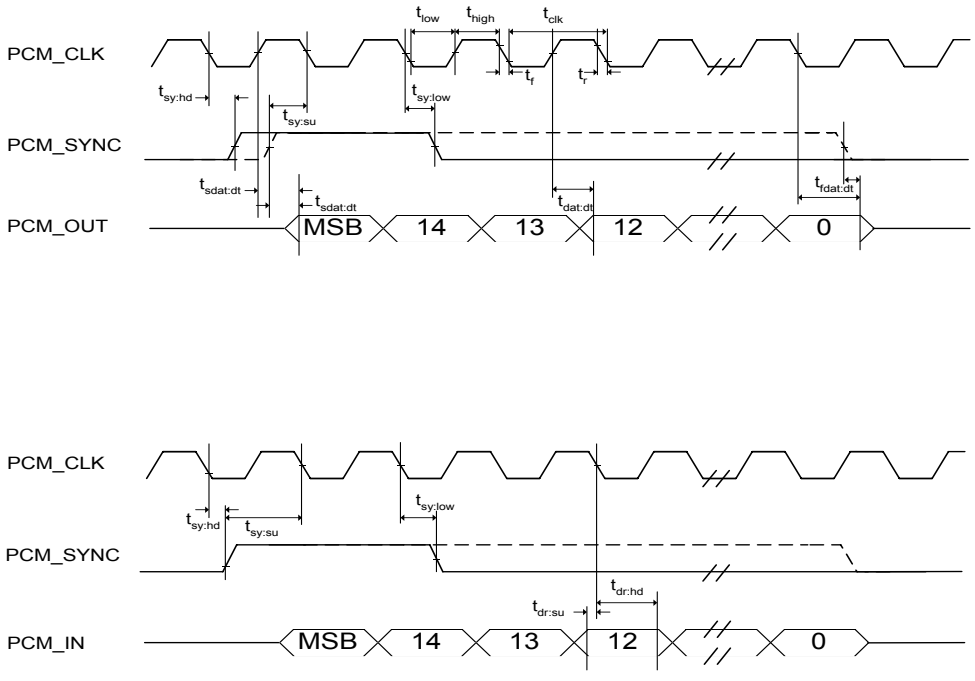


Figure 15: PCM Slave Timing

Interface Descriptions (Continued)

PIO

The Parallel Input Output (PIO) Port is a general-purpose input/output interface to/from BC01MOD2B. The port consists of six programmable, bi-directional I/O lines, PIO[2:7].

Programmable Input/Output can be accessed either via an embedded application running on BC01MOD2B or via private channel or manufacturer-specific HCI commands. See Bluelab documentation for more details.

RECEIVE_ACTIVE

This is used internally, to control the radio front end receive switch and indicates when the RF receiver is active.

TRANSMIT_ACTIVE

This is used to control the radio front end transmit switch and indicates when the RF receiver is active.

PIO[2] / USB_PULL_UP

This is a multifunction terminal. The function depends on whether BC01MOD2B is being used with a USB or UART connection.
On UART connected applications this terminal is used as a programmable I/O. For USB connected applications it drives a pull-up resistor. (See USB section).

PIO[3] / USB_WAKE_UP

This is a multifunction terminal. The function depends on whether BC01MOD2B is being used with a USB or UART connection.
On UART versions, this terminal is a programmable I/O. For USB connected applications, its function is selectable via a Persistent Store Value either as a programmable Input/Output or as a USB_WAKE_UP function.

PIO[4] / USB_ON

This is a multifunction terminal. The function depends on whether BC01MOD2B is being used with a USB or UART connection.
On UART versions, this terminal is a programmable Input/Output. For USB versions the USB_ON function is also selectable. (See USB Interface section).

PO[5] / USB_DETACH

This is a multifunction terminal. The function depends on whether BC01MOD2B is being used with a USB or UART connection.
On UART versions, this terminal is a programmable Input/Output. For USB versions the USB_DETACH function is also selectable. (See USB Interface section).

PIO[6]

Programmable Input/Output terminal.

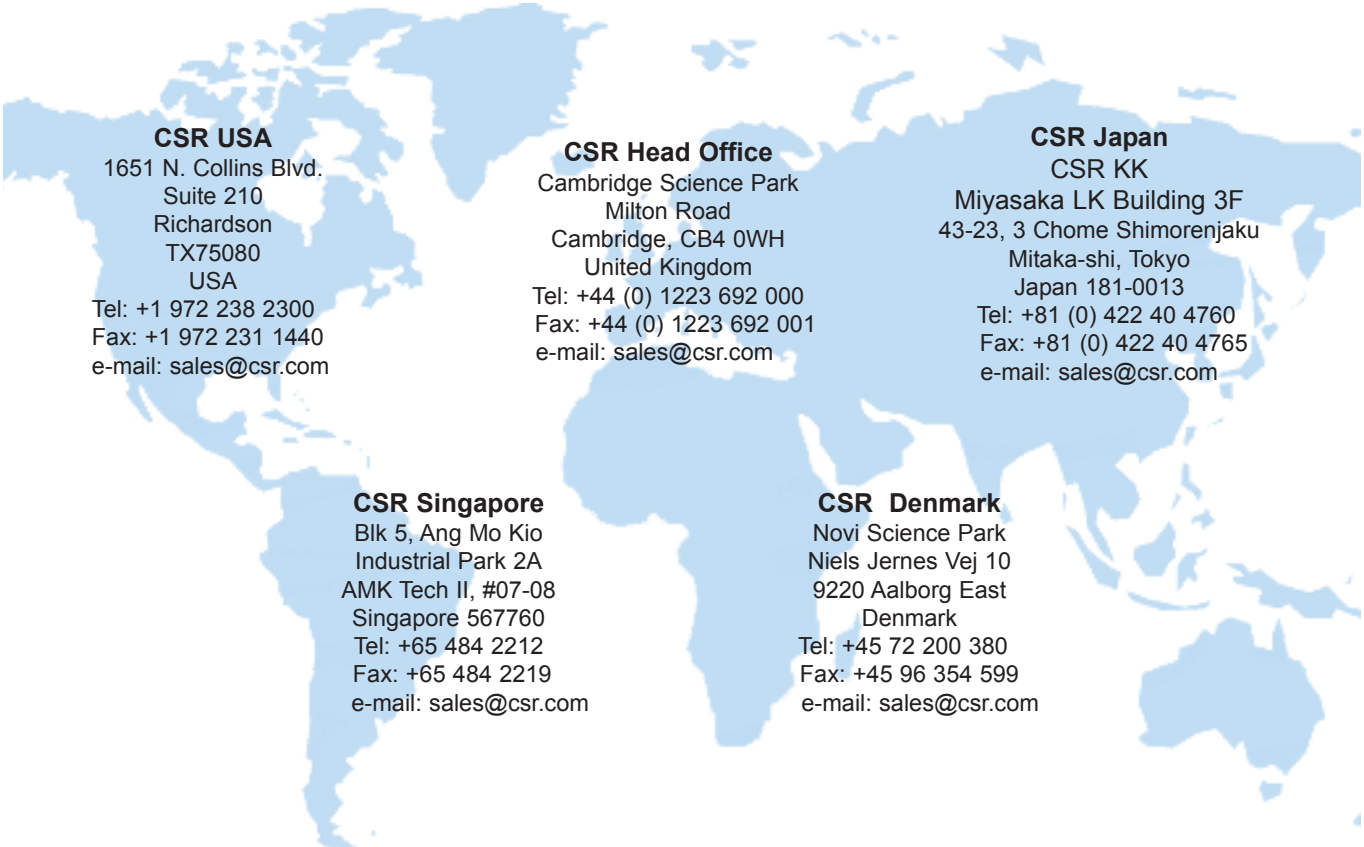
PIO[7]

Programmable Input/Output terminal.

Ordering and Contact Information

Order Number	Description
BC01MOD2B	Class 2 Modules. Note that the M.O.Q. is 10 and is delivered with: 2 CBMOD2 carrier boards 2 ANT001 antennas

Contact CSR Worldwide



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To contact a CSR representative, please go to www.csr.com/contacts.htm

Status of Information

The progression of CSR Product Data Sheets follows the following format:

a) Advance Information

Information for designers on the target specification for a CSR product in development.
All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

b) Pre-Production Information

Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

c) Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications. Production Data Sheets supersede all previous document versions.

The status of this Data Sheet is **Production Information.**

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications.

Record of Changes

Date:	Revision:	Reason for Change:
17th May 2001	bc01-ds-MOD2ESa	Original publication of this document
24th September 2001	bc01b-ds-MOD2Bb	Production information added to original Data Sheet

BC01MOD2B Product Data Sheet

bc01b-ds-MOD2Bb

September 2001