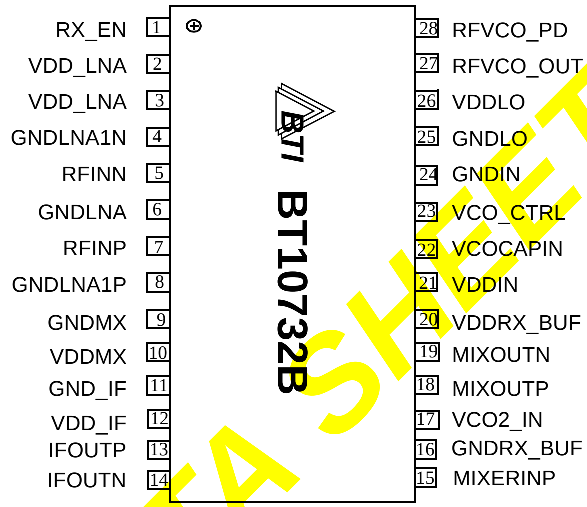
900MHz RF RECEIVER

Features

- Complete RF receiver front end
- On-chip RF local oscillator
- Single power supply 2.7 - 3.3 V
- Low power BiCMOS technology
- Ambient temperature range (-40^{o}C to +85^{o}C)
- 28L SSOP package



Applications

- 900 MHz Digital Telephones
- Wireless Communication Products
- Cordless Telephones
- Spread Spectrum Voice and Data
- Wireless Communication Products
- Wireless Networking Products
- 902-928 MHz ISM Band Applications

Description

The BT10732B is a BiCMOS monolithic integrated RF transceiver. With an RF input/output signal range of 850MHz to 950MHz, it is ideally suited for use in digital cordless phones. Designed for use with the BT10731B transmitter, the IC contains all of the required components to implement a complete RF-IF transceiver. The BT10732B includes an RF local oscillator, a low noise amplifier with an overall noise figure of less than 3.5dB over temperature and power supply variations, two highly linear down-conversion mixers, and an IF amplifier. The unit operates with a power supply voltage range of 2.7 - 3.3 volts.

Specifications

Parameters	Min.	-3σ	Typ.	+3σ	Max.	Units
Overall:						
Power supply	2.7		3.0		3.3	V
Standby current	3		5		7	uA
Frequency operation	850				950	MHz
Receiver:						
Gain (using the optional IF AMP)	18		26		50	dB
Noise Figure			3.5			dBm
Input IP3			-13			dB
Current consumption (w/ RF VCO)			80			mA
Receiver Section						
LNA:						
Gain	14		17		20	dB
Input IP3			-11			dBm
Input 1dB compression point			-21			dBm
Noise figure	1.5		2.9		4.7	dB
S11	-10		-14		-17	dB
Input impedance			50			Ω

Parameters	Min.	-3σ	Typ.	+3σ	Max.	Units
RF Downconversion Mixer and Buffer:						
Gain	4		9		10	dB
Input IP3			5			dBm
Input 1dB compression point			-5			dBm
Noise figure			11			dB
Output Impedance			700			Ω
IF Downconversion Mixer & IF Amp:						
Gain	4		9		10	dB
Input IP3			5			dBm
Input 1dB compression point			-5			dBm
Noise figure			11			dB
Input Impedance			700			Ω
Output Impedance			330			Ω
RF VCO Section						
Frequency range (at output to PLL)	750		770		800	MHz
VCO phase noise at 100KHz offset (closed-loop)			-100			dBc/Hz
VCO phase noise at 1MHz offset			-120			dBc/Hz

Absolute Maximum Ratings

Parameters	Value	Unit
Supply Voltage	7	V
Power Control Voltage	V_{DD}+0.5	V
Storage Temperature	+150	°C

Pin Table

Pin	Parameter	I/O	Description
Power and Ground Pins			
6 / 4/8	GNDLNA / GNDLNA1N/ GNDLNA1P	-	Ground to LNA
24 / 25	GNDIN / GNDLO	-	Ground to RFVCO
11 / 16	GND_IF / GNDRX_BUF	-	Ground to receiver buffers
9	GNDMX	-	Ground to Down Conversion Mixer
2/3	VDD_LNA	-	Power supply to LNA
21 / 26	VDDIN / VDDLO	-	Power supply to RFVCO
12 / 20	VDD_IF / VDDRX_BUF	-	Power supply to receiver IF buffer
10	VDDMX	-	Power supply to Down Conversion Mixer
RF Local Oscillator Pins			
27	RFVCO_OUT	O	RF VCO output
23	VCO_CTRL	I	RF VCO control input
22	VCOCAPIN	I	External Tuning capacitor for RFVCO

Pin	Parameter	I/O	Description
Receiver Pins			
5 / 7	RFINN / RFINP	I	RF Differential Input to the receiver
13 / 14	IFOUTP / IFOUTN	O	Differential output of the first downconversion mixer
17	VCO2_IN	I	Input of the second IF downconversion mixer (from the external crystal)
15	MIXERINP	I	Input of the second IF downconversion mixer
18 / 19	MIXOUTP / MIXOUTN	O	Differential output of the second IF downconversion mixer
Power Down Pins			
1	RX_EN	I	Receiver power down control
28	RFVCO_PD	I	RFVCO power down control

Detailed Pin Descriptions

RECEIVER

RFINP and RFINN (Pin 7 and Pin 5)
RF Differential Input pins
RF_INP and RF_INN are the differential Inputs of the LNA. An AC coupling capacitor of 10pF is required. RF differential inputs are generated by an external phase-splitter circuit and a matching circuit as shown in the **Application Circuit** . For optimum performance, the component lead length of the external phase-splitter circuit and PCB traces to the LNA input pins should be minimized. Also, the ground plane must surround the phase -splitter circuit to prevent noise coupling from other circuits. The frequency range is from 800MHz to 1000MHz.

IFOUTP and IFOUTN (Pin 13 and Pin 14)
First IF Differential Output pins
These are the differential output pins of internal IF buffers. With an external IF combiner circuit (*as shown in the Application Circuit*), the differential outputs become single-ended signals required to drive the 150.05MHz BPF SAW filter. The internal IF buffers have open-drain outputs to drive the impedance of a 330Ω BPF through an external combiner circuit.

MIXERINP (Pin 15)
Second IF Amplifier Input
The output of a 150.05MHz BPF SAW filter is connected to this pin for the second down-conversion. No AC coupling is required.

MIXOUTP and MIXOUTN (Pin 18 and Pin 19)
Second IF Differential Outputs
These pins are the second IF Amp differential outputs. The gain of the IF Amp can be controlled by connecting MIXOUTP through a resistor to ground. Normally a 470Ω resistor to ground gives a 0 dB gain. The other Amp output, MIXOUTN, is fed to a 10.7MHz BPF through a 0.1uF AC coupling capacitor.

VCO2_IN (Pin 17)
External Clock Input
A clock of 139.35MHz is fed to this pin to down-convert the first IF at 150.05MHz to 10.7MHz. No AC coupling is required.

VDD_LNA (Pin 2 and Pin 3)
LNA power
VDD_LNA supplies power to the first and second stages of the LNA. Since the LNA input signal level is small and high frequency, the VDD_LNA should be decoupled very close to the chip (*i.e. within 0.25 inches of the package*).

GNDLNA1P, GNDLNA1N and GNDLNA (Pin 8, Pin 4 and Pin 6)
LNA Ground
The GNDLNA1P and GNDLNA1N pins are the ground for the first stage of LNA and GNDLNA is the ground for the second stage of LNA. GNDLNA1P and GNDLNA1N are internally separated. For stability and optimum performance, GNDLNA1P and GNDLNA1N should be physically short.

VDDMX (Pin 10)
Down Converter Power
VDDMX supplies power to the down conversion mixers.

GNDMX (Pin 9)
Down Converter Ground
GNDMX is the ground for the down-conversion mixers. This ground connection is recommended to be shorted via holes to the underside ground plane.

VDD_IF and VDDRX_BUF (Pin 12 and Pin 20)
IF Buffers and Second Down-Conversion Mixers Power
Both power supplies require 0.1uF bypass capacitors to ground.

GND_IF and GNDRX_BUF (Pin 11 and Pin 16)
IF Buffers and Second Down-Conversion Mixers Ground
GND_IF is the ground for the internal IF buffers, and GNDRX_BUF is the ground for the second down-conversion mixers and IF amplifiers.

RFVCO

VCO_CTRL (Pin 23)
RFVCO Input Control
An external tank circuit is connected to this pin - VCO_CTRL (*see Application Circuit*). The tank circuit generates the overall oscillation frequency for the RFVCO and therefore must be optimized to avoid any interference from other components. The VCO_CTRL pin and the external PLL completes the RF-PLL loop that generates a fixed oscillation frequency for the RFVCO. An external VCO can also be used to drive this input if such a source is available and preferred over the on-chip VCO.

RFVCO_OUT (Pin 27)
RFVCO Output
This is the RFVCO output pin designed to drive the 50Ω input impedance of the external RFPLL/Frequency synthesizer.

VCOCAPIN (Pin 22)
RFVCO Tank circuit Input
This pin is used in conjunction with VCO_CTRL (pin# 23) to form the external tank circuitry for the on-chip RFVCO.

VDDIN and GNDIN (Pins 21 and 24)
RFVCO Input Stage Power Supply and Ground
VDDIN is the power supply for the input stage of the RFVCO. For optimum performance, VDDIN should be bypassed to GNDIN using a high frequency decoupling capacitor. The input stage of the RFVCO is very critical in generating the overall frequency of the RFVCO, therefore, isolating the power supply pins - VDDIN and GNDIN will enhance the overall performance of the RFVCO.

VDDLO and GNDLO (Pin 26 and 25)
RFVCO Power Supply and Ground
VDDLO and GNDLO provide the power supply for the remaining stages of the RFVCO.

POWER SAVING/POWER DOWN PINS
The following pins are all CMOS digital interface.

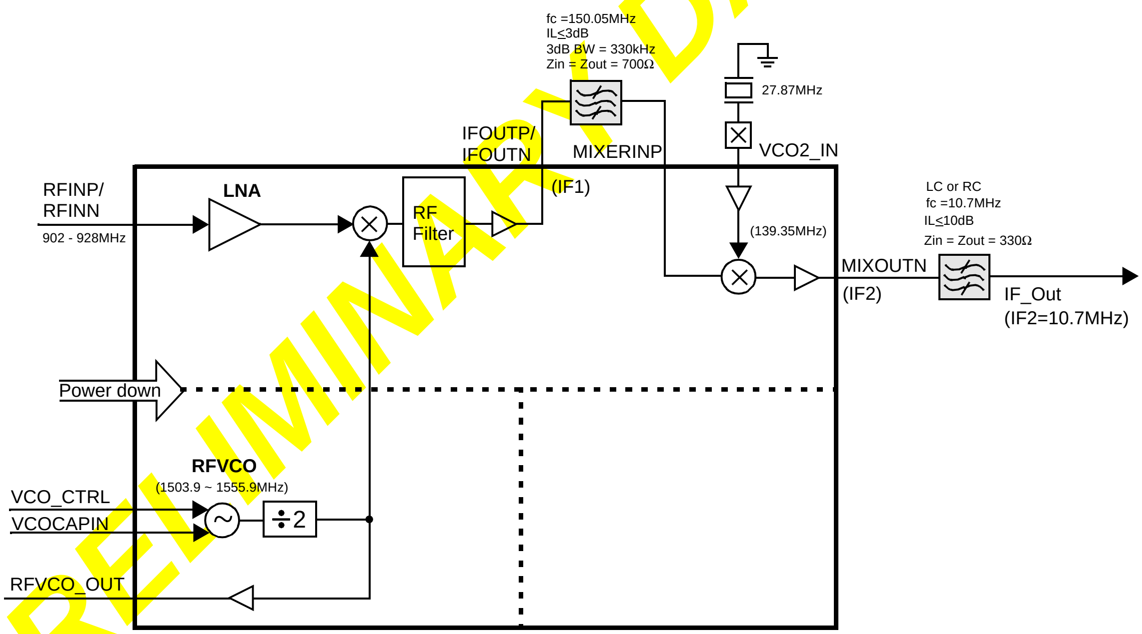
RFVCO_PD (Pin 28)
RF VCO Power Down Control
This pin controls the power down function of the RFVCO. A HIGH signal turns the circuit *off* while a LOW signal turns the circuit *on*.

RX_EN (Pin 1)
Receiver Power Down Control
This pin controls the power down function of the entire receiver. A HIGH signal turns the circuit on while a LOW signal turns the circuit off.

The recommended TDD mode as well as power saving mode usage of all these control pins are as follows:

Pins	Communication Mode	Power Save
	RX	
RX_EN	HI	LO
RFVCO_PD	LO	HI

Block Diagram



Typical Performance Characteristics

RECEIVER:

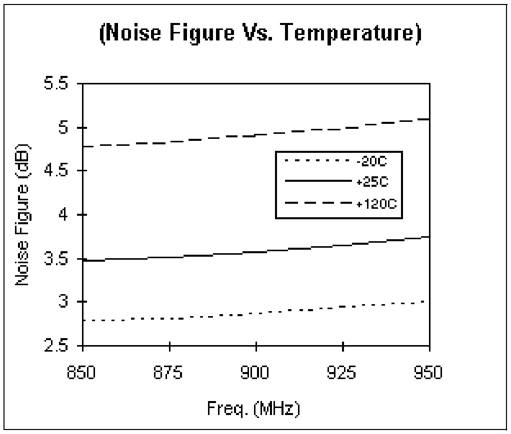


Figure 1. NF vs. Freq, varying temp.

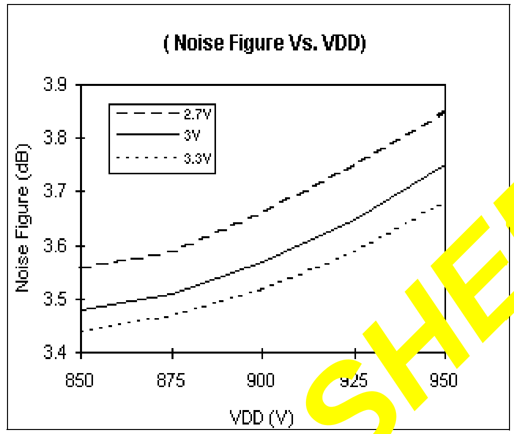


Figure 2. NF vs. Freq, varying vdd

TBD

Figure 3. Gain vs Freq, varying temp.

TBD

Figure 4. Gain vs Freq, varying vdd

TBD

Figure 5. IF amp: Res. vs. Gain, varying temp.

TBD

Figure 6. IF amp: Res. vs. Gain, varying VDD

RFVCO:

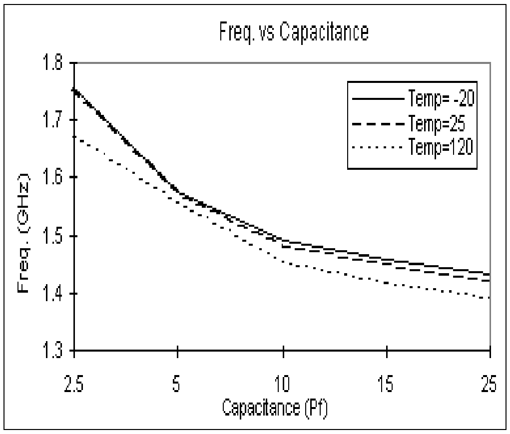


Figure 7. Freq vs. Cap., varying temp.

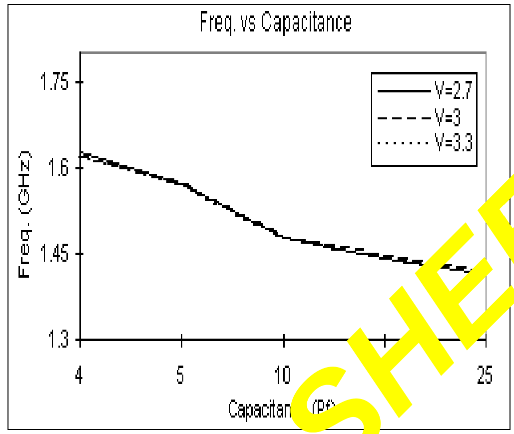


Figure 8. Freq vs. Cap., varying vdd

Application Information:

The BT10732B is a BiCMOS monolithic integrated RF receiver (Rx) designed for use with the BT10731B transmitter. The BT10731B/BT10732B contains all of the required components for a complete RF-IF transceiver. The BT10732B includes an RF local oscillator, a Low Noise Amplifier (LNA), and two on-chip downconversion mixers for the RF and IF stages. The unit operates from 2.7 - 3.3 volts.

An external bandpass filter is provided between the two IF stages for optimum noise performance. An external crystal/multiplier combination is required for the VCO2_IN pin to obtain the 10.7MHz second IF frequency that interfaces with a demodulator/data slicer. The IF output signals are differential and require a power combiner as shown in the Application Circuit (*Figure 2*). .

The RF local oscillator is conveniently provided on-chip and can be used with an external RF PLL frequency synthesizer. The RF local oscillator requires external tuning elements, as shown in the Application Circuit (*Figure 2*) to achieve the required oscillation frequency.

The BT10732B provides power-down pins for the different sections of the chip. The power down/power save mode can be implemented on the BT10732B by a microcontroller (*see Application Circuit, Figure 2 for more power down information*).

The BT10732B uses an advanced silicon BiCMOS process which provides superior performance compared to existing discrete components. The BT10732B chip demonstrates low sensitivity to process and temperature variations and the power consumption of the unit is less than 270mW under typical conditions from a 3V power supply.

The recommended usage for the BT10732B is shown below in *Figure 1.*

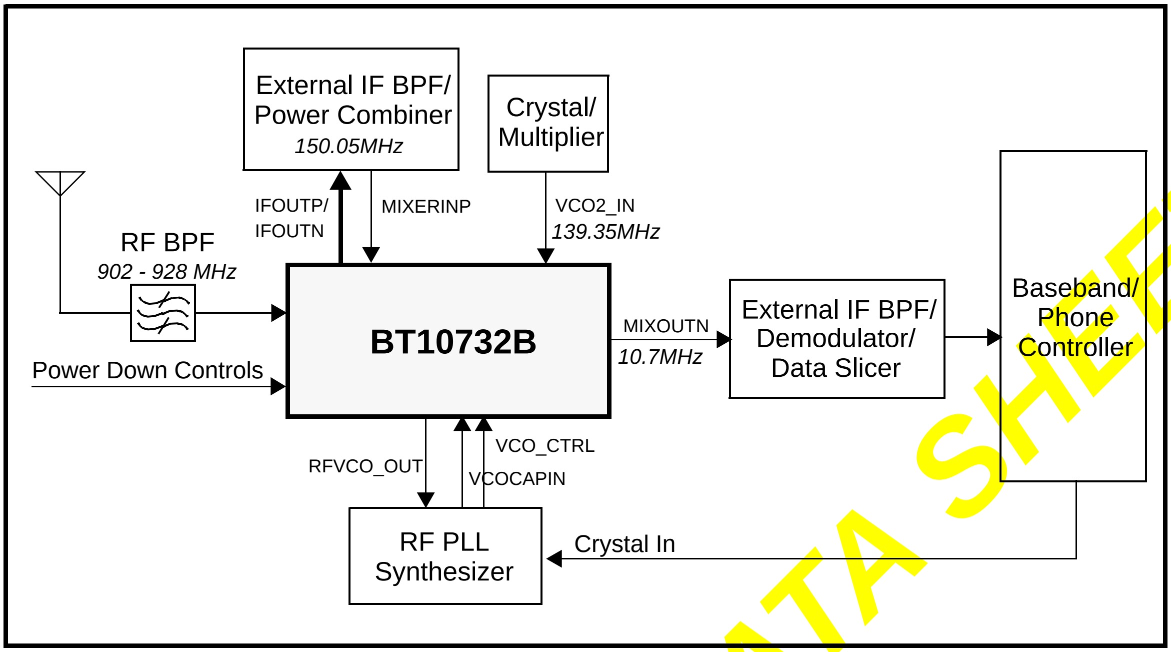


Figure 1

Typical Application Circuit:

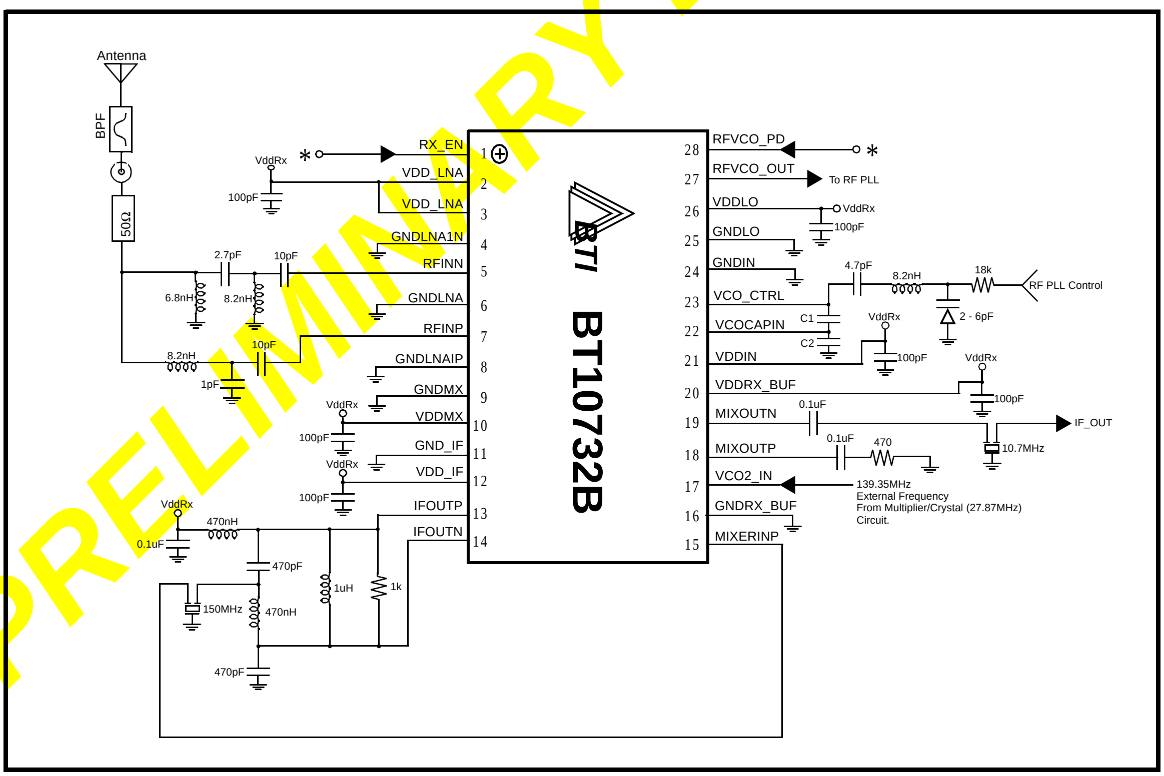


Figure 2

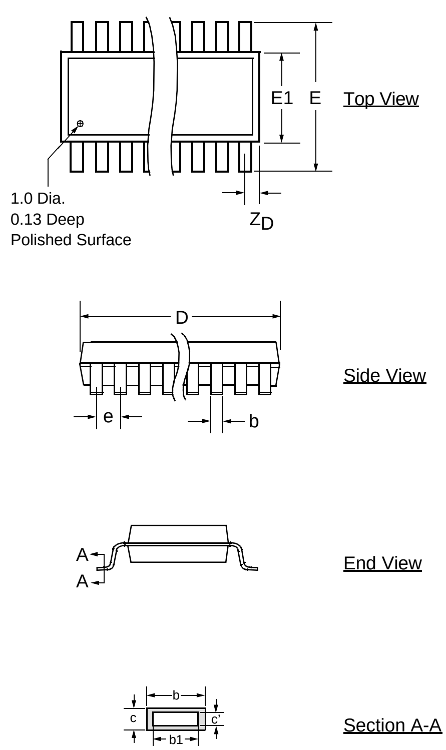
Notes :

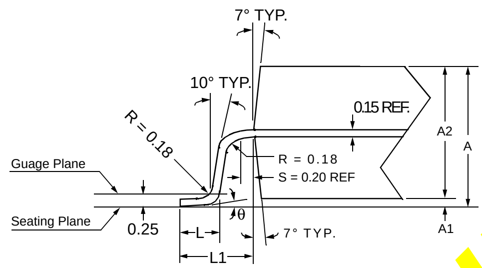
* Power Down Mode:

RFVCO_PD = ***vdd*** for power down mode, ***gnd*** for operational mode.
RX_EN = ***gnd*** for power down mode, ***vdd*** for operational mode.

Package Dimension

28L (150mils) 3.9mm Wide SSOP Package





Lead Count		28L
Body Thickness		2.00
Footprint (Body+)		2.50
Dimensions	Tolerance	
A	Max.	2.00
A1		0.05 Min/0.21 Max
A2	± 0.05	1.70
D	± 0.05	7.20
E	± 0.10	5.99
E1	± 0.10	1.47
L	+0.15/-0.10	0.80
L1	Ref.	1.25
e	Basic	0.65
b	± 0.05	0.30
c		0.13 Min/0.20 Max
Z_D	Ref.	0.20
θ	±4°	0.675

Package dimensions in mm.

Ordering Information

Part No./ Description	For:	Contact:
BT10732B **RF RECEIVER**	• Pricing Information • Application Assistance • Application Notes • Samples & Eval Boards • Other TRFIC™ products	USA:* BethelTronix, Inc. Tel: (562) 407-0500 Fax: (562) 407-0510 *see our WEB SITE for a list of our world wide sales reps

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