BtT9170

Intelligent T1 Controller

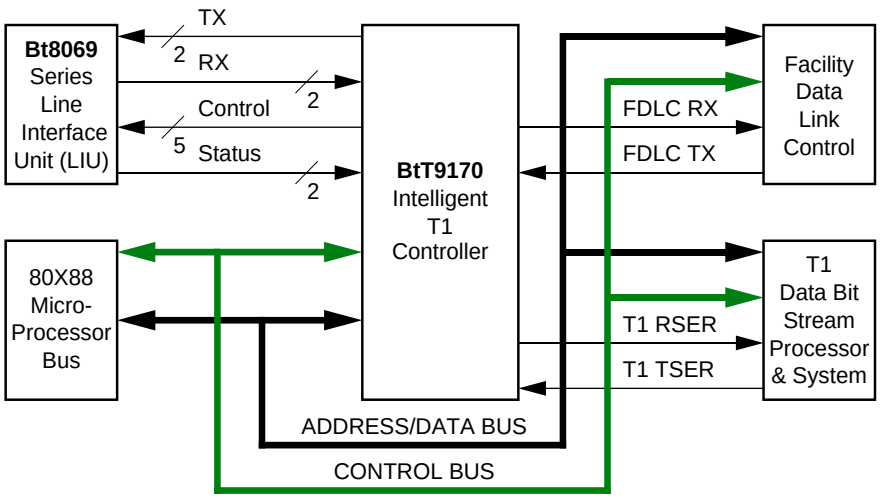
Product Description

The BtT9170 Intelligent T1 Controller is a microprocessor (MPU) controlled device which implements a T1 interface between the multiplexed digital DS1 signal and the PCM highway of digital voice and data system equipment. The BtT9170 handles both D4 (SF) and D5 (ESF) standards with Facility Data Link (FDL) used in T1, ISDN primary-rate, and digital carrier systems.

Designers are provided a cost-effective solution for T1/ISDN primary-rate interface that integrates complex functions to minimize system development time, component count, board space, and cost. Combining dedicated control pins with MPU-addressable registers, maximum functional control is achieved with minimal MPU intervention. The BtT9170 provides direct control over the Bt8069-series line interface unit (LIU).

Use of a memory-mapped microprocessor bus interface minimizes the host MPU real-time requirement. Direct MPU access to T1 control and monitor functions in the BtT9170 register map allows software access without complicated serial message protocols.

BtT9170 Functional System Interface



Distinguishing Features

- Intelligent Single-Device DS1 T-Carrier Transceiver (1.544 MHz)
- Compatible with ANSI Standard T1.403 Covering Facility Data Link Operations:
  - Priority Codeword Handling
  - Near-End and Far-End Performance Monitoring
  - Extracted Link Data Handling
- Signalling Register Bank
- Independent Transmit and Receive Per-Channel Conditioning
  - Automatic Conditioning of Receive Trunk and Signalling During CGA
  - Unconditional Replacement of Transmit or Receive Trunk and Signalling
- Dedicated per-channel control register for each time slot
- 80x88-Compatible Parallel Microprocessor Bus Interface
  - 8-Bit Address/Data Bus for Accessing Control and Status Information
- Separate Serial Interfaces for DS1 Transmit & Receive Data
- Microprocessor-Accessible Registers
  - 16 Control and Monitor
  - 14 Facility Data Link
  - 24 Per-Channel Control
  - 12 Received Signalling
- User-Maskable Interrupt Request Generated on Specified Alarm and Error Conditions
- Independent Transmit and Receive Functions, Each With a Separate Timebase
- Off-line Framer Flywheel Timebase Option
- Implements T1 Formats With and Without Signalling
  - ESF: 24 Frames/Multiframe
  - SF: 12 Frames/Multiframe
  - N: 4 Frames/Multiframe

- continued

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Distinguishing Features *(continued)*

- Zero-Suppression Modes
  - Bit-7 Stuffing
  - B8ZS Line Coding
  - Transparent
- Meets CCITT G.733 (1.544 MHz) and Applicable Sections of G.703
- Compatible with AT&T Technical Advisories on ESF and Clear-Channel Operation With B8ZS
- Alarm Generation and Detection
- Remote and Locally Controlled Payload Loopback
- Pin-For-Pin Compatible with BtP9170, Intelligent El Framer
- Direct Interface and Control of the Bt8069-series Line Interface Unit (LIU)
- Direct Interface to the Bt8071A 32-Channel HDLC Controller
- Packages:
  - 40-pin Plastic (DIP)
  - 44-pin Plastic (PLCC) Package
- Operates From a Single +5 Vdc ±5% Power Supply
- CMOS/TTL-Compatible Inputs and Outputs
- Low-Power CMOS Technology

Ordering Information

Model Number	Package	Ambient Temperature
BtT9170KP	40-pin Plastic DIP	0° C to 70° C (Commercial)
BtT9170KPJ	44-pin Plastic Leaded Chip Carrier (PLCC)	0° C to 70° C (Commercial)
Consult factory about extended temperature availability.		

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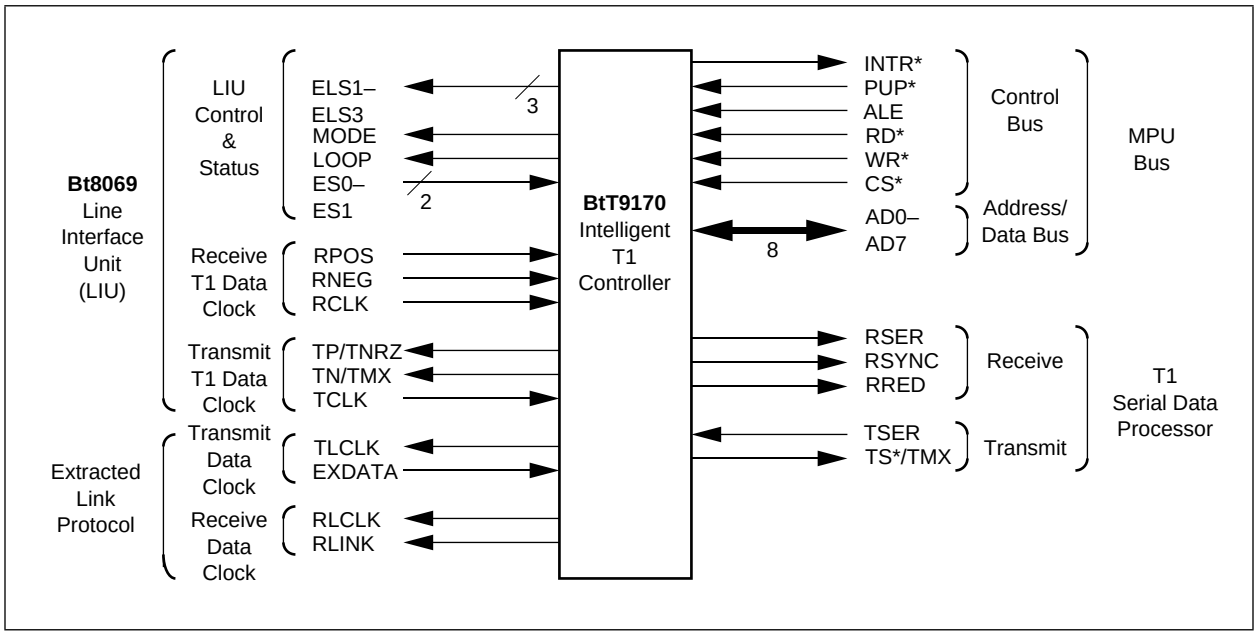
Product Description

Microprocessor Interface

The BtT9170 provides the intelligent functions of T1 mode control, signalling control, error and alarm reporting, and handling of the facility data link through internal registers via the 8-bit parallel, memory-mapped MPU interface. The BtT9170 has 66 registers to provide intelligent interface control. The BtT9170 also provides a maskable interrupt-request output for handling of alarm and error conditions. The BtT9170 functional interface signals are shown in Figure 1.

Figure 1. BtT9170 Functional Interface Signals



Facility Data Link

Control over the ESF Facility Data Link (FDL) is managed by the BtT9170, which adheres to ANSI standard T1.403-1989 and emerging standards for primary rate access. The FDL is user selectable as either a 4 kbps or 2 kbps channel. The BtT9170 supports priority codeword handling, automatic performance monitoring and reporting, and user-supplied link data handling. The ESF data link may be used for user-supplied extracted-link protocol transmission when it is not being used for yellow alarms, priority codewords, or performance messages; four pins are provided for this purpose.

Per-Channel Control

Twenty-four internal registers provide individual control of each T1 channel. Users can control trunk and signalling conditioning on a per-channel basis. Robbed bit signalling (2-, 4-, or 16-code “ABCD” signalling) or non-signalling can be implemented on a per-channel basis. Trunk conditioning substitutions may be made on a per-channel basis to include IDLE (both user-specified and standard IDLE codes), BUSY, VACANT, and digital milliwatt codes.

Transceiver and Off-line Framer (Flywheel Timebase)

The BtT9170 has independent transmit and receive sections. The receiver incorporates a robust framing algorithm, which prevents false synchronization on patterns that mimic the framing bits in ESF mode. Transceiver functions also include zero suppression, alarm generation and detection, and loopback modes.

An off-line framer mode provides continuity of synchronized functions during frame searches. In this mode, the receiver output signals are derived from the off-line framer, which also provides timing for receive trunk and signalling conditioning.

Line Interface Unit Control

The BtT9170 provides dedicated I/O pins that allow direct MPU software access to a Bt8069-series LIU. The BtT9170 T1 operating mode is selected by configuring the framing mode and the line code.

Framing Modes

Superframe Format (SF) Mode

The SF mode implements the standard D4 PCM format at 1.544 Mbps with 12 frames per multiframe.

Extended Superframe Format (ESF)

The ESF mode implements the standard D5 PCM format at 1.544 Mbps with 24 frames per multiframe. This mode is sometimes referred to as ESF, Fe, or D5.

The transmitter generates the framing pattern sequence (FPS), computes the cyclic redundancy check (CRC) checksum, and formats the facility data link (FDL) bits. The receiver recovers the FPS to establish framing, checks the CRC against the data, and provides a facility data link control (FDLC) report via the far-end monitor registers. “ABCD” robbed bit signalling is controlled via the per-channel control registers and stored in the received signalling registers.

Non-Signalling Superframe Format (N) Mode

The N mode implements the standard D4 PCM format at 1.544 Mbps with four frames per multiframe, without signalling.

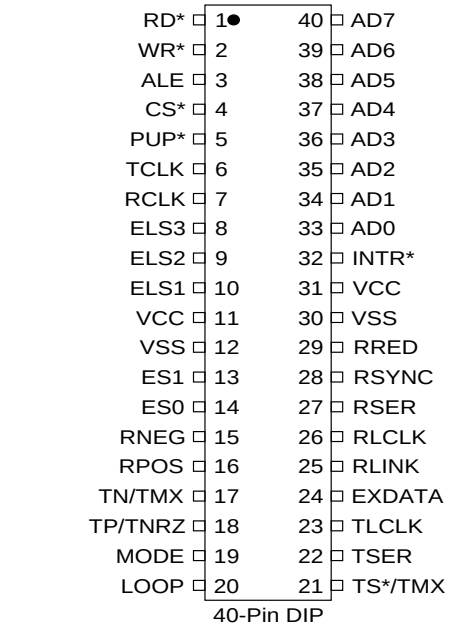
Line Codes/Zero Suppression

To satisfy the ones-density requirement, either B8ZS line coding or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

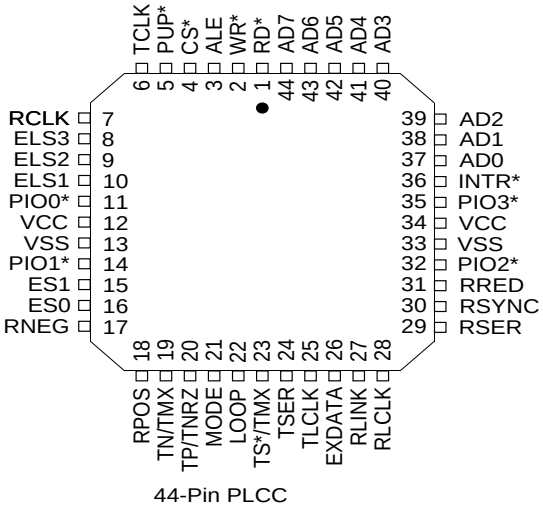
Pin Information

The BtT9170 pin assignments are shown in Figure 2 and are listed in Table 1. The BtT9170 hardware interface signals are defined in Table 2.

Figure 2. BtT9170 Pin Assignments



40-Pin DIP



44-Pin PLCC

Note: "*" denotes active low signal. All BtT9170 pin assignments are identical to BtP9170 assignments.

Table 1. BtT9170 Pin Assignments *(1 of 2)*

Pin No. (40-Pin DIP)	Pin No. (44-Pin PLCC)	Pin Label	I/O
1	1	RD*	I
2	2	WR*	I
3	3	ALE	I
4	4	CS*	I
5	5	PUP*	I
6	6	TCLK	I
7	7	RCLK	I
8	8	ELS3	O
9	9	ESL2	O
10	10	ELS1	O
–	11	PIO0*	I/O
11	12	VCC	PWR
12	13	VSS	GND
–	14	PIO1*	I/O
13	15	ES1	I
14	16	ES0	I
15	17	RNEG	I
16	18	RPOS	I
17	19	TN/TMX	O
18	20	TP/TNRZ	O
19	21	MODE	O
20	22	LOOP	O
21	23	TS*/TMX	I/O
22	24	TSER	I
23	25	TLCLK	O
24	26	EXDATA	I
25	27	RLINK	O
26	28	RLCLK	O
27	29	RSER	O
28	30	RSYNC	O
29	31	RRED	O
–	32	PIO2*	I/O
30	33	VSS	GND

Table 1. BtT9170 Pin Assignments *(2 of 2)*

Pin No. (40-Pin DIP)	Pin No. (44-Pin PLCC)	Pin Label	I/O
31	34	VCC	PWR
–	35	PIO3*	I/O
32	36	INTR*	O
33	37	AD0	I/O
34	38	AD1	I/O
35	39	AD2	I/O
36	40	AD3	I/O
37	41	AD4	I/O
38	42	AD5	I/O
39	43	AD6	I/O
40	44	AD7	I/O

Table 2. BtT9170 Pin Definitions *(1 of 4)*

	Pin Label	Signal Names	I/O	Description
Microprocessor Interface Pins	AD0–AD7	Address/Data Bus	I/O	Multiplexed address and data pins (AD0-AD7) are used to specify the address of the BtT9170 internal register accessed during an MPU read or write cycle, and to transfer data between the MPU and the BtT9170. The BtT9170 will service only register addresses 00H to 7FH; addresses outside this range are ignored.
	PUP*	Power-Up	I	This active low input asynchronously three-states all BtT9170 outputs. Outputs assume their normal impedance state within 600 ns after PUP* returns high. PUP* is also sampled by the rising edge of TCLK and may be applied synchronously to initialize all BtT9170 internal registers. To properly initialize the registers, PUP* must be held high for at least 20 TCLK cycles before going low. Initialization is completed within 128 TCLK cycles after PUP* transitions from high to low.
	RD*	Read	I	This active low control input is strobed low during the MPU read cycle. During the MPU read cycle, data from the addressed BtT9170 internal register is output to the MPU data lines. Read data outputs reflect the content of the addressed register after a given period of time has elapsed (Refer to tRLDV timing parameter #10a, Table 7). An additional 1/2 TCLK cycle must elapse (Refer to tRLDL timing parameter #10b, Table 7) before read data outputs become latched and are guaranteed not to change. MPU read cycles using long read strobes (RD* asserted for a period > tRLDL) can guarantee data bus setup/hold times. Short MPU read strobes (RD* asserted for a period > tRLDV) cannot guarantee data bus setup/hold times, but can use faster read cycles without compromising system performance. Reference the software guidelines provided in the MPU interface section of this datasheet for an explanation of the necessary procedures.
	WR*	Write	I	This active low control input is strobed low during the MPU write cycle. During the write cycle, data from the MPU data lines is written into the addressed BtT9170 internal register.
	ALE	Address Latch Enable	I	This active high control input enables the BtT9170 to capture the address from the multiplexed address/data bus.
	CS*	Chip Select	I	This active low control input is low during MPU bus access to the BtT9170.
	INTR*	Interrupt Request	O	This open-drain output is used to interrupt the MPU when any one of the Interrupt Cause Register (ICR) bits and its respective Interrupt Enable Register (IER) bits are set. The open-drain output allows the interrupt request output line from several devices to connect to the common MPU interrupt request line. This output requires an external pull-up resistor to VCC (recommended pull-up resistance is 4.7K Ω).

Table 2. BtT9170 Pin Definitions *(2 of 4)*

	Pin Label	Signal Names	I/O	Description
Line Interface Unit Interface Pins	ELS3–ELS1	Equalization Line Select	O	Outputs that control the cable-length equalization for the attached Bt8069-series LIU. Line equalization is selected through register CR4. **ELS3 ELS2 ELS1 Cable Length** 0 0 0 0–110 ft 0 0 1 110–220 ft 0 1 0 220–330 ft 0 1 1 330–440 ft 1 0 0 440–550 ft 1 0 1 550–660 ft
	ES1, ES0	Error Status	I	Error status inputs from the Bt8069-series LIU. **ES1 ES0 Indication** 0 0 AIS detected 0 1 Elastic Buffer limit 1 0 Loss of signal 1 1 Normal Operation
	LOOP	Loop Select	O	Loop Select.
	MODE	Mode Select	O	Loop and mode outputs determine the Bt8069-series LIU mode of operation. (Refer to the specific LIU datasheet for LOOP and MODE definitions.)
Extracted Link Pins	TLCLK	Transmit Link Clock	O	TLCLK is an output used to clock EXDATA. Either edge of TLCLK may be used to make EXDATA available to the BtT9170.
	EXDATA	Extracted Link Data	I	The EXDATA input is a high-impedance pin that provides the extracted link protocol bit stream data. EXDATA is sampled on the rising edge of TCLK during TSER FDL or Fs bit while TLCLK is low.
	RLCLK	Received Link Clock	O	RLCLK is an output that systems may use to sample the RLINK bit stream. Either the rising or falling edge, or the high level of RLCLK may be used to store the RLINK data.
	RLINK	Received Link Data	O	RLINK is an output that provides the link data. The data is stable one RCLK period before the rising edge of RLCLK and is centered around the falling edge of RLCLK.

Table 2. BtT9170 Pin Definitions *(3 of 4)*

	Pin Label	Signal Names	I/O	Description
Transmitter Pins	TCLK	Transmit Clock	I	TCLK is the transmitter clock input and must be unconditionally present. TCLK must be in the range of 100 kHz–3.1 MHz and will normally be 1.544 MHz. All transmit inputs are sampled by the rising edge of TCLK, and all transmit output transitions are caused by the rising edge of TCLK.
	TSER	Transmit Serial Data	I	TSER is the serial input for the transmitted channel data and optionally the transmitted signalling data. Each bit is sampled on the rising edge of TCLK.
	TN/TMX	Transmit Negative/Transmit Maximum	O	A bimodal pin whose function is controlled by the ETRNZ bit in register CR5. After power-up or software reset, this pin defaults to “transmit negative.”
		Transmit Negative (TN)		The transmit output bit stream encoded for alternate mark inversion. The output sequences normally with a one on TP followed by a one on TN, followed by a one on TP, and so on. This sequence is deliberately broken when a B8ZS substitution takes place.
		Transmit Maximum (TMX)		This output pulses high for one bit time and is coincident with the sampling of the last serial bit of a multiframe.
	TP/TNRZ	Transmit Positive/Transmit Non-Return to Zero	O	A bimodal output pin whose function is controlled by the ETRNZ bit in register CR5. After power-up or software reset, this pin defaults to “transmit positive.”
		Transmit Positive (TP)		The transmit output bit stream encoded for alternate mark inversion. This output complements the Transmit Negative (TN) pin as described above.
		Transmit Non-Return to Zero (TNRZ)		TNRZ is the unipolar output for transmitted data. TNRZ includes the results of bit-7 stuffing (if enabled) but does not include B8ZS encoding.
	TS*/TMX	Transmit Sync/Transmit Maximum	I/O	A bidirectional pin whose function is controlled by the MASTER bit in register CR5. After power-up or software reset, this pin defaults to “transmit sync” input.
		Transmit Sync (TS*)		A low on this input synchronously resets the transmit timebase. Following the rising edge of transmit sync, the first bit of a multiframe will be sampled by the BtT9170.
		Transmit Maximum (TMX)		This output pulses high for one bit time and is coincident with the sampling of the last serial bit of a multiframe.

Table 2. BtT9170 Pin Definitions *(4 of 4)*

	Pin Label	Signal Names	I/O	Description
Receiver Pins	RCLK	Receive Clock	I	RCLK is the receive clock input and must be present for normal operation. RCLK must be in the range of 100 kHz–3.1 MHz and will normally be 1.544 MHz. All receive inputs are sampled by the rising edge of RCLK, and all receive output transitions are caused by the rising edge of RCLK.
	RPOS, RNEG	Receive Positive, Receive Negative	I	RPOS and RNEG are the (alternate unipolar) inputs for the received data recovered from the positive and negative AMI line pulses. RPOS and RNEG may be of either NRZ or RZ form. When receiving a single unipolar data stream, the data is connected to both RPOS and RNEG simultaneously.
	RSYNC	Receive Synchronization	O	The RSYNC output pin provides a synchronization signal whose nature depends on the receive master state, off-line framer selection (controlled by OLFRE bit in register CR1), and period mode selection (controlled by PER bit in register CR2). RSYNC will pulse at the first bit of each multiframe. From initialized condition, the first RSYNC pulse appears only after the receiver attains synchronization.
	RSER	Receive Serial Data	O	RSER is the output that represents the received serial data bit stream. This bit stream includes all received bit positions and any B8ZS corrections. The user can substitute RSER with other predefined data by programming the various internal registers.
	RRED	Receive Red Alarm	O	The RRED output pin indicates the condition of the receive synchronizer. The function of this pin is controlled by the REDMD bit in register CR1. When REDMD is reset to a zero, the RRED output will be high when the BtT9170 is not multiframe aligned; RRED output will be low when the BtT9170 is both frame and multiframe aligned. If REDMD is set to a one, RRED will be high when the BtT9170 is not frame aligned and low if frame aligned. RRED transitions one bit time after the F-bit is available at RSER.
Power and Ground Pins	Vcc	+5 Vdc Power	I	+5 Vdc ±5% power.
	Vss	Ground	I	Power and signal ground.

Functional Description

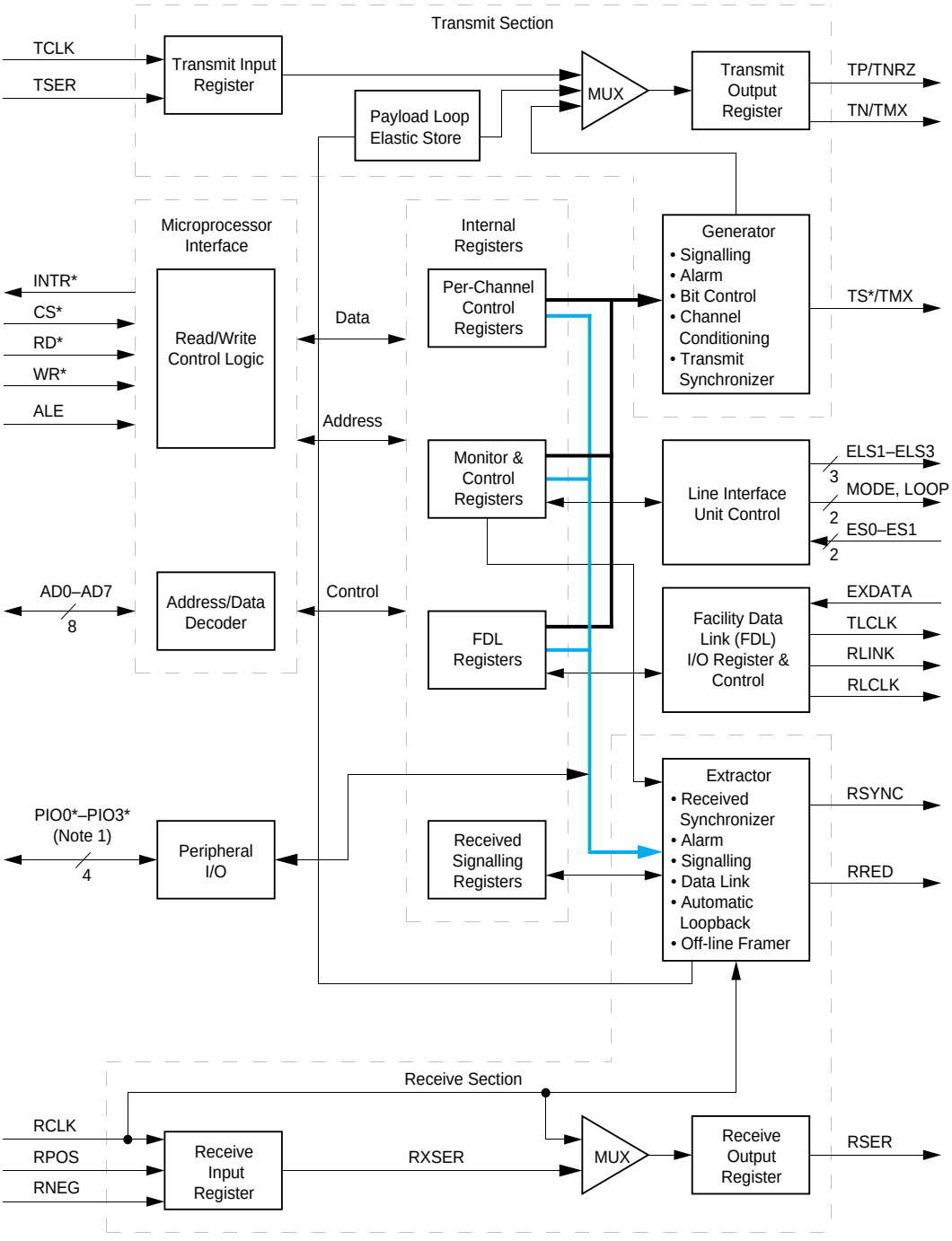
Introduction

The BtT9170 consists of the following major sections:

1. Transmit Section
2. Receive Section
3. Facility Data Link Section
4. Line Interface Unit Control Section
5. Peripheral I/O Section
6. Microprocessor Interface Section

The major signal interfaces to these sections are shown in Figure 3.

Figure 3. BtT9170 Detailed Block Diagram



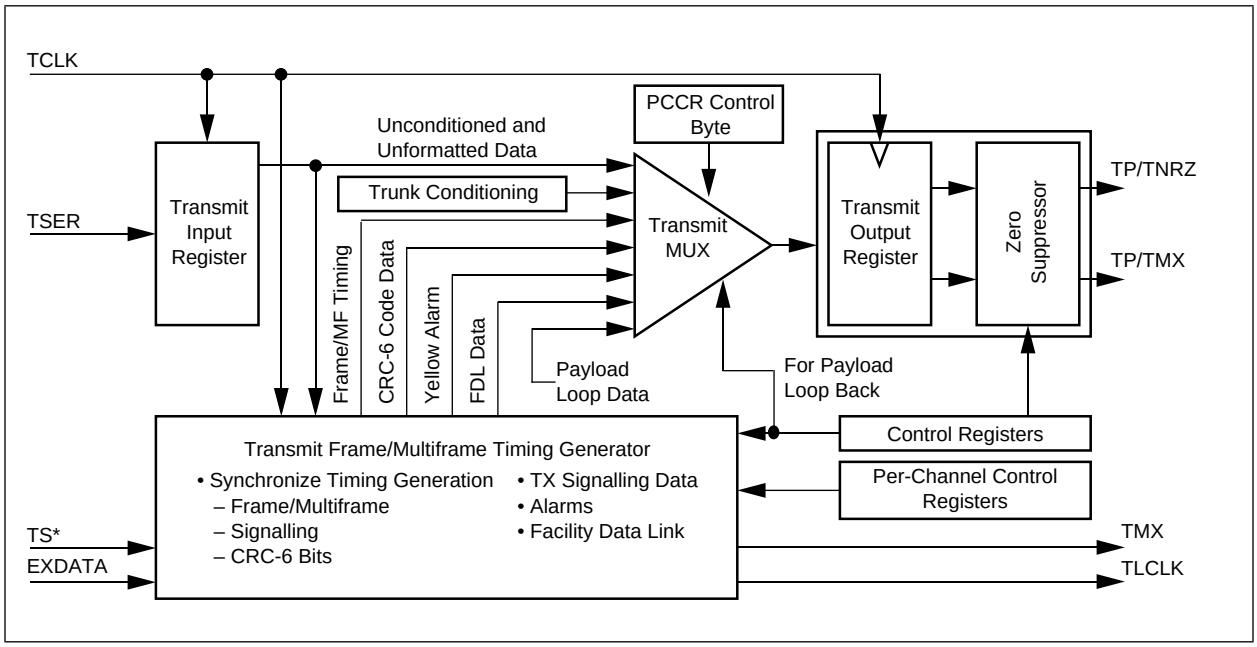
Note: PIO pins available only on 44-pin package.

Transmit Section

The BtT9170 transmit section provides the transmitter synchronization, frame/multiframe data formatting, transmit signalling, and yellow-alarm transmission functions. In addition, the transmit section also converts the transmitted data to paired alternate unipolar in support of AMI line codes. The transmit section is composed of the following subsections (Figure 4):

1. Transmit Input Register
2. Transmit Frame/Multiframe Timing Generator
3. Transmit Multiplexer
4. Transmit Output Register/Zero Suppressor

Figure 4. Transmit Section Functional Block Diagram



Transmit Input Register

The serial T1 data to be transmitted enters the BtT9170 at the TSER input pin. Data is clocked into the transmit input register on the rising edge of the transmit clock (TCLK). TCLK has the nominal frequency of 1.544 MHz and is provided by the system. The unconditioned and unformatted (raw) data is sent to both the transmit multiplexer and the transmit frame/multiframe timing generator.

Transmit Frame/Multiframe Timing Generator

The transmit frame/multiframe timing generator provides both data pattern and timing for frame and multiframe alignment, CRC-6 bits, signalling, facility data link, and yellow alarm. These bits are sent to the transmit multiplexer, where they are added to the raw data stream to format the raw data into the appropriate T1 format according to the selected mode of operation.

Frame and multiframe counters in the transmit frame/multiframe timing generator generate the timing and framing bits. The required F-bit (Fs, Ft, or FPS) can be generated internally or be supplied externally via TSER and EXDATA. The frame and multiframe counter may be reset to the first bit of the multiframe when the Transmit Synchronize (TS*) input is pulsed low.

This section also generates the Transmit Max (TMX) output, which pulses high for one bit time during the last serial bit of a multiframe, based on the timebase set by the TS* input, or the arbitrary timebase set after power-up.

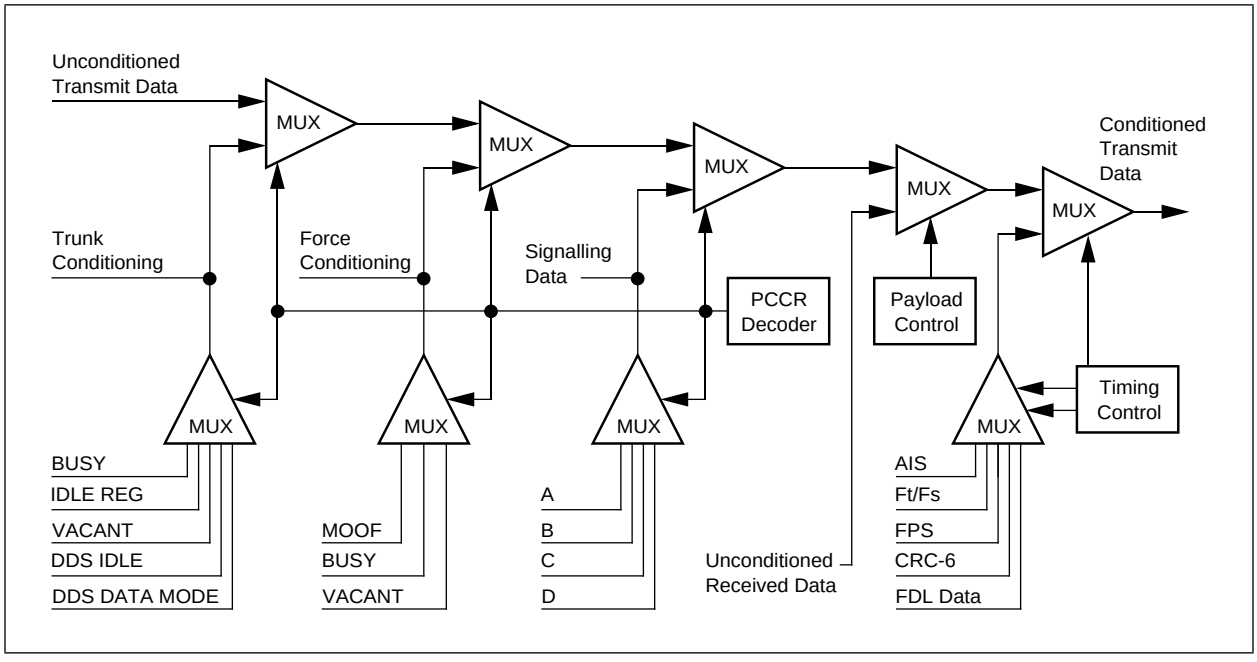
Transmit Multiplexer

The transmit multiplexer inserts the appropriate F-bit into the transmit data stream. If “payload loop-back” is active, the raw received data replaces the raw transmit data and becomes the transmit output. The output goes to the transmit output register/zero suppressor and is subsequently transmitted to the LIU in the form of a paired unipolar signal, ready for conversion to a true AMI signal.

The transmit multiplexer consists of five submultiplexers (see Figure 5):

1. Trunk Conditioning Multiplexer
2. FORCE Conditioning Multiplexer
3. Signalling Multiplexer
4. Payload Control Multiplexer
5. Timing Control Multiplexer

Figure 5. Transmit Multiplexer Data Flow



Trunk Conditioning Multiplexer

The first multiplexer encountered by the unconditioned raw transmit serial T1 data is the trunk conditioning multiplexer. The trunk conditioning multiplexer allows the replacement of the unconditioned raw T1 data stream in any given channel on a per-channel basis. The type of channel conditioning is determined by the control byte in the specific channel's per-channel control register (PCCR). Trunk conditioning allows the replacement of channel data with either BUSY code (0111 1111), VACANT code (1111 1111), custom IDLE code as specified in Idle Register (IR), DDS IDLE code (1111 1110), or DDS DATA mode (XXXX XXX1; where X indicates that the channel data remains unchanged). The specific channel's PCCR can also be set up to bypass the channel conditioning and allow the channel data to pass without trunk conditioning.

FORCE Conditioning Multiplexer

The FORCE conditioning multiplexer expands the available trunk-conditioning options. The type of FORCE conditioning is determined by the control byte in the specific channel's PCCR. FORCE conditioning allows the replacement of channel data with either MOOF (Mux-Out-Of-Frame), BUSY (0111111S), or VACANT (11111111) codes. The PCCR control byte structure prevents the enabling of both the TRUNK and FORCE conditioning multiplexers.

Signalling Multiplexer

The transmit serial T1 data stream then enters the signalling multiplexer. The signalling multiplexer allows the BtT9170 to implement robbed-bit signalling in any given channel on a per-channel basis. Robbed-bit signalling substitution is enabled by the PQX bit combinations in the individual channel's PCCR. The type of robbed-bit signalling selected for any given channel is determined by control code bits E, D, C, B, A in the specific channel's PCCR.

In SF mode, control code bits E, D, C, B, A can select either no signalling, 2-code signalling (substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the A-bit of the PCCR), or 4-code signalling (substituting the LSB of channel data in frames 6 with the A-bit and the LSB of channel data in frame 12 with the B-bit of the specific channel's PCCR). If 16-code signalling is selected, the BtT9170 uses only the A-bit and the B-bit information in the SF mode.

In ESF mode, control code bits E, D, C, B, A can select no signalling, 2-code signalling (substituting the LSB of the channel data in frames 6, 12, 18, and 24 with the content of the A-bit of the PCCR), 4-code signalling (substituting the LSB of the channel data in frames 6 and 18 with the content of A-bit of the PCCR while the LSB of the channel data in frames 12 and 24 are substituted with the content of B-bit of the PCCR), or 16-code signalling (which allows the LSB of the channel data in frames 6, 12, 18, and 24 to be substituted with the contents of A-, B-, C-, and D-bits of the PCCR, respectively).

In N mode, no robbed-bit signalling is selected, and the transmit serial data stream remains unchanged.

Payload Control Multiplexer

The payload loopback feature allows the BtT9170 to internally loopback the unconditioned received raw data. When loopback is selected (PLOOP = 1 in CR5), the received serial data (excluding the framing bits) becomes the transmit serial data. When loopback is not selected, the serial T1 data stream output from the signalling multiplexer is passed directly to the timing control multiplexer.

In ESF mode, when payload loop automatic is selected (PLAUTO = 1 in CR5), the loopback can be controlled from the far-end via the priority codeword in the facility data link.

Timing Control Multiplexer

The timing control multiplexer injects the appropriate framing bits into the serial T1 data stream for the selected operating mode. The data is then sent to the transmit output register/zero suppressor.

In SF mode, the timing control multiplexer inserts Ft and Fs bits into the serial T1 data stream.

In ESF mode, the timing control multiplexer takes data generated by the transmit frame/multiframe generator and inserts the FPS, CRC-6, and FDL bits.

In N mode, the timing control multiplexer inserts only the Ft bit pattern into the serial T1 data stream. The Fs bit may be in the TSER input data stream or in the EXDATA input.

The BtT9170 also allows the user to bypass the internally generated F-bit, FDL, and CRC-6 bit patterns. Bypassing the internally generated timing bits requires that the data stream entering the TSER input contain all the bypassed bits. Setting FBYPAS = 1 in CR5 allows F-bits to be provided via the TSER input. Bypassing the internally generated FDL bits requires setting LBYPAS = 1 in CR5, while setting CBYPAS = 1 in CR5 allows bypass of the internally generated CRC bits.

The timing control multiplexer also controls the transmission of an alarm indication signal (AIS). When SAIS = 1 in CR4, AIS is transmitted, which forces the timing control multiplexer to transmit unframed all-ones data.

Transmit Output Register

The output of the transmit multiplexer, with the appropriate bits inserted into the original unconditioned data stream, is clocked out of the transmit section on the rising edge of TCLK. The data is output to the TP/TNRZ and TN/TMX dual-function pins. The ETNRZ bit in CR5 selects the function of pins. When ETNRZ = 0, the pins function as alternate mark inverted (AMI) output data on TP and TN. When ETNRZ = 1, the pins function as TNRZ and TMX outputs.

When AMI output is selected, the transmit output register clocks the data in and converts it to the equivalent alternate unipolar-pair output on TP and TN. These outputs are then subjected to zero-suppression encoding as selected by the LCM1 and LCM0 bits in CR0. The BtT9170 encodes data with B8ZS line codes or Bit-7 stuffing, or performs no encoding (transparent mode). After power-up or software reset, the BtT9170 defaults to B8ZS.

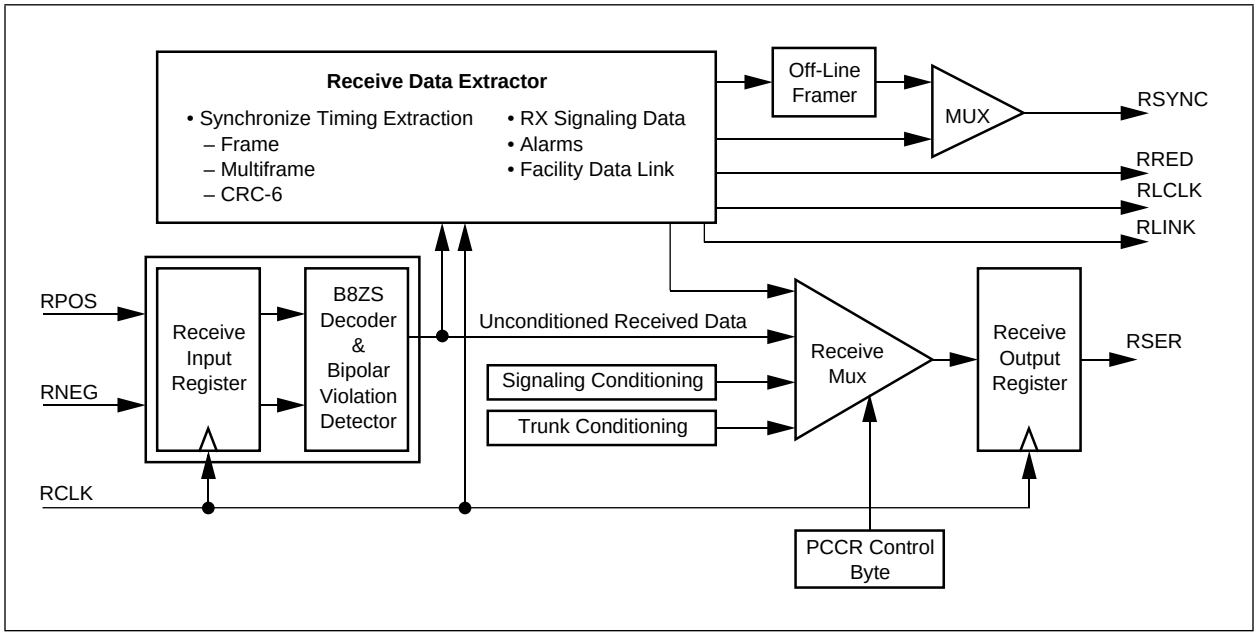
In TNRZ output mode, bit-7 stuffing is the only zero-suppression coding available.

Receive Section

The BtT9170 receive section provides the synchronization, signalling, and alarm indication functions. The receiver is composed of the following subsections (see Figure 6):

1. Receive Input Register/B8ZS Decoder and Bipolar Violation Detector
2. Receive Extractor
3. Receive Multiplexer
4. Receive Output Register
5. Off-line Framer

Figure 6. Receive Section Functional Block Diagram



Receive Input Register/B8ZS Decoder and Bipolar Violation Detector

T1 data from the LIU enters the BtT9170 on the RPOS and RNEG pins. This paired unipolar received data is clocked into the receive input register by the rising edge of RCLK and is sent to the receive multiplexer and the receive extractor. Incoming data is first decoded for B8ZS code (if enabled). There is no algorithm to decode Bit-7 stuffing. The data is then checked for bipolar violations. Bipolar violations are counted and reported to the MPU via the near-end monitor registers.

Receive Extractor

The receive extractor extracts specific information from the bit stream of the receiver input register. The extracted information is placed into the appropriate internal registers for the MPU to access. Receiver timing synchronization from the incoming data is also extracted. Receiver synchronization is handled by a multi-stage process which singles out the correct synchronization lock point. Other information extracted is not valid unless the receiver has achieved valid synchronization.

Upon achieving valid synchronization, other extracted information is valid for the MPU to use. This information includes received signalling, FDL, and remote alarms. Received signalling is stored into the received signalling registers (RSR1–RSR15). FDL information is placed in the appropriate registers (FEPR1–FEPR8 and RPCR) and routed to the RLINK output. Alarm conditions are reported to the MPU via the monitor registers (MR0–MR2), and error counts are stored in the appropriate near-end monitor registers (NEMR1–NEMR6).

Receiver Synchronization

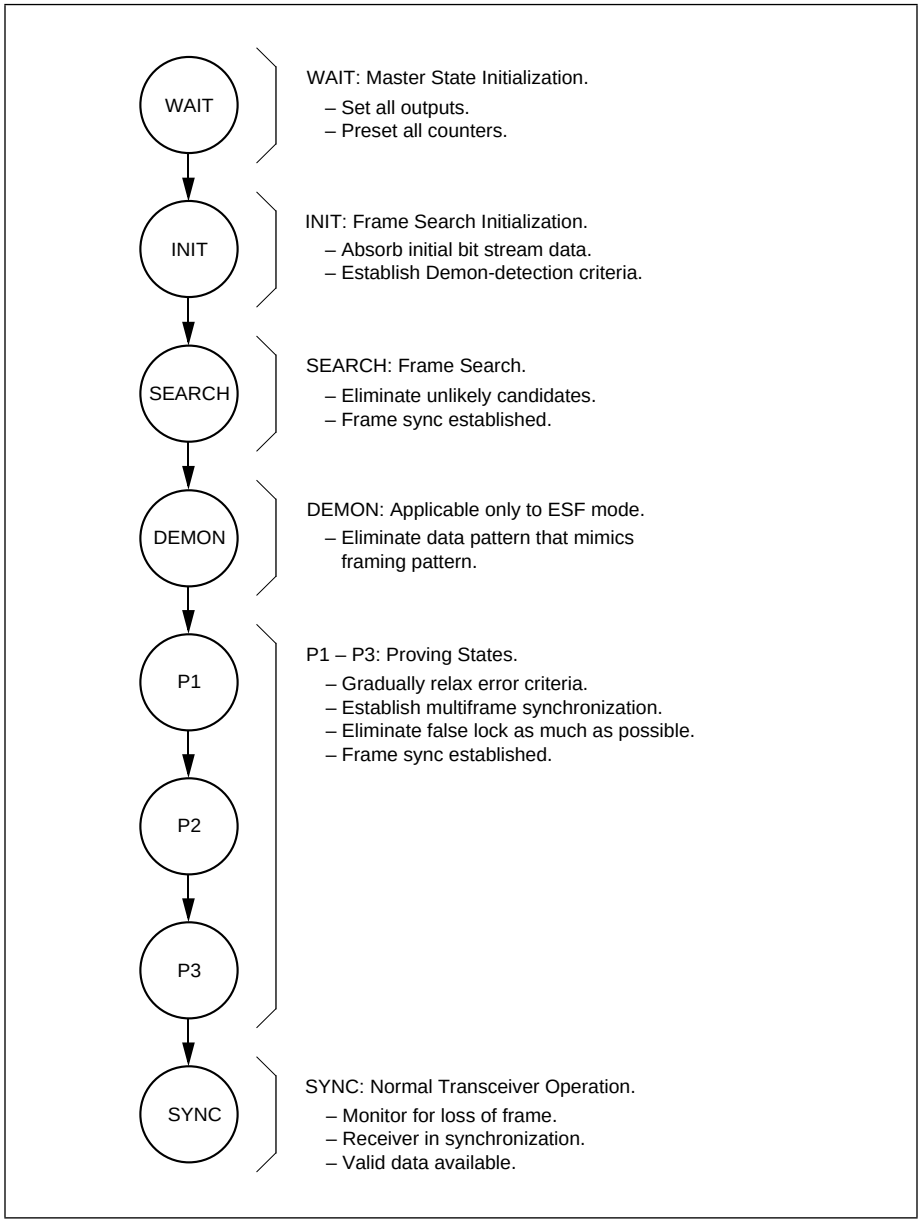
After power-up (PUP*), software reset (RESET = 1 in CR2), or a receiver frame-synchronization restart (RFSR = 1 in CR2), or when a framing-error condition is detected, the receiver begins to search for candidates for frame and multiframe alignment. In ESF mode, the receiver does not achieve full synchronization until the data has gone through a qualifying period. In the qualifying period, CRC-6 block checks are used to ensure that the chosen synchronizing candidate is valid. This qualifying period ensures that the BtT9170 achieves correct frame alignment and synchronization even in the presence of data patterns that mimic the framing patterns. (Intentional framing mimics may prevent frame synchronization.) The general synchronization flow is illustrated in Figure 7.

When synchronization is achieved, the receiver monitors alignment signals for errors. A red alarm is generated if frame alignment is lost. The criteria for loss of frame alignment in all modes is two out of five errors in the Ft or FPS bit pattern.

The receiver can be forced to restart a synchronization search (RFSR = 1 in CR2) or to prevent a resynchronization search when synchronization has been achieved (SL = 1 in CR1).

With framed random data inputs, synchronization is achieved within 10 ms of the initialization of a framing search.

Figure 7. General Synchronization Flow Chart



Signalling Extraction

When synchronization is achieved, signalling bits (also known as robbed-bit signalling) can be extracted from the incoming data. Signalling bits are then stored into the appropriate internal registers (RSR1–RSR15). If frame alignment is subsequently lost, the receiver stops updating the received signalling registers.

In the SF mode, the A- and B-bit signalling is available to the MPU by way of the received signalling subarray A (registers RSR1–RSR3) and subarray B (registers RSR5–RSR7), respectively. Whenever two-code signalling is selected, the signalling data contained in signalling channels A and B are both placed in subarray A. An interrupt request may also be generated at the end of a multiframe in which a change of signalling data has occurred.

In the ESF mode, the A-, B-, C-, and D-bit signalling is available to the MPU by way of the received signalling subarray A (registers RSR1–RSR3), subarray B (registers RSR5–RSR7), subarray C (registers RSR9–RSR11), and subarray D (registers RSR13–RSR15), respectively. Whenever 16-code signalling is selected, the data from each signalling channel is placed into its respective subarray. Whenever four-code signalling is selected, the A signalling data contained in signalling channels A and C is placed in subarray A; and the signalling data contained in signalling channels B and D is placed in subarray B. For two-code signalling, the signalling data contained in signalling channels A, B, C, and D is placed in subarray A. An interrupt request may be generated at the end of a multiframe in which a change of signalling data has occurred. In the N mode, no robbed-bit signalling is used.

Facility Data Link Extractor

The facility data link extractor function is available only in the ESF mode, in which the F-bit structure is shared between the framing, CRC-6, and the facility data link. The received FDL information is made available to the MPU via the receive priority codeword register (RPCR) or, in the form of an error report, through the far-end performance message registers (FEPR1–FEPR8). In addition, FDL data is extracted and output in serial form on the RLINK pin where it can be sampled at the falling edge of RLCLK. The FDL can be selected to operate at 4 kbps or 2 kbps.

FEPR1–FEPR8 are updated whenever a complete and valid report is received. If the FDL is not carrying higher priority messages, such as yellow alarm or priority codewords, a complete report is expected every second. Figure 8 illustrates the performance report message structure specified by ANSI standard T1.403-1989.

Figure 8. Performance Report Message Structure

Octet No.	LSB							MSB
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS (Most Significant Byte)							
14	FCS (Least Significant Byte)							

Notes: 1. The 1-second report consists of octets 5–12.
2. R, U1, and U2 are reserved for future standardization and should be set to 0 (see Control Register CR3).

Alarm Condition Extractor

The alarm condition extractor examines the incoming T1 data for alarm conditions. When an alarm condition is detected, corresponding bits are set in the monitor registers (MR0–MR2). The possible alarms are:

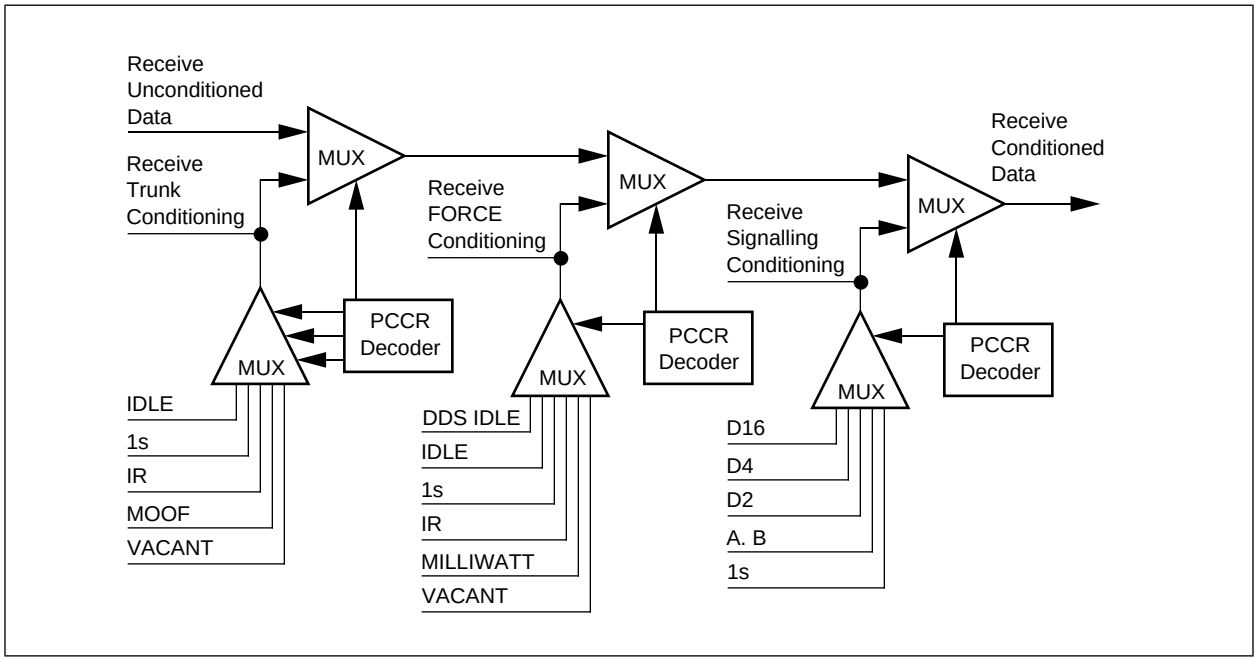
Alarm	Framing Mode	Description
RRED	All	Red alarm loss of frame alignment
RYEL	All	Yellow alarm (transmitted by the far end)
AISDET	All	All-ones condition detected
FERR	All	Framing error(s)
ALTF	N, SF	1 of 5 Ft alternation error detected (possibly caused by two frame controlled slip)
LOST	All	Lost carrier
BPVS	All	Bipolar violation(s)
COFA	All	Change of frame alignment
CRCS	ESF	CRC-6 block error(s)

Receive Multiplexer

Internally generated data can be substituted for the actual received data. The data substitution on individual channels is controlled by the MPU through the per-channel control registers (PCCR1–PCCR24), which allow the received data to be replaced on a channel-by-channel basis. The actual substitution of received data is accomplished by the receive multiplexer as controlled by red alarm and control registers.

The data entering the receive multiplexer arrives from the receive input register/B8ZS decoder as an unconditioned serial data stream (see Figure 9). The data goes through three levels of multiplexers prior to being sent to the receive output register. The three multiplexers perform receive trunk conditioning, receive FORCE conditioning, receive signaling conditioning, and receive output register.

Figure 9. Receive Multiplexer Block Diagram



Receive Trunk Conditioning

The unconditioned received data is substituted with trunk conditioning on an individual channel basis. The per-channel trunk conditioning is established by the PQX bit combination in the selected channel's PCCR register and enabled by either the TCE bit (when RRED is active) or the CGA bit in CR2. Trunk conditioning options are:

1. **No-Trunk Conditioning**. The received data is passed through without trunk conditioning substitution.
2. **Standard Idle-Code Conditioning**. The chosen channel data is replaced with the standard idle code (0111 1111).
3. **All-Ones Conditioning**. The chosen channel data is replaced with all ones (1111 1111).
4. **MOOF Code Conditioning**. The chosen channel data is replaced with the MUX Out-Of-Frame (MOOF) code (0101 1000).
5. **Custom Idle-Code Conditioning**. The chosen channel data is replaced with the user's custom Idle code previously written from the MPU to the Idle Register (IR).

Receive FORCE Conditioning

Data from the receive trunk conditioning multiplexer can be replaced with digital milliwatt, DDS IDLE, and other codes. The substitution is enabled by the PQX bit combination set in the selected channel's PCCR, and is independent of the CGA and TCE bits in CR2. The PCCR control byte structure prevents enabling both the receive TRUNK and receive FORCE conditioning multiplexers.

Receive Signalling Conditioning

Replacement of the data from the Receive FORCE conditioning multiplexer with receive signalling conditioning is enabled by the PQX bit combination in the specific channel's PCCR if the CGA bit in CR2 is also set. Signalling conditioning options are:

1. **No-Signalling Conditioning**. The received data is passed through transparently (without replacement).
2. **Signalling Conditioning**. The actual signalling bits in the data stream are replaced with signalling bits from the default signalling register (DSR) or from the A-bit and B-bit in the selected channel's PCCR.
3. **All-Ones Conditioning**. The chosen channel's signalling bit(s) are replaced with ones.

Receive Output Register

The conditioned output data from the receive multiplexer is fed directly to the receive output register. The data is then clocked out as serial data on the RSER pin by the rising edge of RCLK. This serial data is the recovered data after B8ZS decoding (if enabled) and all appropriate conditioning of data and signalling.

Off-line Framer/RSYNC Multiplexer

The off-line framer can generate the RSYNC timing signal when the on-line framer loses synchronization. The off-line framer is a flywheel timebase, initially synchronized by the on-line framer RSYNC output. If the off-line framer is enabled (OLFRE bit = 1 in CR1), the RSYNC output is driven from the off-line framer. If the off-line framer is not enabled (OLFRE bit = 0), the RSYNC output is driven by the RSYNC signal derived from on-line framer timing.

The off-line framer also supplies the timebase (for bit, frame, and multiframe timing) for insertion of trunk and signalling conditioning into the receive bit stream (RSER). This occurs whether the off-line framer is enabled or disabled.

The RSYNC output can be selected to pulse at every frame boundary (PER bit = 1 in CR2) or at every multiframe boundary (PER bit = 0).

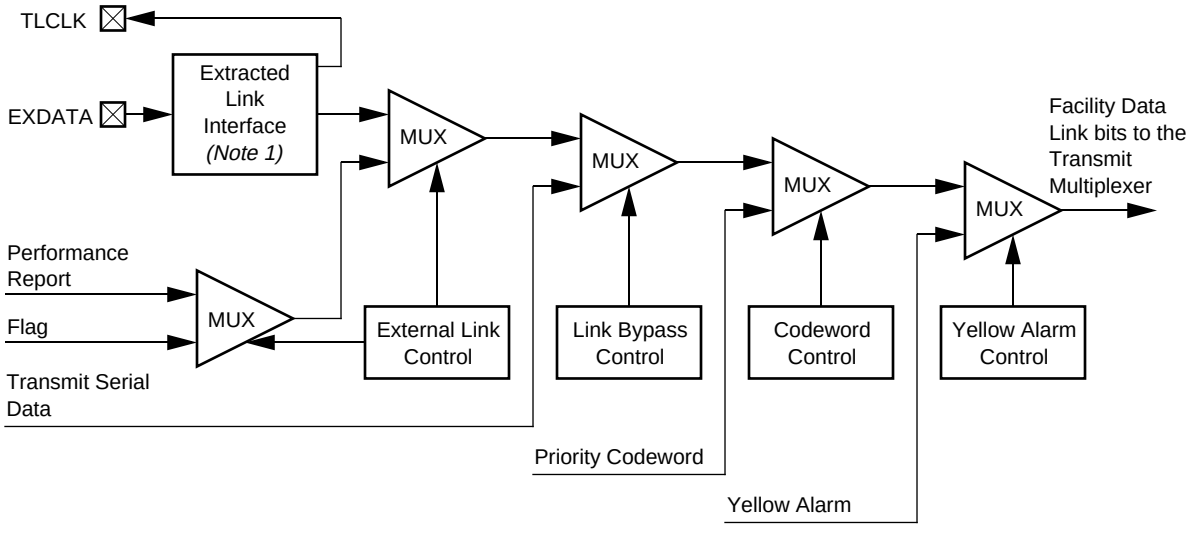
Facility Data Link Section

The facility data link is generated and decoded by the facility data link section. FDL information is available only in the ESF mode. It is generally grouped into either bit-oriented or message-oriented data. Bit-oriented data carries a higher priority than message-oriented data and always preempts message-oriented data transmission. The transmit FDL data flow is illustrated in Figure 10 and the receive FDL data flow is illustrated in Figure 11.

The incoming facility data link is extracted from the incoming bit stream and is placed into the internal registers. The FDL is also output on RLINK and can be sampled by the system.

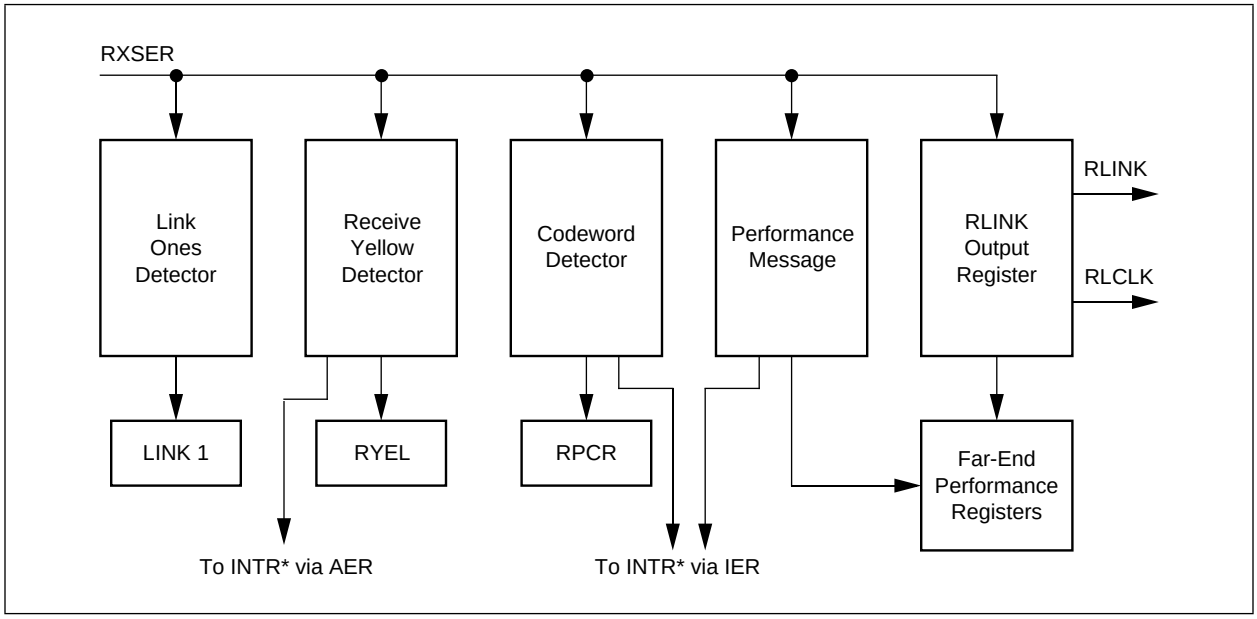
Outgoing FDL data can be entered either through the EXDATA input, TSER, or the FDL data can be generated internally. When the internal FDL message-oriented transmission is bypassed (LBYPAS bit = 1 in CR5), the FDL bits are supplied by the TSER input. If the internal FDL generator is selected (LBYPAS bit = 0 in CR5), the BtT9170 provides the message-oriented information and the bit-oriented information to the FDL multiplexer. Flags, EXDATA, and performance reports are lost when LBYPAS = 1; the link bypass function does not override yellow alarm or other bit-oriented functions.

Figure 10. Transmit FDL Data Flow



Note: No protocol checking on Extracted Link; Interface assumes protocol is handled externally.

Figure 11. Receive FDL Data Flow



Transmit FDL Data Flow

The FDL multiplexer assembles data from the transmit FDL codeword generator and performance report generator, along with EXDATA, and outputs the data to the transmit multiplexer.

Flags

When the FDL is idle, HDLC flags (0111 1110) are transmitted continuously. Transmission of idle flags is the lowest priority function in the FDL level of hierarchy.

Extracted Link

The next-higher priority FDL activity is the transmission of extracted link. The extracted-link data, in turn, has a lower priority than the transmission of the performance report. But, by setting the EXLPS bit in CR5, the extracted-link input may be made a higher priority than the performance report. If EXLPS is set in the middle of a performance-report transmission, the performance report will not be aborted. However, after the report has been completed the external link data will subsequently be able to override internally generated performance reports.

Transmit Extracted Link Protocol

The TLCLK output is a 4 kHz or 2 kHz clock as long as data is passing through EXDATA or as long as EXDATA is held high. If EXDATA goes low and the BtT9170 is in the middle of sending higher priority information, the TLCLK remains low until the FDL can process EXDATA, at which time TLCLK resumes its 4 kHz or 2 kHz operation.

If a message being sent from EXDATA has not been completed, a higher priority message (when initiated) will prevail. The connection between EXDATA and the FDL will be broken until the higher priority message completes transmission.

Performance Message Generator

At the end of each 1-second error-counting interval for the near-end monitor registers, the error counts are encoded, along with the latest MPU-provided U1, U2, R, and SL bits, and the coded information is saved from the last 3 seconds of reports. The results are sent serially on the FDL by the performance message generator. This process will be aborted if a higher-priority message must be sent on the FDL.

Priority Codeword

Priority codeword data (from the TPCR) can overwrite FDL data provided as described above. After the priority codeword has been written by the MPU to the TPCR with the TXC bit in TPCR set to a one, codeword transmission is initiated. The content of the codeword is determined by the data in TX5–TX0 bits in TPCR. The codeword format of 0XXX XXX0 1111 1111 will be transmitted 10 times. All lower priority FDL transmission will be truncated and replaced with the priority-codeword sequence. While the 10 repetitions are being transmitted, the TXR bit in MR2 is held high. By setting XXX XXX = 000 000, the MPU can send yellow alarms or may use the methods described below. After completing codeword transmission, the INTR* output is asserted if enabled by the TXCODE bit in the IER.

Yellow Alarm

The yellow alarm is the highest priority information in the FDL hierarchy, and transmission of the yellow alarm overrides other information. Yellow alarm can be transmitted by setting the TYEL bit = 1 in CR4. The length of the yellow alarm is determined by both the TYEL bit in CR4 and the YELMD bit in CR0. The YELMD bit controls the alarm duration. The default mode transmits a minimum of 255 repetitions of 1111 1111 0000 0000 when TYEL is set. Setting YELMD allows a custom yellow-alarm transmission length with a duration determined solely by the TYEL bit.

The data from the FDL multiplexer is merged into the transmit output by the transmit multiplexer. This determines when the FDL bits are to be inserted into the serial T1 bit stream.

Receive FDL Data Flow

Information received on the FDL is processed by five parallel mechanisms:

1. Link-Ones Detector
2. Receive-Yellow Detector
3. RLINK-Output
4. Codeword-Detector
5. Performance-Message Assembler

Link-Ones Detector

The link-ones detector allows determination of the type of idle code being sent by the far-end framer. Older designs send all-ones idle codes on the FDL. When 16 consecutive ones are received on the FDL, the LINK1 bit of MR2 is set. Newer designs send HDLC flags as idle codes. Receipt of an HDLC flag resets the LINK1 bit.

Receive-Yellow Detector

The receive-yellow detector monitors the FDL for 16 ±1 repetitions (without errors) of the 1111 1111 0000 0000 yellow alarm pattern. Upon detection of the pattern, the RYEL bit in MR1 is set. RYEL will remain set as long as the pattern continues to be received. An interrupt is generated if alarm interrupt is enabled.

RLINK Output

Receive FDL is passed to the RLINK output. Provision of RLCLK allows the system to easily access the FDL for user-proprietary FDL processing.

Codeword Detector

Priority codewords, including yellow alarms, are detected by a robust algorithm that uses forward-error correcting techniques to provide detection of priority codewords in spite of high bit-error rates. This technique enables 99.8% correct detection of a codeword with a BER of .001. After error correction has taken place, the 6-bit codeword is placed in the Receive Priority Codeword Register (RPCR) with an incremented modulo-4 count value. At that time, the INTR* output is asserted if enabled by the RXCODE bit in the IER.

Performance-Message Assembler

The performance-message assembler (PMA) is triggered by receipt of the expected data pattern in octets 1–4 of the performance report message, including the C/R bit as specified by the RHCR bit in CR0. When triggered, the PMA buffers the next 8 bytes for placement into the far-end performance registers (FEPR1–FEPR8). After the FCS has been checked, the INTR* output is asserted if the RXPERM bit in the IER is set. The results of the latest FCS check are placed in the PMOK bit of MR1.

Line Interface Unit (LIU) Control Section

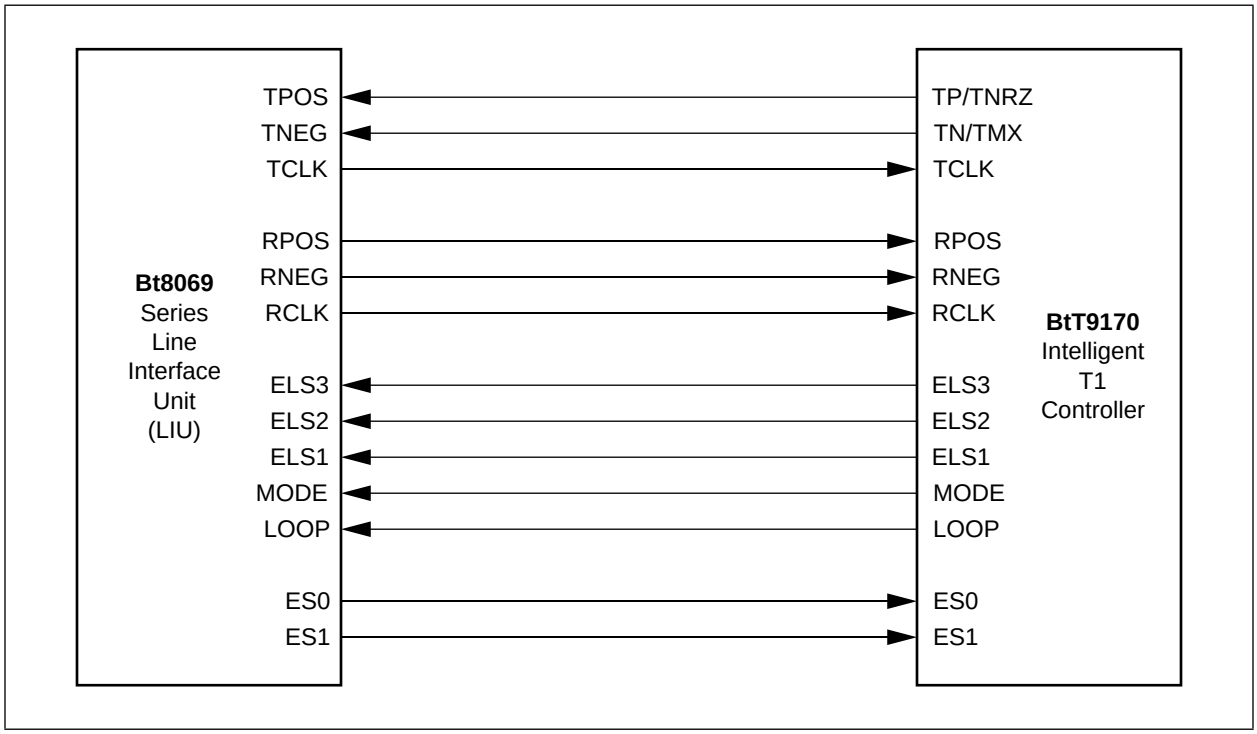
The LIU control section allows the BtT9170 to interface directly with and control the Bt8069-series LIU (see Figure 12). Transmit paired unipolar output data from BtT9170 output pins TP/TNRZ and TN/TMX connect directly to LIU input pins TPOS and TNEG, respectively. Conversely, receive paired unipolar input data from the LIU output pins RPOS and RNEG connect directly to BtT9170 input pins RPOS and RNEG.

Interfacing the transmit and receive data directly between the BtT9170 and an Bt8069-series LIU requires no external circuitry. In addition, the MPU can control the LIU through the contents of register CR4 and access the status of the LIU through register MR2.

The five control lines from the BtT9170 to the LIU select the line equalization (ELS1–ELS3), and master/slave (MODE) and loopback (LOOP) modes of the LIU.

The two status lines from the LIU (ES0–ES1) provide the BtT9170 with the status of the LIU. The status from the LIU can indicate loss of signal, elastic buffer limit, and can inform the BtT9170 of an AIS condition.

Figure 12. Line Interface Unit Interface Signals

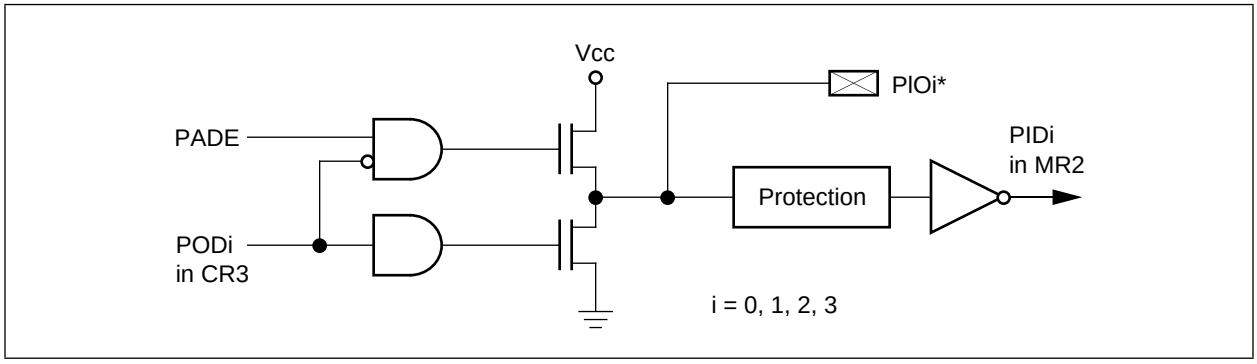


Peripheral I/O Section

The PIO0*, PIO1*, PIO2*, and PIO3* peripheral I/O pins on the 44-pin PLCC and CLCC packages are available for general-purpose use. These four pins can be programmed to be either input/outputs (PADE bit = 0 in CR2) or output only (PADE bit = 1). When programmed as input/output or output only, the outputs of these pins are inverted from the data written in the POD0–POD3 bits in CR3 (i.e., bit state = 1 = output low). The pin state can be monitored in MR2. The PID3–PID0 bit states are inverted from the data state on the PIO3*–PIO0* pins (i.e., bit state = 1 = input low). Figure 13 shows the logic for a peripheral I/O port.

These pins may be configured to control external devices or additional LIU functions, such as RESET and CB.

Figure 13. Peripheral I/O Port



Microprocessor Interface

The BtT9170 is controlled by the MPU through the memory-mapped microprocessor interface. The parallel bus is 80x88 compatible. The addition of a few external components can make the bus compatible with 16/32-bit buses.

The BtT9170 microprocessor interface directly connects to the multiplexed address and data bus without additional logic. The address and data are accessed through pins AD0–AD7 on the BtT9170. The microprocessor bus control lines are: CS*, RD*, WR*, ALE, and INTR*. These hardware signals are described in Table 1.

All registers are 1 byte wide, and are addressed with an 8-bit address. The address space used by the BtT9170 is from address 00H to 7FH. Depending on the function of the register, the access can be either a read/write, read/clear (also called destructive read), or read only. All registers are reset to 00H as a result of power-up or software reset.

The internal registers can be generalized into four functions:

1. Control and Monitor Register Array
2. Per-Channel Control Register Array
3. Received Signalling Registers
4. Performance Registers

Asynchronous MPU Reads

The BtT9170 provides two types of read cycles—short read and long read with latched data output.

During an MPU short read cycle, BtT9170 data outputs reflect the content of the addressed register after a given period of time (refer to tRLDV timing parameter #10a, Table 7). For long read, an additional 1/2 TCLK cycle must elapse (refer to tRLDL timing parameter #10b, Table 7) before data outputs become latched and are guaranteed not to change. MPU read cycles which use long read strobes (RD* assertion ≥ tRLDL) can guarantee MPU bus setup/hold times and avoid bus timing hazards associated with asynchronous MPU read cycles.

MPU read cycles using short read strobes, (RD* assertion ≥ tRLDV and < tRLDL), may do so without compromising bus timing, provided the MPU responds to the register update indicator and completes the register read before the next update occurs. BtT9170 supplies a register update indicator to identify when each register is updated and its contents are latched. The update indicator for most registers (MR0, RXCODE, NEMR, FEPR, RXSIG) is a bit becoming set in the interrupt cause register (ICR), and the update indicator for ICR is the negative edge of the interrupt output pin (INTR*). Interrupts may not be applicable to every system design, but even in a polled system the MPU can enable interrupts in IER and poll the INTR* pin to determine when an update occurs. Register update intervals and their associated update indicators are listed in Table 3.

Since MPU reads are not synchronized to internal register updates, short reads that do not follow an update indicator and short reads from registers which lack an update indicator are subject to asynchronous bus timing hazards. The worst timing hazard results in read data that is a mixture of old and new (updated) bits. To avoid acting upon transitory data read under these circumstances, the MPU may use a software latching procedure to resolve the asynchronous data transfer effects. The software latching procedure reads the register twice and compares results; if the results from back-to-back short reads are identical, then read data may be considered latched.

Table 3. RD-Only Register Updates

RD-ONLY REGISTER	UPDATE INTERVAL	UPDATE INDICATOR
MR0	16 TCLK	ALAMS = 1 in ICR
MR1 (D7) (D6) (D5-D3) (D2-D0)	16 TCLK	 COFA = 1 in MRO RXPERM = 1 in ICR 1SEC = 1 in ICR none
MR2 (D7) (D6-D0)	16 TCLK	 TXCODE = 1 in ICR none
RPCR	40 ms	RXCODE = 1 in ICR
ICR	16 TCLK	INTR* output = 0
RSR1-15	1.5 ms (SF), 3.0 ms (ESF)	RXSIG = 1 in ICR
NEMR1-6	1 second	1 SEC = 1 in ICR
FEPR1-8	1 second	RXPERM = 1 in ICR

Control and Monitor Register Array

Monitor Registers There are three monitor registers that report the status of the BtT9170: two read-only registers, MR1 and MR2; and one read/clear register, MR0 (e.g., status of the receiver framing alignment, LIU, and FDL). Alarms (e.g., red or yellow alarm) and error conditions are also reported. Register MR0 is cleared when it is read by the MPU.

Priority Codeword Registers Priority codewords are specific commands transmitted and received on the facility data link (ESF mode only). Two priority codeword registers are provided. One read-only register, RPCR, supports the receive function; one read/write register, TPCR, supports the transmit function.

Control Registers Six read/write control registers, CR0–CR5, select the operating modes of the BtT9170 (e.g., framing: SF, ESF, or N mode; zero suppression; and yellow-alarm transmission modes). Also included are peripheral I/O pin control, LIU control, FDL control, and synchronization control.

Idle Code Register Other than the standard accepted idle codes, the user can program a specific 8-bit idle code. This custom idle code can then be used in place of the standard idle code in both the receiver and transmitter sections. There is one read/write register for idle code, IR.

Default Signalling Register Default 2-, 4-, and 16-code signalling can be specified. When receive signalling substitution is enabled by the bits in the per-channel control register, the substitution is made from this read/write register, DSR.

Alarm Enable Register Bits in the AER, read/write, register correspond to the alarms reported in Monitor Register 0 (MR0). If any alarm enable bit is set and the corresponding alarm condition is reported in the MR0, then the ALARMS bit is set in the Interrupt Cause Register (ICR).

Interrupt Enable Register The one IER, read/write, register allows the INTR* output to the MPU to be asserted upon selected conditions reported in the ICR. A variety of conditions and errors, including alarm conditions enabled in the AER, can cause INTR* to be asserted if enabled in this register.

Interrupt Cause Register Bits in the one ICR, read/clear, register indicate which of the enabled interrupts in IER caused INTR* to be asserted. In response, the MPU must read this register to determine which condition caused the interrupt in order to perform the correct interrupt service routine. All bits in the ICR except the ITST bit are cleared when the ICR is read by the MPU.

Per-Channel Control Register Array

The per-channel control register array consists of 24 identical read/write registers (PCCR1–PCCR24), each specifically assigned to a single channel. Each register allows the user to choose codes to selectively control the substitution of IDLE/milliwatt code, receiver trunk conditioning, receiver signalling storage, receiver signalling substitution, and transmitter channel conditioning on a per-channel basis. Conditioning or substitution for a single channel occurs independently of all other channels.

Received Signalling Registers

The received signalling registers are 12 read-only registers: RSR1–3, RSR5–7, RSR9–11, and RSR13–15. These registers are grouped into four subarrays corresponding to the received signalling bits A, B, C, D. RSR1–RSR3 hold the signalling bit A from all 24 channels in a frame; RSR5–RSR7 bit B; RSR9–RSR11 bit C; and RSR13–RSR15 bit D.

Performance Registers

The performance registers consist of two sets of registers, one set reporting near-end performance and one set reporting far-end performance.

Near-End Monitor Registers

The six read-only near-end monitor registers (NEMR1–NEMR6) report the receiver's performance for the previous 1-second monitoring interval. NEMR1 and NEMR2 hold the number of CRC-6 block or Fs-bit errors (up to 4095). NEMR3 and NEMR4 hold the number of Ft-bit errors (up to 4095) and severely errored framing events (0, 1, 2, or more). NEMR5 and NEMR6 hold the number of bipolar violations (up to 4095). Received error counts greater than 4095 are reported as 4095.

Far-End Performance Registers

The eight read-only far-end performance registers (FEPR1–FEPR8) contain the most recent information that was transmitted by the far end in the form of the performance report message received by the BtT9170. Performance is reported in terms of the number of CRC-6 block errors, framing bit errors, bipolar violations, and severely errored framing events that the far end experienced. These registers contain octets 5–12 of the received performance report (see Figure 8).

Internal Registers

The BtT9170 internal registers addressable from the MPU bus are listed in Table 4. The BtT9170 registers are 1 byte addressable and are 1 byte wide. The address space is 00H to 7FH, and any address greater than 7FH is ignored by the BtT9170. *After power-up or software reset, all registers are reset to 00H.*

Writing to an undefined address within the 00H-to-7FH address range will not affect any of the registers at a defined address. Reading an undefined address will cause indeterminate data to be transferred to the MPU data bus.

Table 4. BtT9170 Internal Register Map *(1 of 3)*

Addr (Hex)	Register Label	Bit Number							
		7	6	5	4	3	2	1	0
Control And Monitor Registers									
00	MR0	RRED	AISDET	LOST	CRCS	BPVS	FERR	RYEL	COFA
01	MR1	ALTF	PMOK	ODDS	LBST	PDV	RRED	SC2	SC1
02	MR2	TXR	LINK1	ES1	ES0	PID3	PID2	PID1	PID0
03	RPCR	RXP	RXQ	RX5	RX4	RX3	RX2	RX1	RX0
04	TPCR	TXC	-	TX5	TX4	TX3	TX2	TX1	TX0
05	CR0	YELMD	TKLE	THCR	RHCR	FM1	FM0	LCM1	LCM0
06	CR1	REDMD	OLFRE	(1)	(1)	(1)	RZSD	FSE	SL
07	CR2	RESET	RFSR	PADE	PER	MPD	MPM	TCE	CGA
08	CR3	U1BIT	U2BIT	RBIT	PMSL	POD3	POD2	POD1	POD0
09	CR4	TYEL	SAIS	ADS	MODE	LOOP	ELS3	ELS2	ELS1
0A	CR5	MASTER	ETNRZ	PLAUTO	PLOOP	EXLPS	FBYPAS	LBYPAS	CBYPAS
0B	IR	IREG1	IREG2	IREG3	IREG4	IREG5	IREG6	IREG7	IREG8
0C	DSR	(1)	D2A	D4B	D4A	D16D	D16C	D16B	D16A
0D	AER	RRED	AISDET	LOST	CRCS	BPVS	FERR	RYEL	COFA
0E	IER	1SEC	RXCODE	TXCODE	RXPERM	RXSIG	ALARMS	-	ITST
0F	ICR	1SEC	RXCODE	TXCODE	RXPERM	RXSIG	ALARMS	0	ITST
10		-	-	-	-	-	-	-	-
				•					
				•					
				•					
1F		-	-	-	-	-	-	-	-

Notes: (1). Reserved for factory test; must remain zero.

Table 4. BtT9170 Internal Register Map *(2 of 3)*

Addr (Hex)	Register Label	Bit Number							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Per Channel Control Registers									
20	PCCR1	P	Q	X	E	D	C	B	A
21	PCCR2	P	Q	X	E	D	C	B	A
		•							
		•							
		•							
36	PCCR23	P	Q	X	E	D	C	B	A
37	PCCR24	P	Q	X	E	D	C	B	A
38		-	-	-	-	-	-	-	-
		•							
		•							
		•							
3F		-	-	-	-	-	-	-	-
Received Signalling Registers									
40	RSR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
41	RSR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
42	RSR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
43		-	-	-	-	-	-	-	-
44	RSR5	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
45	RSR6	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
46	RSR7	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
47		-	-	-	-	-	-	-	-
48	RSR9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
49	RSR10	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
4A	RSR11	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
4B		-	-	-	-	-	-	-	-
4C	RSR13	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
4D	RSR14	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
4E	RSR15	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
4F		-	-	-	-	-	-	-	-

Table 4. BtT9170 Internal Register Map *(3 of 3)*

Addr (Hex)	Register Label	Bit Number							
		7	6	5	4	3	2	1	0
Near-End Monitor Registers									
50		-	-	-	-	-	-	-	-
51		-	-	-	-	-	-	-	-
52	NEMR1	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
53	NEMR2	0	0	0	0	CRC11	CRC10	CRC9	CRC8
54	NEMR3	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
55	NEMR4	SEF1	SEF0	0	0	FBE11	FBE10	FBE9	FBE8
56	NEMR5	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
57	NEMR6	0	0	0	0	BPV11	BPV10	BPV9	BPV8
Far-End Monitor Registers									
58	FEPR1	G3	LV	G4	U1	U2	G5	SL	G6
59	FEPR2	FE	SE	LB	G1	R	G2	Nm	Nl
5A	FEPR3	G3	LV	G4	U1	U2	G5	SL	G6
5B	FEPR4	FE	SE	LB	G1	R	G2	Nm	Nl
5C	FEPR5	G3	LV	G4	U1	U2	G5	SL	G6
5D	FEPR6	FE	SE	LB	G1	R	G2	Nm	Nl
5E	FEPR7	G3	LV	G4	U1	U2	G5	SL	G6
5F	FEPR8	FE	SE	LB	G1	R	G2	Nm	Nl

Monitor Registers

The monitor registers report BtT9170 status to the MPU.

Monitor Register 0 (MR0)

MR0 is a destructive read-only register that will reset all its bits following an MPU read of MR0. When a bit has been set as a result of a condition, the bit will remain set until MR0 is read. Conditions indicated in this register may be selectively enabled to assert the INTR* output. [See alarm enable register (AER).]

RRED **Receive Red Alarm**. The RRED bit is used to indicate that a loss of frame alignment has occurred.

0 = No red alarm
1 = Red alarm has occurred

AISDET **Alarm Indication Signal Detected**. The AISDET bit is used to indicate that an unframed all ones condition has been detected.

0 = No all ones condition detected
1 = All ones condition detected

LOST **Lost Carrier**. The LOST bit is used to indicate that a loss of carrier has occurred. A loss of carrier occurs when neither RPOS or RNEG receives a high-level input for 31 consecutive bit times.

0 = No lost carrier
1 = Lost carrier

CRCS **CRC-6 Error Status**. The CRCS bit is used to indicate that one or more CRC-6 block errors have occurred.

0 = No CRC-6 errors
1 = CRC-6 error detected

BPVS **Bipolar Violation Status**. The BPVS bit is used to indicate that one or more bipolar violations have occurred.

0 = No bipolar violations
1 = Bipolar violation detected

FERR **Framing Error(s)**. The FERR bit is used to indicate that one or more frame-alignment bit errors have occurred. When set to a one, FERR does not necessarily indicate that synchronization has been lost.

0 = No F-bit error
1 = F-bit error detected

RYEL **Receive Yellow Alarm**. The RYEL bit is used to indicate that a yellow alarm has been received. In N and SF modes, this condition is triggered by receiving all bit 2 = 0 in channels 1–24. In SF mode, this condition can alternatively be triggered by the reception of the Fs bit = 1 in frame 12 while YELMD = 1. In ESF mode, this is initiated by receiving 16 ±1 repetitions of 8 ones and 8 zeros pattern on the data link.

0 = No yellow alarm
1 = Yellow alarm

COFA **Change Of Frame Alignment**. The COFA bit is used to indicate that the RSYNC signal has changed alignment of the off-line framer with respect to its last multi-frame position.

0 = No COFA detected
1 = COFA detected

Monitor Register 1 (MR1)

MR1 is a non-destructive read-only register that samples the FDL status and the receive framing conditions.

ALTF **Ft Alternation Error**. One out of five errors was detected while checking Ft alternating pattern. This could indicate that a two frame controlled slip occurred. This detection does not necessarily indicate that synchronization has been lost (N and SF modes only).

0 = No alternation error detected
1 = Alternation error detected

PMOK **Performance Message OK**. The PMOK bit is used to indicate that a performance message has been received without FCS error.

0 = No performance message report was received since power-up or software reset, or the last report had an FCS error
1 = Performance message has been received with no FCS error

ODDS **Odd Second**. The ODDS bit is used to indicate that an odd second has been detected in the data link bit or the long second has occurred. The one-second timer has three periods of 999, 999, and 1002 ms.

0 = No odd second
1 = Odd second

LBST **Payload Loopback Status**. The LBST bit is used to indicate if the BtT9170 is in payload loopback mode.

0 = No loopback
1 = Loopback

PDV **Performance Data Valid**. The PDV bit is used to indicate that the near-end performance data is valid. Performance data is not valid under any of the following conditions:

1. Receiver is not synchronized.
2. PUP* or RESET has been activated and the 1-second timer has not expired.
3. COFA has occurred and the 1-second timer has not expired.
4. Change in Transmit Sync (TS*) and the 1-second timer has not expired.

0 = Performance data not valid
1 = Performance data valid

RRED **Receive Red Alarm**. The RRED alarm bit is used to indicate that the RRED output pin is active. The criteria for RRED is 2 out of 5 F-bits in error.

0 = RRED output is low
1 = RRED output is high

SC2,SC1 **State Code 2, 1**. These 2 bits in conjunction with RRED bit in MR1 are used to indicate the status of the receiver framing alignment.

RRED(1)	RRED(2)	SC2	SC1	Status
1	1	0	0	Restart/start
1	1	0	1	Initialize
1	1	1	0	Search for candidate phase 1
1	1	1	1	Search for candidate phase 2
1	0	0	0	Search for multiframe
1	0	0	1	Prove frame alignment
1	0	1	0	Prove multiframe alignment
0	0	1	1	Synchronized

Notes: (1). REDMD bit = 0 in CR1.
(2). REDMD bit = 1 in CR1.

Monitor Register 2 (MR2)

MR2 is a non-destructive read-only register containing the LIU's status, the state of the priority codeword response, and the peripheral input data bits.

TXR **Transmit Response**. The TXR status bit reflects the state of the priority codeword transmitter.

0 = Ready to accept codeword in TPCR.
1 = Presently transmitting codeword; not ready to accept new codeword in TPCR.

LINK1 **Link 1**. The LINK1 bit is set if 16 consecutive ones are received on the FDL. LINK1 is reset by receiving an HDLC flag (0111 1110).

0 = Not link 1
1 = Link 1

ES1,ES0 **Error Status 1, 0**. These encoded error status bits indicate the condition of the LIU receiver.

ES1	ES0	
0	0	AIS detected
0	1	Elastic buffer limit
1	0	Loss of signal
1	1	No error

PID3–PID0 **Peripheral Input Data Bit 3–0**. These bits are the inverted data as seen on the PIO3*–PIO0* pins.

Priority Codeword Registers

Priority codewords are specific commands transmitted and received on the facility data link (available only in ESF mode). These priority codewords are distinguished from other data by a repetitive transmission data pattern in the form:

MSB ↓	LSB ↓		
0XXX	XXX0	1111	1111

BtT9170 is programmed to repeat transmitting this pattern.

NOTE: XXX XXX is the content of TX5–TX0 in TPCR if the priority codeword is being transmitted, and if the priority codeword is received, it is stored as RX5–RX0 in the RPCR.

The right-most bit is transmitted and received first. Of the possible 64 patterns for XXX XXX bits, two are capable of generating automatic response in the BtT9170. The two automatic responses, payload loopback activation and deactivation, are enabled by the PLAUTO bit in CR5.

Codeword	Response
0001 0100 1111 1111	Payload Loopback Activate
0011 0010 1111 1111	Payload Loopback Deactivate
Another special codeword is:	
0000 0000 1111 1111	Yellow Alarm

Priority codewords have higher priority than the performance message data and will truncate any current performance message transmission. Back-to-back codewords (repeated or different codewords) can be transmitted without full or partial flag separations. This is accomplished as long as the succeeding codeword is set no later than 210 microseconds after the TXR bit in MR2 indicates that BtT9170 is ready to transmit the next priority codeword.

The priority codeword detector can receive codewords correctly 99.8 percent of the time with a Bit Error Rate (BER) of 0.001. After powerup or software reset, all priority codeword registers are reset to zero.

Receive Priority Codeword Register (RPCR)

RPCR is a non-destructive read-only register containing information regarding the number of priority codewords received and the latest priority codeword.

RXP, RXQ Upon receipt of a codeword, BtT9170 increments the count stored in [2 x RXP + RXQ] modulo 4. (RXP and RXQ will repeat the count 00, 01, 10, 11.)

RX5–RX0 **Receive Data Bits 5–0**. Upon receiving a code word, the latest codeword is placed in these bits with RX0 being the first bit received, and RX5 being the last bit received.

Transmit Priority Codeword Register (TPCR)

TPCR is a read/write register containing the transmitted priority codeword.

TXC **Transmit Command**. Priority codeword (set of 10 repetitions) is transmitted as long as this bit is set. TXC should be cleared after TXR has been set when a single group of 10 repetitions is the desired transmission.

0 = No request to transmit
1 = Request to transmit codeword

TX5–TX0 **Transmit Data Bits 5–0**. These bits contain the priority codeword to be transmitted. TX0 is the code bit to be transmitted first, while TX5 is the last codeword bit to be transmitted.

Control Registers

The control registers emulate many of the strap inputs of a hard-wired framer. All control registers are read/write registers. After power-up or software reset, all control register bits are reset to zero.

Control Register 0 (CR0)

Control register 0 selects the yellow mode, data link bandwidth, framing mode, and zero suppression.

YELMD **Yellow Mode**. The YELMD bit controls the method of detection and transmission of a yellow alarm. In N mode, there is only one kind of yellow alarm (bit 2 inhibit), therefore this bit does not affect that mode.

SF Mode:
0 = Yellow alarm is sent by setting bit 2 = 0 in all data channel
1 = Yellow alarm is sent by setting Fs bit = 1 in frame 12
ESF Mode:
0 = Normal yellow alarm transmission interval of 255 patterns
1 = Alarm length controlled by TYEL bit in CR3

TKLE **Two Kilobit Link Enable**. The TKLE bit is meaningful only in ESF mode. This bit is used to program 4 kbps or 2 kbps FDL. Link frames for 2 kbps are frames 3, 7, 11, 15, 19, and 23. This mode is compatible with ZBTSI.

0 = 4 kbps receive FDL data
1 = 2 kbps receive FDL data

THCR **Transmit Header Command/Response**. In ESF mode, the THCR bit controls the C/R bit during transmission of performance report messages.

0 = Send C/R bit = 0
1 = Send C/R bit = 1

RHCR **Receive Header Command/Response**. In ESF mode, the RHCR bit controls detection of the C/R bit in octet 2 of the received performance report message.

0 = Detect C/R bit = 0
1 = Detect C/R bit = 1

FM1, FM0 **Framing Mode 1, 0**. These 2 bits select the framing mode.

FM1	FM0	Mode
0	0	ESF – Extended Superframe
X	1	SF – Superframe
1	0	N – Non-Signalling

LCM1, LCM0 **Line Code Mode 1, 0**. These 2 bits select the transmitter zero suppression coding or transparent mode of operation.

LCM1	LCM0	Mode
0	0	B8ZS
0	1	Bit 7 stuffing
1	X	Transparent

Control Register 1 (CR1)

Control register 1 controls synchronization and off-line framer selection.

REDMD **Red Mode**. The REDMD bit selects the criteria for determining the characteristic of the RRED output pin.

REDMD	Condition	RRED Pin
1	Frame aligned (may or may not be multiframe aligned)	0
0	Frame and multiframe aligned	0
X	Frame not aligned	1

OLFRE **Off-line Framer Enable**. The OLFRE bit is used to enable the off-line framer mode of operation. OLFRE selects the error counting method. OLFRE = 0 enables error counting only when the on-line framer is in both frame and multiframe sync, such as when RRED = 0 and REDMD = 0. When OLFRE = 1, errors are counted at all times except during the first out-of-sync period following power-up.

OLFRE also controls the RSYNC output pin behavior. RSYNC appears only when the on-line framer is in frame and multiframe sync if OLFRE = 0. RSYNC follows the off-line framer if OLFRE = 1.

0 = Off-line framer disabled
1 = Off-line framer enabled

RZSD **Receiver Zero Suppression Disable**. This bit optionally disables the receiver B8ZS clear channel capability.

0 = B8ZS decoding enabled
1 = B8ZS decoding disabled

FSE **Frame Slip Enable**. (Applicable in SF mode only) The FSE bit allows frame slips to occur without requiring a complete search for frame realignment. A frame slip is considered simply a loss of multiframe, and only realignment to multiframe is all that is necessary when FSE = 1. Applications requiring a complete frame realignment on a frame slip should reset FSE to zero.

SL **Sync Lock**. This bit is used to hold the receiver in sync (when sync is achieved). This will prevent the BtT9170 from trying to reframe the receiver when framing errors are detected.

0 = Sync lock disabled
1 = Sync lock enabled

Control Register 2 (CR2)

RESET **Software Reset**. This bit allows the MPU software to initialize the BtT9170. When RESET is set to a one, the BtT9170 performs the same internal logic reset as caused by assertion of the PUP* input. However, the output pins do not float. The BtT9170 initialization process resets the RESET bit to a zero. After power-up or software RESET, the MPU should not write to the control registers for at least 16 TCLK cycles.

0 = RESET not asserted
1 = RESET asserted

RFSR **Receiver Frame Synchronization Restart**. This bit, when momentarily set greater than 16 TCLK periods, causes the BtT9170 receiver to restart a frame-alignment search. To restart the receiver, set RFSR = 1 for at least 16 TCLK cycles, and then reset RFSR to zero. The on-line framer is stopped while RFSR = 1.

PADE **Peripheral Active Drive Enable**. When the PADE bit is set to a one, the four peripheral I/O pins available on the PLCC or CLCC package (PIO0*–PIO3*) are output only, and are actively driven. When PADE is reset to a zero, these pins are passive, driving actively low only when each respective CR3 bit, POD0–POD3, is high.

0 = PIO0*–PIO3* are passive bi-directional pins.
1 = PIO0*–PIO3* are actively driven outputs.

PER **Period**. This bit selects the period for TMX and RSYNC pins.

0 = Multiframe
1 = One frame

MPD, MPM **Mimic Protection Mode/Disable**. The MPM and MPD bits are used to determine receiver framing strategy (ESF mode only):

MPM	MPD	Action
X	0	CRC check in proving and qualification periods
0	1	CRC check in proving period only
1	1	Ignore CRC check

TCE **Trunk Conditioning Enable**. When this bit is set, receiver trunk conditioning is activated as defined by the per-channel control array when the RRED output is high.

0 = Trunk conditioning disabled
1 = Trunk conditioning enabled

CGA **Carrier Group Alarm**. This bit activates receiver trunk conditioning and signalling conditioning as defined by the per-channel control array.

RRED	CGA	TCE	Trunk Conditioning Enabled	Signalling Conditioning Enabling
X	0	0	No	No
0	0	1	No	No
1	0	1	Yes	No
X	1	X	Yes	Yes

Note: X = Don't care

Control Register 3 (CR3)

Control register 3 contains transmitter performance bit control and the peripheral output data bits.

NOTE: To maintain compatibility with ANSI T1.403-1989, U1, U2, and R should all remain at their 0 (default) value.

U1BIT **U1 Performance Bit**. The content of this bit is sent as "U1" in the performance report to the remote end. (See Figure 8.)

U2BIT **U2 Performance Bit**. The content of this bit is sent as "U2" in the performance report to the remote end. (See Figure 8.)

RBIT **Reserve Performance Bit**. The content of this bit is sent as "R" in the performance report to the remote end. (See Figure 8.)

PMSL **Performance Message Slip**. This bit is allocated for reporting the occurrence of a slip event, sent as "SL" in the performance report to the remote end.

POD3–POD0 **Peripheral Output Data 3–0**. These bits are the output data applied to the peripheral I/O (available only in a 44-pin PLCC or CLCC package). The data is inverted and actively driven low or floated to a high impedance state when PADE = 0. When PADE = 1, the peripheral I/O is output only.

PADE	PODi	PIOi* (i= 0 to 3) Pin
0	0	High Impedance (input)
0	1	Active Low (output)
1	0	Active High (output)
1	1	Active Low (output)

Note: When PADE = 1, data propagates from PODi to PIDi even for the 40-lead packages.

Control Register 4 (CR4)

Control register 4 controls alarm transmission and the output pins to the LIU.

TYEL **Transmit Yellow Alarm**. This bit, when set, activates the transmission of a yellow alarm. (Also, see YELMD bit in CR0.)

0 = No request for transmission of yellow alarm
1 = Request transmission of yellow alarm

Yellow alarm is mode dependent as follows:

SF Mode (YELMD= 0) or N Mode. Yellow alarm is transmitted as bit 2 = 0 in all data channels.

SF Mode (YELMD = 1). Yellow alarm is transmitted as a 1-bit replacement for the Fs bit of frame 12.

ESF Mode (YELMD = 0). Yellow alarm is controlled by the activity of TYEL, as follows:

1. If TYEL has a pulse width shorter or equal to, the time required to transmit 255 patterns of 11111111 00000000, the alarm is transmitted for 255 patterns.
2. If TYEL has a pulse width longer than the time required to transmit 255 patterns, the alarm, after completing the 255 patterns, continues until TYEL goes low.
3. A returning TYEL pulse during an alarm transmission resets the pattern counter (i.e., the 255 count) and extends the alarm duration for another 255 patterns.

ESF Mode (YELMD=1). Yellow alarm is controlled by the duration of TYEL. The pattern counter is disabled, allowing continuous alarms of any length.

SAIS **Send Alarm Indication Signal**. This bit allows the transmission of an unframed all ones alarm indication signal (AIS).

0 = Disable AIS transmission
1 = Enable AIS transmission

ADS **AIS Detector Select**. This bit selects either the internal receiver AIS detection circuit or the LIU AIS detector (via the ES0 and ES1 input pins) to control the AISDET bit in MR0.

0 = Select LIU AIS detector
1 = Select internal AIS detector

MODE, LOOP **MODE, LOOP Control**. These two control bits are used together to select the LIU timing and loopback configuration (depending on the specific LIU) to be sent to the LIU via the MODE and LOOP outputs.

ELS3–ELS1 **Equalizer Line Select 3–1**. These bits specify the codes to be sent to the Bt8069-series LIU via their respective outputs to select the cable-length equalization.

ELS3	ELS2	ELS1	Cable Length
0	0	0	0–110 ft
0	0	1	110–220 ft
0	1	0	220–330 ft
0	1	1	330–440 ft
1	0	0	440–550 ft
1	0	1	550–660 ft

Control Register 5 (CR5)

Control register 5 controls miscellaneous functions.

MASTER **Master**. This bit selects the function of the bimodal TS*/TMX pin.

0 = TS* (Transmit Sync) input
1 = TMX (Transmit Maximum) output

ETNRZ **Enable Transmit NRZ**. This bit selects the function of the multiplexed TP/TNRZ and TN/TMX output pins. TNRZ is the non-return-to-zero output for transmitted data. When in the TNRZ mode, the data is not affected by B8ZS encoding, but stuffed bit 7s appear at TNRZ.

ETNRZ Bit	TP/NRZ Pin	TN/TNX Pin
0	TP	TN
1	TNRZ	TMX

PLAUTO **Payload Loop Automatic**. Setting the PLAUTO bit selects the automatic loopback mode. In automatic loopback mode, the FDL priority codeword detection circuit directly controls the payload loopback. When PLAUTO = 0, automatic payload loopback is deactivated. (See PLOOP.)

PLOOP **Payload Loop**. Setting the PLOOP bit selects the payload loopback mode. In this mode, the unaltered receive serial payload (192 bits) is unconditionally looped back to become the transmit serial data (TSER). The transmitter provides sync, link and CRC bits. Data passes through a 14-bit elastic store, receive channel bits are not guaranteed to maintain channel alignment through the elastic store.

PLOOP	PLAUTO	Loopback Mode
0	0	No payload loopback
0	1	Automatic loopback
1	X	Payload loopback

EXLPS **Extracted Link Priority Select**. This bit controls the extracted link transmit priority compared to far-end performance reporting.

0 = Performance report has priority
1 = Extracted link has priority

FBYPAS **F-Bit Bypass**.

LBYPAS **Link Bypass**.

CBYPAS **CRC-6 Bypass**.These bits enable the F-bits, link bits, and CRC-6 bits to be externally supplied as shown in Table 5.

Table 5. F-Bit Control Options

Mode	Options			Input Source		
	FBYPAS	LBYPAS	CBYPAS	FPS/Ft	FDL/Fs	CRC-6
SF	0	X	X(1)	BtT9170	BtT9170	NA(2)
SF	1	0	X	TSER	EXDATA	NA
SF	1	1	X	TSER	TSER	NA
ESF	0	0	0	BtT9170	BtT9170(3)	BtT9170
ESF	1	0	0	TSER	BtT9170(3)	BtT9170
ESF	0	1	0	BtT9170	TSER(4)	BtT9170
ESF	1	1	0	TSER	TSER(4)	BtT9170
ESF	0	0	1	BtT9170	BtT9170(3)	TSER
ESF	1	0	1	TSER	BtT9170(3)	TSER
ESF	0	1	1	BtT9170	TSER(4)	TSER
ESF	1	1	1	TSER	TSER(4)	TSER
N	0	0	X	BtT9170	EXDATA	NA
N	1	0	X	TSER	EXDATA	NA
N	0	1	X	BtT9170	TSER	NA
N	1	1	X	TSER	TSER	NA

Notes: (1). Don't care.
(2). Not applicable.
(3). FDL source is BtT9170 or EXDATA input.
(4). FDL source is TSER unless yellow alarm or priority codeword.

Idle Register (IR)

Idle register is a read/write control register that supplies a programmable idle code for both the transmitter and receiver. The contents of this register replace received and transmitted data on any given channel, i, under control of PCCRi (see Tables 6a and 6b).

IREG1 IREG8 **Idle Register Bit 1-8**. These bits are aligned per T1 conventions. IREG1 is the T1 most significant bit and first bit transmitted.

Table 6a. PCCR Coding Structure Architecture

Architecture								
Enabling of Cond/Force			Transmit			Receive		
P	Q	X	COND	ABCD	FORCE	COND	ABCD	FORCE
1	1	1	-----TRANSPARENT-----			no	yes	yes
1	1	0	yes	yes	no	no	yes	yes
1	0	1	yes	yes	no	red	cga	no
1	0	0	yes	yes	no	-----TRANSPARENT-----		
0	1	1	no	yes	yes	red	cga	no
0	1	0	no	yes	yes	-----TRANSPARENT-----		
0	0	1	-----TRANSPARENT-----			red	cga	no
0	0	0	-----TRANSPARENT-----			-----TRANSPARENT-----		

Table 6b. PCCR Coding Structure Application

Application												
Meaning of Cond/Force						Transmit			Receive			RXSIG Array
E	D	C	B	A	MODE	COND	ABCD	FORCE	COND	ABCD	FORCE	
1	D	C	B	A	sig 16	xxxxxxxS	ABCD	0111111S	0111111S	D16	mmmmmmmS	abcd
0	1	1	B	A	BUSY AB	0111111S	ABAB	0111111S	0111111S	ABAB	0111111S	ab
0	1	0	1	1	VACANT	11111111		11111111	11111111		11111111	NO
0	1	0	1	0	IDLE REG	I I I I I I Is	1111	11111111	I I I I I I I I	NO	I I I I I I I I	NO
0	1	0	0	1	DDS IDLE	11111110		00011010	00011010	NO	11111110	NO
0	1	0	0	0	DDS DATA	xxxxxxx1		00011010	00011010	NO	11111110	NO
0	0	1	B	A	sig 4	xxxxxxxS	ABAB	0111111S	0111111S	D4	mmmmmmmS	ab
0	0	0	1	A	sig 2	xxxxxxxS	AAAA	0111111S	0111111S	D2	mmmmmmmS	a
0	0	0	0	1	CLR PCM	01111111		11111111	01111111	NO	mmmmmmmm	NO
0	0	0	0	0	CLEAR	01111110		11111111	NO	NO	NO	NO

Notes:
1. "x" indicates the respective bit from TSER.
2. "S" in bit-8 position indicates robbed-bit signalling is inserted.
3. "s" in bit-8 position indicates that ones are inserted in robbed-bit signalling position for transmission.
4. 00011010 is the Mux Out of Frame (MOOF) code.
5. mmmmmmmS is digital milliwatt with signalling.
6. Leftmost bit of binary codes is sent first.
7. D2, D4, and D16 refer to default signalling from the DSR.

Default Signalling Register (DSR)

The default signalling register is a read/write control register. D2, D4, and D16 default signalling is referred to in Table 6b for per-channel control registers.

D2A **Default A Signalling Channel**. The D2A signal is used as the default value for A, B, C, D when default A signalling is selected in the PCCR for two-code signalling.

D4B **Default AB Signalling Channel for B and D**. The D4B signal is used as the default value for B and D when default AB signalling is selected in the PCCR for four-code signalling.

D4A **Default AB Signalling Channel for A and C**. The D4A signal is used as the default value for A and C when default AB signalling is selected in the PCCR for four-code signalling.

D16D **Default ABCD Signalling Channel for D**. The D16D signal is used as the default value for D when default ABCD signalling is selected in the PCCR for 16-code signalling.

D16C **Default ABCD Signalling Channel for C**. The D16C signal is used as the default value for C when default ABCD signalling is selected in the PCCR for 16-code signalling.

D16B **Default ABCD Signalling Channel for B**. The D16B signal is used as the default value for B when default ABCD signalling is selected in the PCCR for 16-code signalling.

D16A **Default ABCD Signalling Channel for A**. The D16A signal is used as the default value for A when default ABCD signalling is selected in the PCCR for 16-code signalling.

Interrupt Registers

Alarm Enable Register (AER)

The alarm enable register (AER) is a read/write control register. This interrupt mask register prevents or allows the ALARMS bit in the ICR from being set when the corresponding bit in MR0 is set. If the ALARMS bit in the ICR and the ALARMS bit in the IER are set, the INTR* output is asserted. In response, the MPU should examine MR0 to determine the alarm or error causing the interrupt request.

0 = Prevents the corresponding MR0 bit from setting the ALARMS bit in the ICR
1 = Enables the corresponding MR0 bit to set the ALARMS bit in the ICR

Interrupt Enable Register (IER)

The interrupt enable register (IER) is a read/write control register. Each bit of this mask register, if set to a one, allows its respective bit in the ICR, if also set to a one, to assert the INTR* output. After power-up or software reset, all interrupt enable bits in the IER are reset to disable the INTR* output.

0 = Prevent the corresponding ICR bit from asserting INTR* output
1 = Enable the corresponding ICR bit to assert INTR* output

Interrupt Cause Register (ICR)

The interrupt cause register (ICR) is a destructive read-only register whose individual bits are internally set whenever certain conditions occur. Any of these source bits, when enabled by its respective IER mask bit, will cause the INTR* output to be asserted. An MPU read of ICR resets all ICR bits except ITST to zero, which in turn resets the INTR* output if ITST is zero. After power-up or software reset, all ICR bits are reset to initially disable the INTR* output.

1SEC **One-Second Timer Event**. This bit, when set to a one, indicates that an elapsed time of 1 second has occurred and the near-end monitor data has been updated.

RXCODE **Receive Codeword**. This bit, when set to a one, indicates that a priority codeword has been received and should be read.

TXCODE **Transmit Codeword**. This bit, when set to a one, indicates that 10 repetitions of a priority codeword have been sent. TXCODE is not set if a priority codeword transmission is truncated (e.g., by a TYEL).

RXPERM **Received Far-End Performance Report**. This bit, when set to a one, indicates that a new far-end performance report should be read.

RXSIG **Received Signalling Array**. This bit, when set to a one, indicates that new signalling information is available and should be read. RXSIG is set at the end of any multiframe in which at least 1 signalling bit has changed.

ALARMS **Alarms**. This bit, when set to a one, indicates that an alarm bit has been latched in MR0. Persistent alarm conditions will cause the corresponding bits in MR0 to remain set after the MPU reads MR0.

ITST **Interrupt Test**. This bit, when set to a one in the IER, causes the ITST bit in ICR to be set and the INTR* output to be asserted. When MPU software clears the ITST bit in the IER, the ICR's ITST bit is cleared, and normal operation of INTR* output resumes.

Per-Channel Control Registers

Bits [7:0] of each PCCR control per-channel operations (see Tables 6a and 6b).

Architecture Control

Bits [7:5] are called P, Q, and X, respectively. These bits determine the architecture of the channel connection in the system by controlling the enabling of conditioning and forcing functions.

Application Control

Bits [4:0] are called E, D, C, B, and A, respectively. These bits determine the application of the channel connection in the system by controlling the meaning of the conditioning and forcing functions.

Default Operations

The default function, selected by PCCRxx=0000 0000, is for completely transparent receive and transmit data flow.

Transmit Data Flow Control

Transmit conditioning and forcing functions apply to the data path from the TSER input signal to the TP, TN, and TNRZ output functions. When coded by the PCCR, these functions are always active.

Receive Data Flow Control

Receive conditioning and forcing functions apply to the data path from the RPOS and RNEG inputs to the RSER output. When coded by the PCCR, some functions are always active and others depend on the state of the RRED output and on the TCE and CGA bits in CR2. Functions coded by “red” in Table 6a are gated by either the RRED output signal when TCE is set or by the CGA bit. Functions coded as “cga” in Table 6a are gated by the CGA bit alone.

Data Conditioning

Columns in Tables 6a and 6b labeled “COND” are for conditioning of the data passing in the affected channel. Conditioning may apply to all bits of the channel or to selected bits only.

Signalling Conditioning or Force

Columns in Tables 6a and 6b labeled “ABCD” are for signalling. Where signalling applies for transmit functions, the values of the signalling bits are taken from the appropriate A, B, C, and D bits of the PCCR contents. Received signalling can be replaced by other signalling values as the channel exits the device on RSER. These values can come from the A and B bits of the PCCR or from specific values stored in the default signalling register.

Data Force

Columns in Tables 6a and 6b labeled “FORCE” are for data that can unconditionally overwrite that which is presented at the device inputs. Forced channels also include the “ABCD” signalling function where appropriate.

Receive Signalling Array Operations

The “RXSIG ARRAY” column in Table 6b indicates whether received robbed-bit signals are processed into the receive signalling array. If the signals are enabled through the interrupt enable register, these signalling channels may cause an interrupt output if their values change.

Received Signalling Registers

The received signalling registers are grouped into four arrays, each array contains received signalling bits from these channels which have signalling enabled by PCCR application options sig2, sig4, or sig16, or BUSY AB.

Receive Signalling Array A (RSA)

Receive signalling array A is a set of three read-only registers (RSR1–RSR3) containing the A signalling bits received for all 24 channels.

CH1–CH24 **Receive Signalling Channels 1–24**. These bits indicate the most recent A signalling bit of each of the 24 channels.

Receive Signalling Array B (RSB)

Receive signalling array B is a set of three read-only registers (RSR5–RSR7) containing the B signalling bits received for all 24 channels.

CH1–CH24 **Receive Signalling Channels 1-24**. These bits indicate the most recent B signalling bit of each of the 24 channels.

Receive Signalling Array C (RSC)

Receive signalling array C is a set of three read-only registers (RSR9–RSR11) containing the C signalling bit received for all 24 channels.

CH1–CH24 **Receive Signalling Channels 1–24**. These bits indicate the most recent C signalling bit of each of the 24 channels.

Receive Signalling Array D (RSD)

Receive signalling array D is a set of three read-only registers (RSR13–RSR15) containing the D signalling bit received for all 24 channels.

CH 1–CH24 **Receive Signalling Channels 1–24**. These bits indicate the most recent D signalling bit of each of the 24 channels.

Near-End Monitor Registers

The near-end monitor registers are a group of six consecutive read-only registers (NEMR1–NEMR6). These registers report error counts which are updated once each second. They form the basis for the far-end performance report sent over the FDL. Error counting is disabled until the first time sync is achieved. Subsequently, error counting is enabled when the off-line framer is enabled or on-line when the on-line framer is synchronized.

The one-second timing is derived from the transmit multiframe synchronization by counting sequences of 333, 333, and 334 multiframes to arrive at an average of 333-1/3 multiframes per second. At the end of each 1-second interval, the current values of the counters are loaded into the registers and the counters are simultaneously reset so that the counters may count the errors in the next second. The MPU can read the current error counts in the NEMRs for the duration of the next counting interval.

The MPU can set the 1SEC bit in the IER to enable INTR* output to be asserted each time the 1SEC bit of the ICR is set (when a 1-second interval has occurred). An MPU read of the ICR will reset the ICR 1SEC bit and turn off INTR*.

Near-End Monitor Registers 1 and 2 (NEMR1 and NEMR2)

These two read-only registers report CRC-6 block errors or Fs-bit errors depending on the operating mode (not applicable in N mode).

CRC11–CRC0 **Number of CRC-6 Block Errors or Fs-Bit Errors.** These bits indicate the number of CRC-6 block errors (in ESF mode) or Fs-bit errors (in SF mode) received. CRC0 represents the least significant bit, while CRC11 represents the most significant bit. A maximum of 4095 errors can be counted.

Near-End Monitor Registers 3 and 4 (NEMR3 and NEMR4)

These two read-only registers report FPS or Ft-bit errors.

FBE11–FBE0 **Number of F-bit Errors**. These bits indicant bit, while FBE11 represents the most significant bit. A maximum of 4095 errors can be counted.

SEF1–SEF0 **Number of Severely Errored Framing Events**. Severely errored framing events are those in which two-or-more out of six F-bits are in error. SEF0 represents the least significant bit. Three or more severely errored framing events are reported as three errors.

Near-End Monitor Registers 5 and 6 (NEMR5 and NEMR6)

These two read-only registers report bipolar violations.

BPV11–BPV0 **Number of Bipolar Violations**. These bits report the number of bipolar violations received. BPV0 represents the least significant bit, while BPV11 represents the most significant bit. A maximum value of 4095 indicates 4095 or more bipolar violations received.

Far-End Performance Registers

The BtT9170 will receive all 14 bytes in the performance report message as specified by ANSI standard T1.403-1989. The far-end performance registers consist of an array of eight consecutive read-only registers (FEPR1–FEPR8) that contain only the four one-second reports (bytes 5–12 in Figure 8). These bytes are updated whenever a bit sequence appearing to be a performance report is received on the incoming FDL.

Far-End Performance Registers 1 and 2 (FEPR1 and FEPR2)

These two read-only registers report the most current far-end performance status.

G1 **CRC Error Event Range 1**. This bit indicates one occurrence of a CRC-6 block error.

G2 **CRC Error Event Range 2–5**. This bit indicates from 2–5 occurrences of a CRC-6 block error.

G3 **CRC Error Event Range 6–10**. This bit indicates from 6–10 occurrences of a CRC-6 block error.

G4 **CRC Error Event Range 11–100**. This bit indicates from 11–100 occurrences of a CRC-6 block error.

G5 **CRC Error Event Range 101–319**. This bit indicates from 101–319 occurrences of a CRC-6 block error.

G6 **CRC Error Event Range Greater Than 319**. This bit indicates more than 319 occurrences of a CRC-6 block error.

SE **Severely Errored Framing Event**. This bit indicates that at least one severely errored framing event has occurred.

FE **Frame Synchronization Bit Error**. This bit indicates that at least one frame synchronization bit error has occurred without a severely errored framing event.

LV **Line Code Violation**. This bit indicates that at least one line code violation has occurred.

SL **Frame Slip**. This bit indicates that a frame slip occurred at the remote end.

LB **Loopback**. This bit, when set to a one, indicates that the remote end is in payload loopback.

R, U1, U2 **User-Defined Bits**. These bits have not yet been standardized.

Nm, Nl **Far-End Performance Report Order.** Nm and Nl together provide the near end with the order in the count sequence of the far-end performance report being received. By decoding the Nm and Nl (00, 01, 10, 11), the near end can detect if a far-end performance report has been pre-empted by other higher priority functions or lost due to noise.

Far-End Performance Registers 3 and 4 (FEPR3 and FEPR4)

These two read-only registers report the far-end performance status that was recorded 1 second before the report in FEPR1 and FEPR2. Bit descriptions are identical to those of FEPR1 and FEPR2.

Far-End Performance Registers 5 and 6 (FEPR5 and FEPR6)

These two read-only registers report the far-end performance status that was recorded 1 second before the report in FEPR3 and FEPR4. Bit descriptions are identical to those of FEPR1 and FEPR2.

Far-End Performance Registers 7 and 8 (FEPR7 and FEPR8)

These two read-only registers report the far-end performance status that was recorded 1 second before the report in FEPR5 and FEPR6. Bit descriptions are identical to those of FEPR1 and FEPR2.

Switching Characteristics

Microprocessor Interface

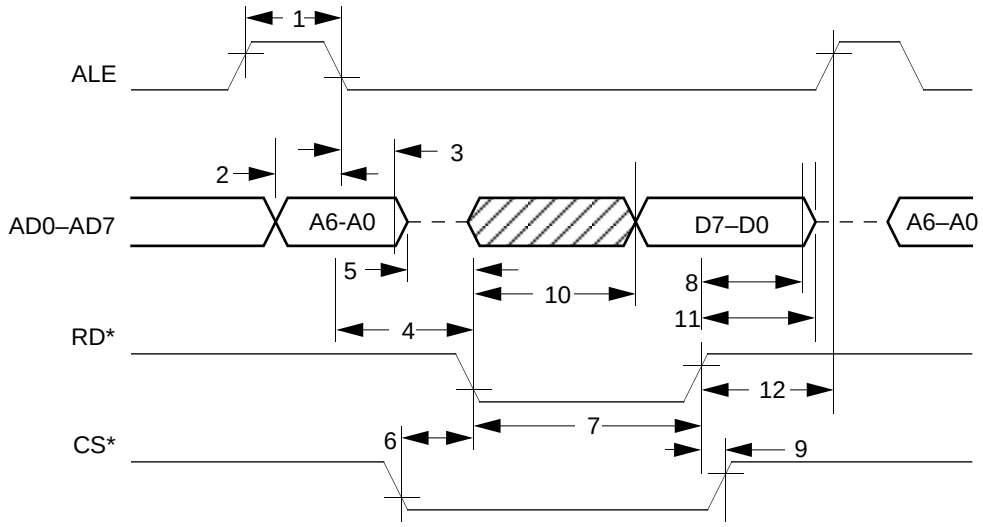
Refer to Tables 7 and 8 and Figures 14 and 15.

Table 7. MPU Bus Interface Read Timing

Number	Symbol	Parameter	Min	Typ	Max	Units
1	t_{LHLL}	ALE High to ALE Low Width	40	–	–	ns
2	t_{AVAL}	Address Valid to ALE Low	15	–	–	ns
3	t_{ALAV}	ALE Low to Address Valid Hold	20	–	–	ns
4	t_{ALRL}	ALE Low to RD* Low	20	–	–	ns
5	t_{AZRL}	Address High Impedance to RD* Low	0	–	–	ns
6	t_{CLRL}	CS* Low to RD* Low Setup Time	0	–	–	ns
7	t_{RLRH}	RD* Low to RD* High Pulse Width	100	–	–	ns
8	t_{RHDH}	RD* High to Data Hold	5	–	–	ns
9	t_{RHCH}	RD* High to CS* High Hold	0	–	–	ns
10a	t_{RLDV}	RD* Low to Data Valid	–	–	80	ns
10b	t_{RLDL}	RD* Low to Data Latched	–	–	405*(1)*	ns
11	t_{RHDZ}	RD* High to Data High Impedance	–	60	–	ns
12	t_{RHAH}	RD* High to ALE High	60	–	–	ns

Notes: (1). Assumes TCLK frequency = 1.544 MHz and TCLK duty cycle = 50/50.
2. Test Conditions: T_A = 0° to 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V.

Figure 14. MPU Bus Interface Read Waveforms



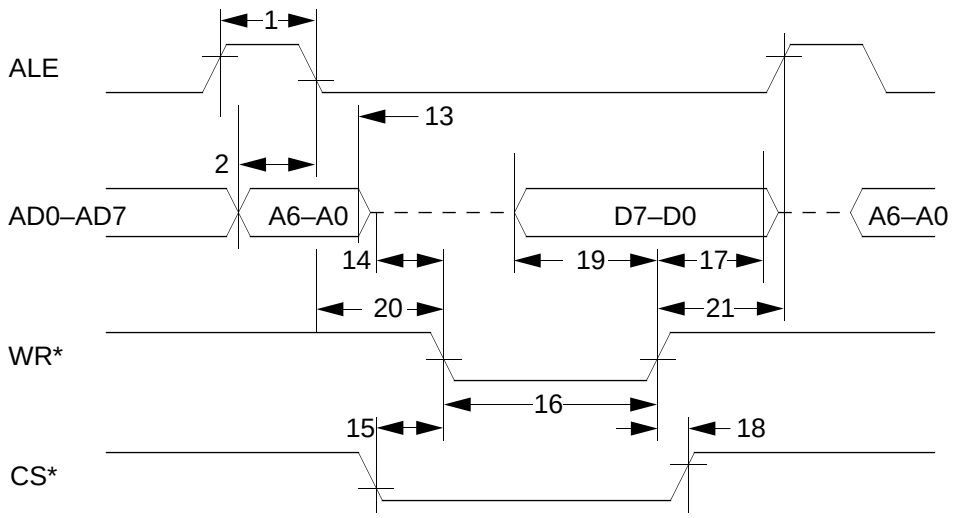
Notes: 1. AC timing threshold measured at 0.8 V and 2.0 V.
2. Output load capacitance: AD0–AD7 at 100 pF; other signals at 50 pF.

Table 8. MPU Bus Interface Write Timing

Number	Symbol	Parameter	Min	Typ	Max	Units
13	t_{ALAV}	ALE Low to Address Valid Hold	20	–	–	ns
14	t_{AZWL}	Address High Impedance to WR* Low	0	–	–	ns
15	t_{CLWL}	CS* Low to WR* Low Setup	20	–	–	ns
16	t_{WLWH}	WR* Low to WR High Pulse Width	100	–	–	ns
17	t_{WHDX}	WR* High to Data Hold	20	–	–	ns
18	t_{WHCH}	WR* High to CS* High Setup	0	–	–	ns
19	t_{DVWH}	Data Valid to WR* High Setup	80	–	–	ns
20	t_{LLWL}	ALE Low to WR* Low	20	–	–	ns
21	t_{WHLH}	WR* High to ALE High	60	–	–	ns

Note: Test Conditions: T_A = 0° to 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V

Figure 15. MPU Bus Interface Write Timing

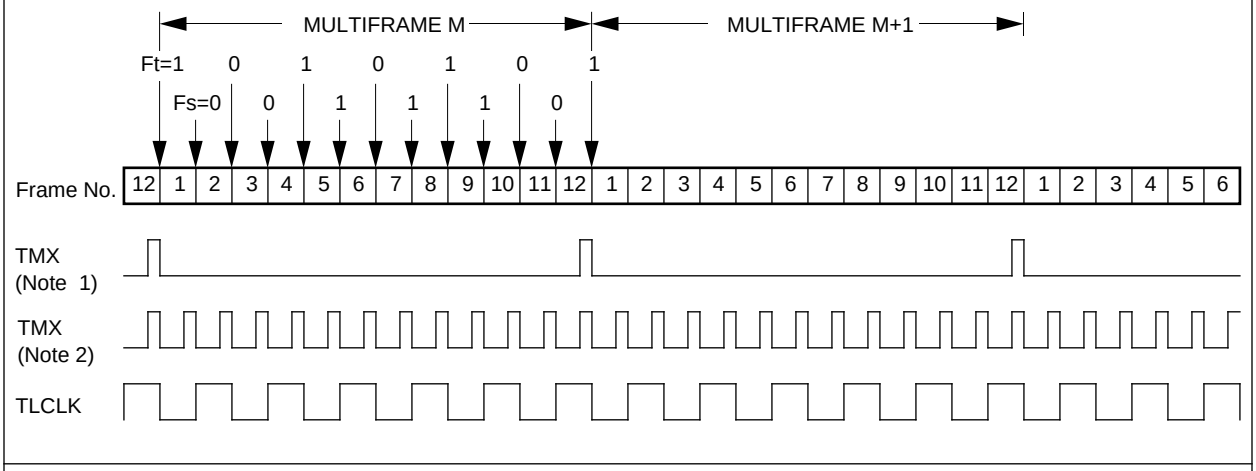


Notes: 1. AC timing threshold measured at 0.8 V and 2.0 V.
2. Output load capacitance: AD0–AD7 at 100 pF; other signals at 50 pF.

Transmit Timing

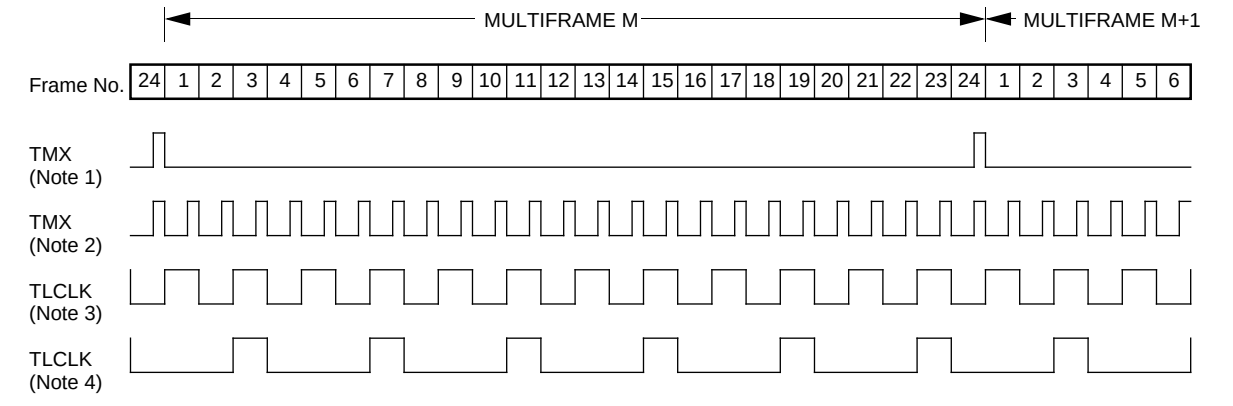
Refer to Figures 16 through 19.

Figure 16. Transmit Interface Timing–SF Mode



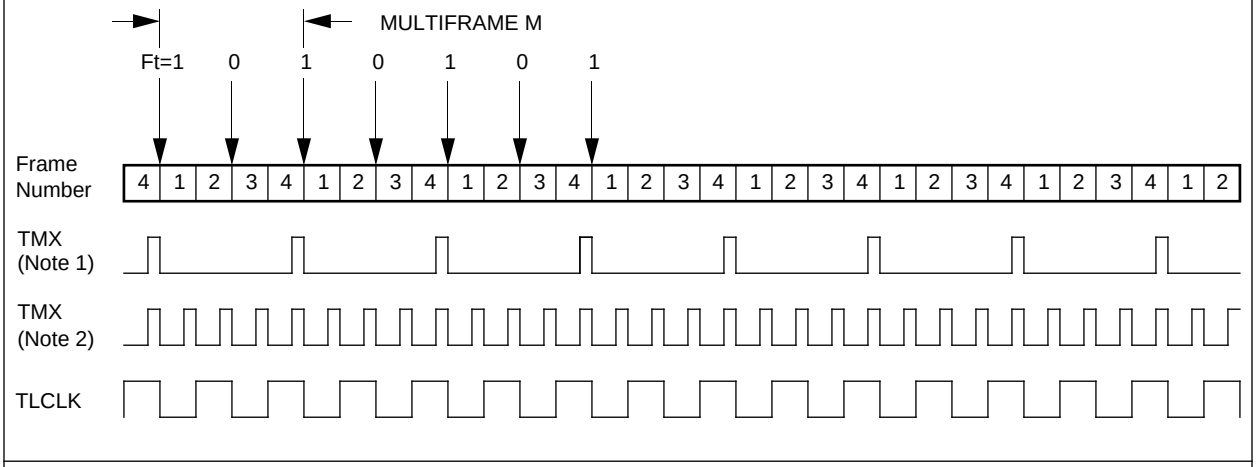
Notes: (1). TMX is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). TMS is programmed to pulse every frame (PER bit = 1 in CR2).

Figure 17. Transmit Interface Timing–ESF Mode



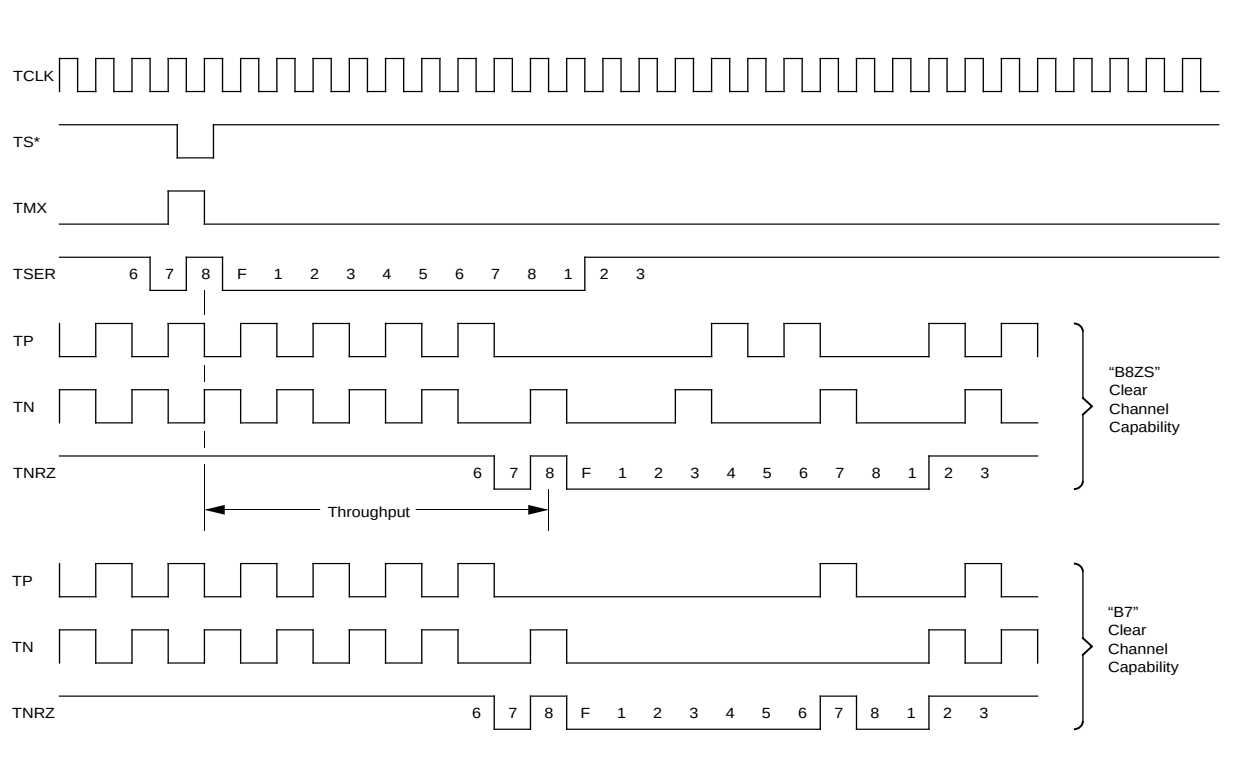
Notes: (1). TMX is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). TMX is programmed to pulse every frame (PER bit = 1 in CR2).
(3). TLCLK is programmed to 4 kHz (TKLE bit = 0 in CR0).
(4). TLCLK is programmed to 2 kHz (TKLE bit = 1 in CR0).

Figure 18. Transmit Interface Timing–N Mode



Notes: (1). TMX is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). TMX is programmed to pulse every frame (PER bit = 1 in CR2).

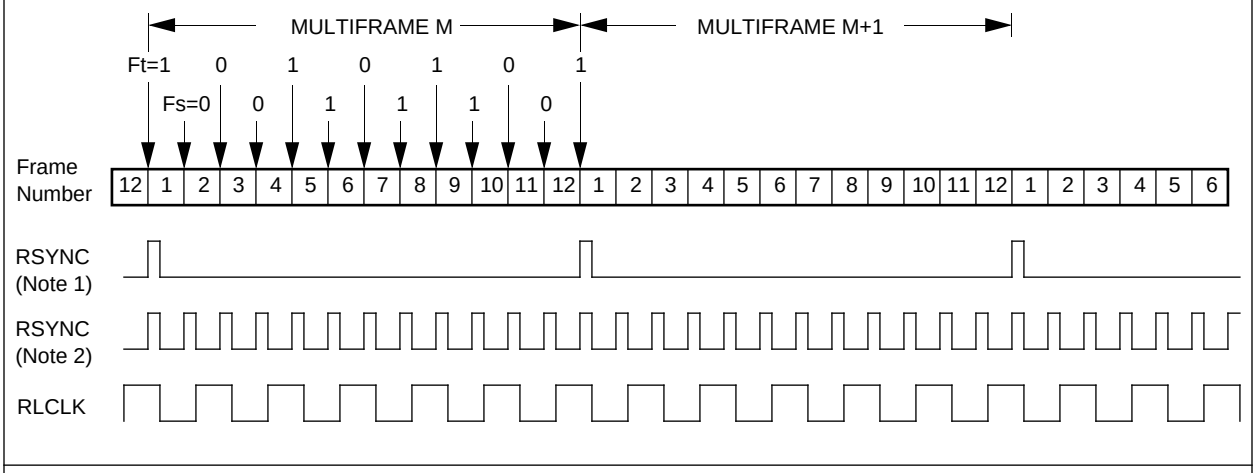
Figure 19. Transmit Timing with B8ZS or Bit-7 Stuffing



Receiver Timing

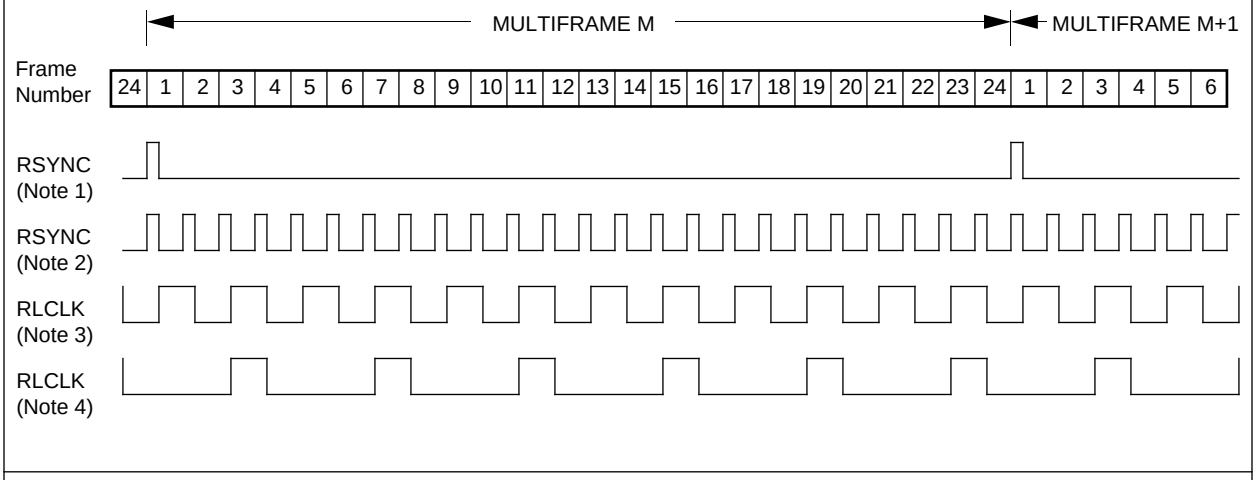
Refer to Figures 20 through 24.

Figure 20. Receive Interface Timing–SF Mode



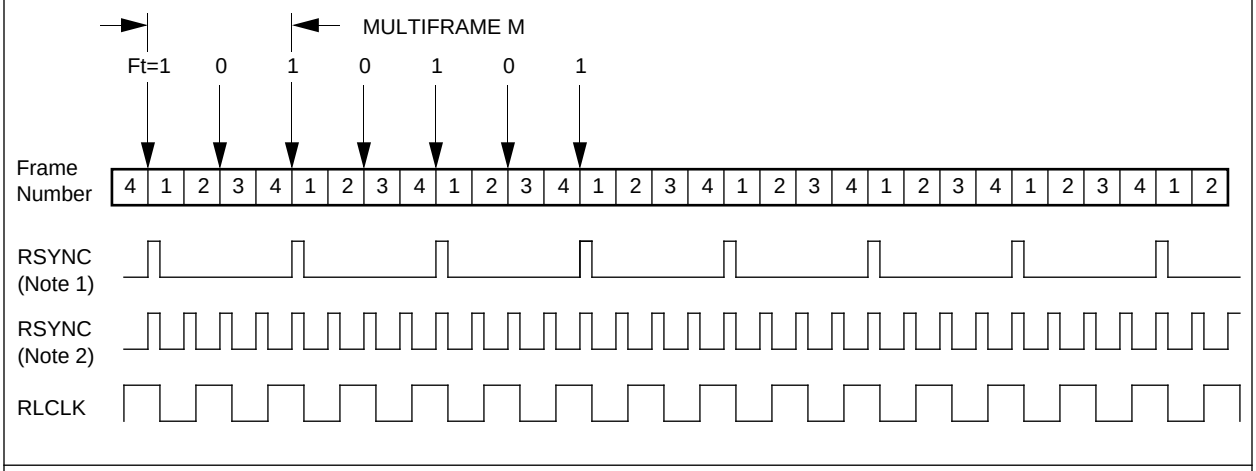
Notes: (1). RSYNC is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). RSYNC is programmed to pulse every frame (PER bit = 1 in CR2).

Figure 21. Receive Interface Timing–SF Mode



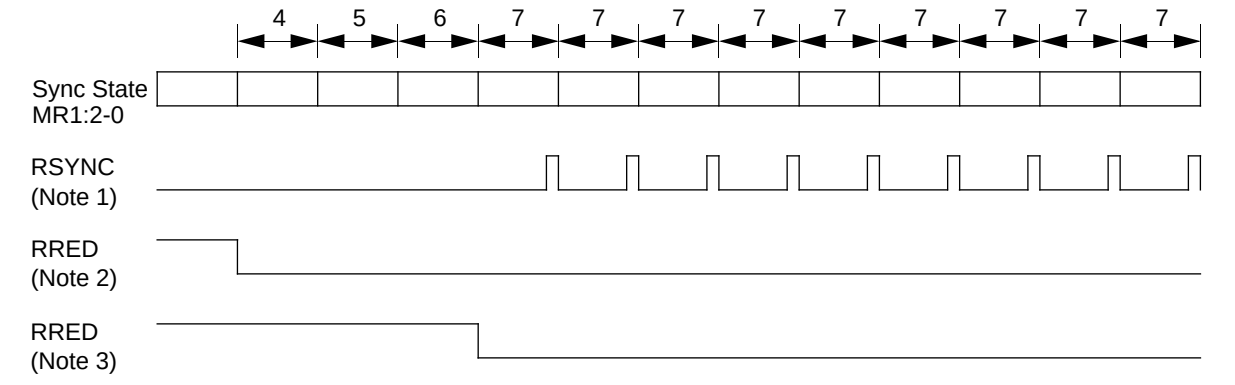
Notes: (1). RSYNC is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). RSYNC is programmed to pulse every frame (PER bit = 1 in CR2).
(3). RLCLK is programmed to 4 kHz (TKLE bit = 0 in CR0).
(4). RLCLK is programmed to 2 kHz (TKLE bit = 1 in CR0).

Figure 22. Receive Interface Timing–N Mode



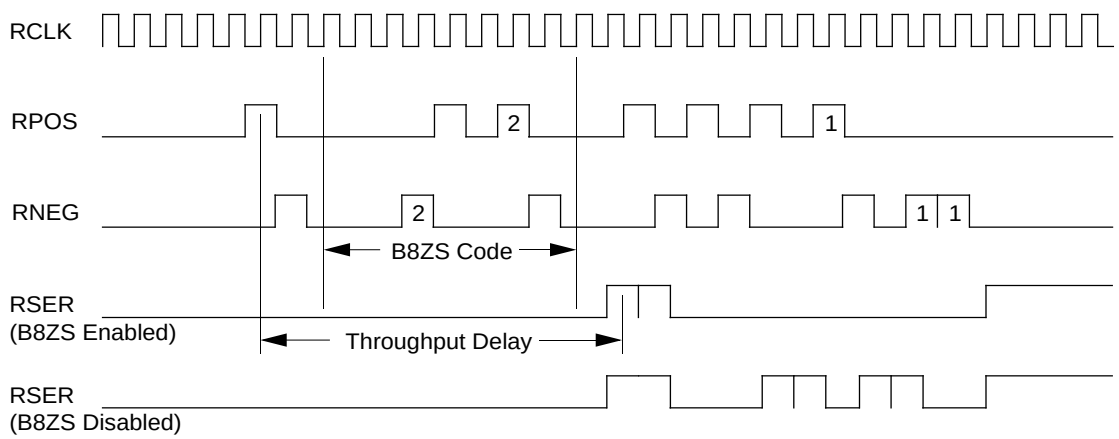
Notes: (1). RSYNC is programmed to pulse every multiframe (PER bit = 0 in CR2).
(2). RSYNC is programmed to pulse every frame (PER bit = 1 in CR2).

Figure 23. RRED Timing (Long and Short)



Notes: (1). When in on-line frame mode, RSYNC will appear when the receiver is synchronized.
(2). RRED when short (REDMD bit = 1 in CR1).
(3). RRED when long (REDMD bit = 0 in CR1).
4. Search for multiframe alignment.
5. Confirming multiframe alignment (ESF CRC-6 calculation).
6. Confirming multiframe alignment (ESF CRC-6 validation).
7. Multiframe length: For N mode: 4 frames; SF mode: 12 frames; ESF mode: 24 frames.

Figure 24. Receiver B8ZS Decoding



Notes: (1). Bipolar violations, any mode.
(2). Bipolar violations if B8ZS mode disabled.

Clock and Data Timing

See Table 9 and Figures 25 through 27.

Table 9. Clock Timing

Parameter	Symbol	Min	Max	Units
Clock Frequency	f_C	0.1	3.1	MHz
Clock Pulse Width High	t_{CH}	160	-	ns
Clock Pulse Width Low	t_{CL}	160	-	ns
Input Data Setup Time	t_{DS}	60	-	ns
Input Data Hold Time	t_{DH}	60	-	ns
Output Data Delay Time	t_{DOD}	10	100	ns
Clock Rise/Fall Time	t_R, t_F	-	20	ns

Figure 25. Minimum Clock Pulse Widths

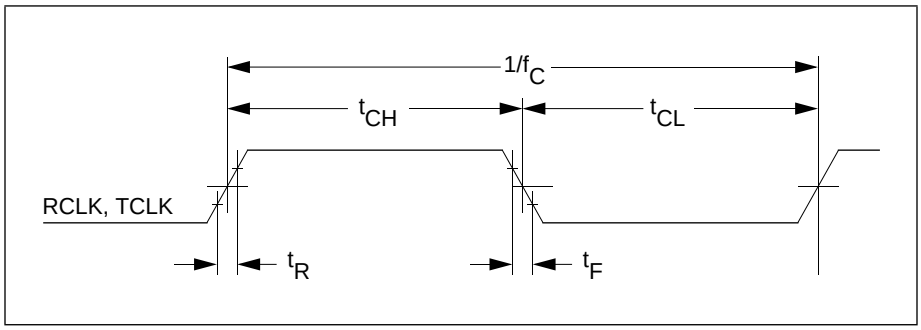


Figure 26. Input Data Setup and Hold Times

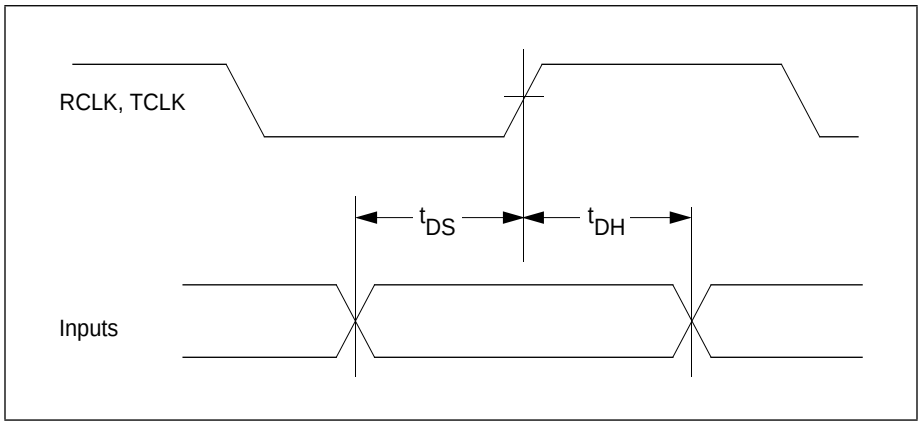
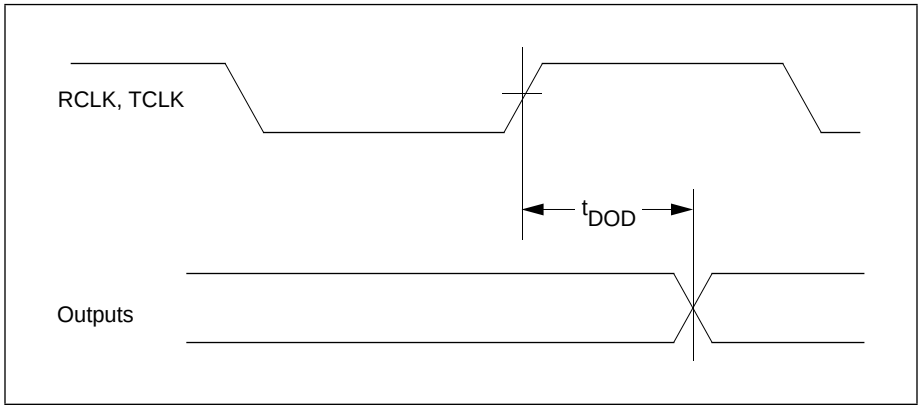


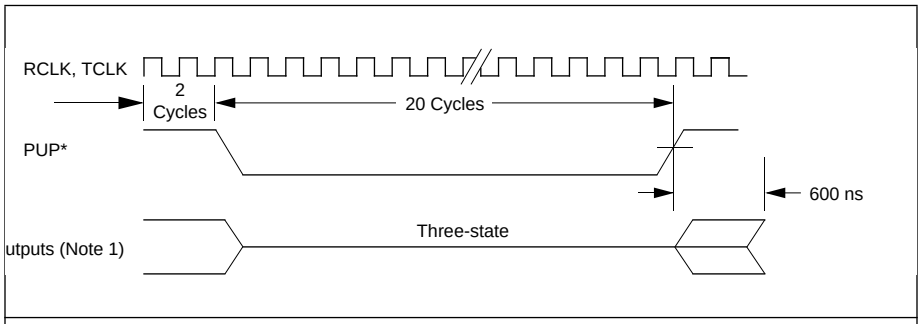
Figure 27. Output Data Delay Time



Reset Timing

See Figure 28

Figure 28. Minimum Reset Time



Notes: (1). Internal registers require 128 TCLK cycles after PUP* goes low to reach default (all zeros) state.

Reframe Time

See Table 10.

Table 10. Reframe Timing

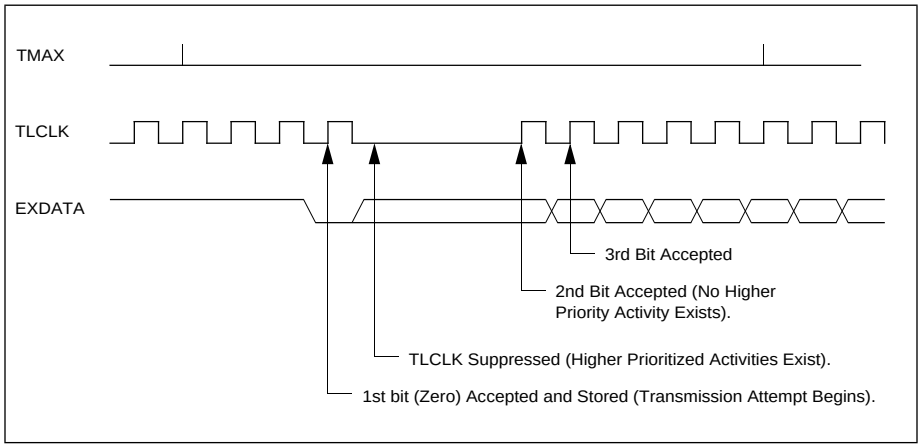
Mode	Minimum	Average	Maximum	Unit
SF	1.0	1.6	2.2	ms
ESF	4.5	6.7	8.5	ms
N	1.5	2.7	3.8	ms

Notes:
1. Times are for worst case average reframe.
2. Times do not include multiframing.
3. Maximum times are for 99th percentile.

Extracted Link DataTiming–ESF Mode

See Figure 29.

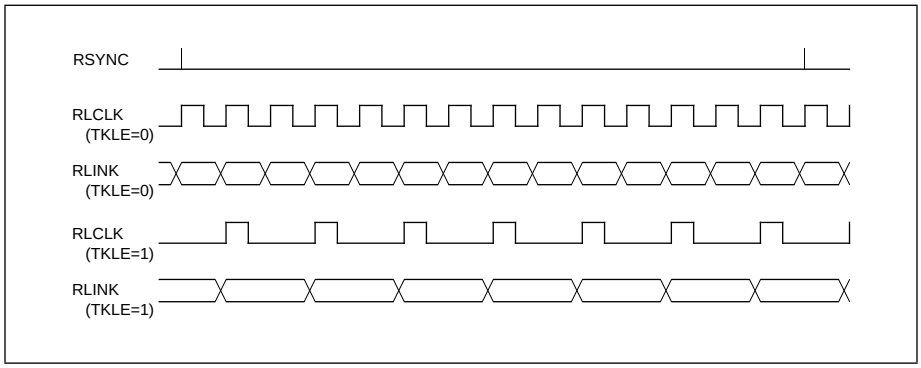
Figure 29. Extracted Link Data Timing–ESF Mode



Receive Link Data Timing–ESF Mode

See Figure 30.

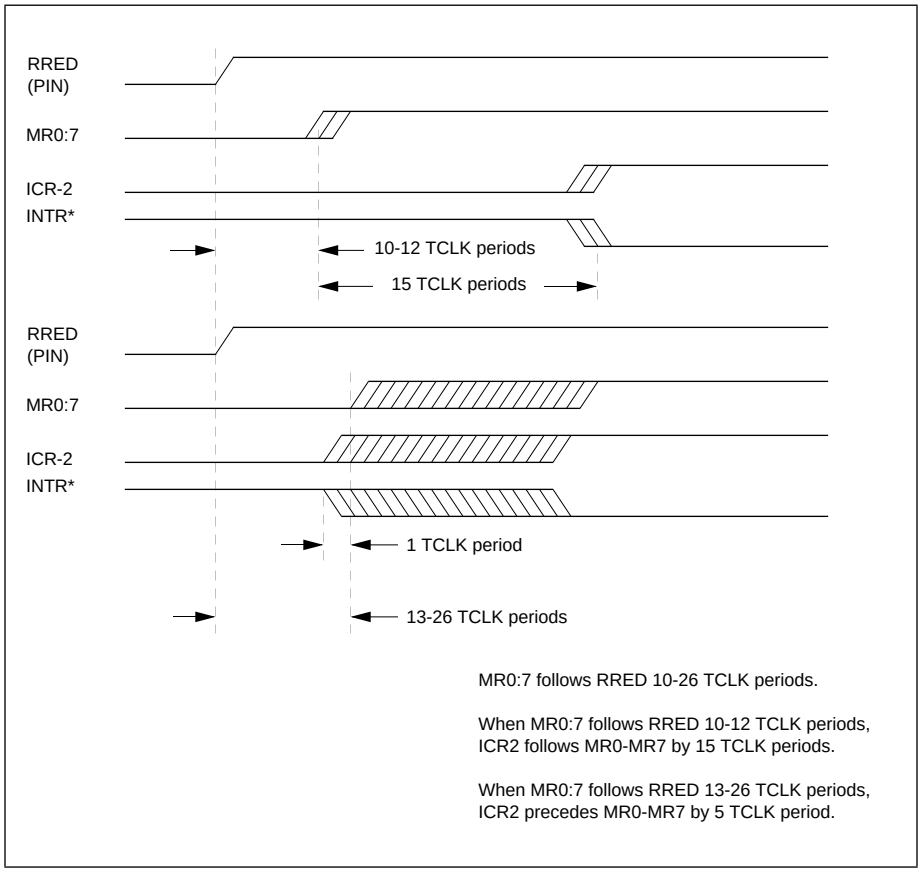
Figure 30. Receive Link DataTiming–ESF Mode



Alarm-to-Interrupt Delay

See Figure 31.

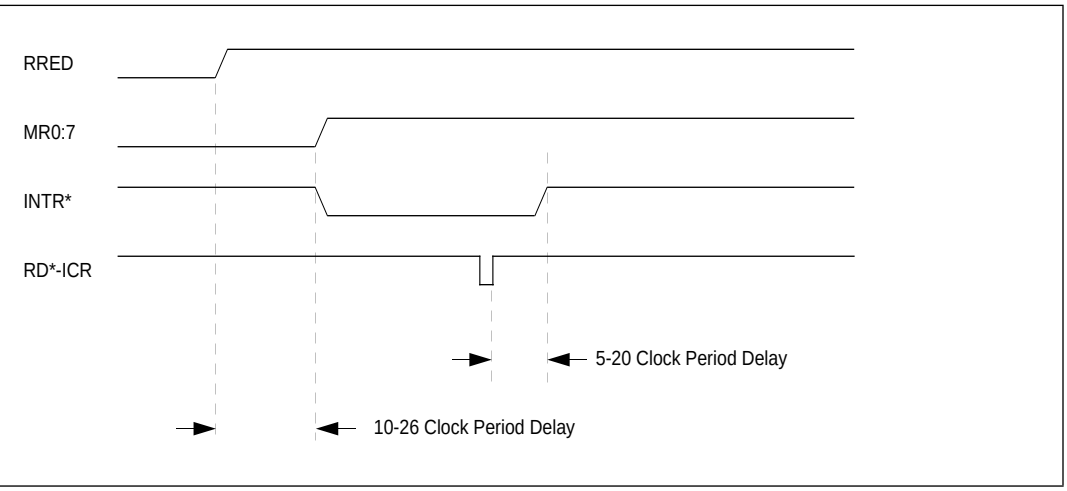
Figure 31. Alarm-to-Interrupt Delay



RRED Interrupt—MPU Read and Clear

See Figure 32.

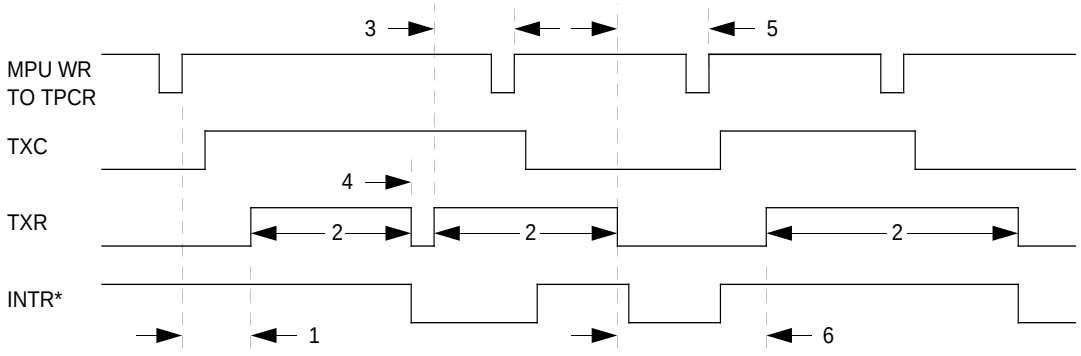
Figure 32. RRED Interrupt–MPU Read and Clear



Transmit Priority Codeword Response Timing

See Figure 33.

Figure 33. Transmit Priority Codeword Response Timing



1	Codeword response accepted	10 µs – 20 µs
2	Codeword transmitting pulse width	40 ms min. (less if truncated by yellow alarm)
3	Codeword request removed	0 µs min.
4	Back-to-back codeword TXR min. separation	10 µs – 30 µs.
5	Last chance request for back to back	210 µs max.
6	Back-to-back codeword TXR max. separation	240 µs max.

Absolute Maximum Ratings

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	Vdc
Input Voltage	V_{IN}	–0.3 to VCC + 0.3	Vdc
Output Voltage	V_{OUT}	–0.3 to VCC + 0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

Note: Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Electrical Characteristics

V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise specified

Table 12. Electrical Characteristics

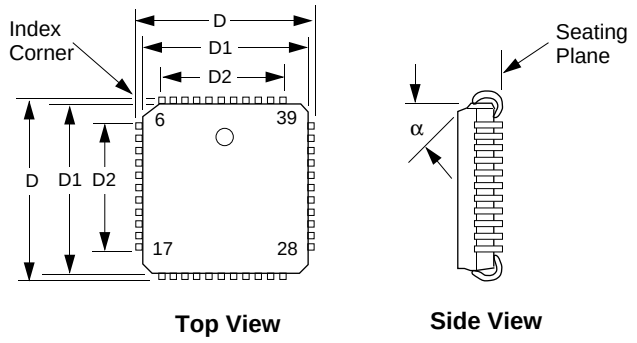
Parameter	Symbol	Min	Typ	Max	Units	Test Condition
Input Low Voltage	V_{IL}	–0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}	–	–	+0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage	V_{OH}					
TTL		+2.4	–	–		I_{LOAD} = 1.6 mA(1)
CMOS		+3.5	–	–		I_{LOAD} = –100 µA
Supply Current	I_{CC}	–		15	mA	(2)
Input Leakage Current	I_{LI}	–10	–	+10	µA	0 V ≥ V_{IN} ≥ V_{CC}
Output Leakage Current	I_{CO}	–10	–	+10	µA	0 V ≥ V_{IN} ≥ V_{CC}
Input Capacitance	C_{IN}	–	–	5	pF	(3)
I/O Capacitance	$C_{I/O}$				pF	(3)
Output Capacitance	C_{OUT}				pF	
AD0–AD7		–	–	100		
All others		–	–	50		
Power Dissipation	P_D	–	–	80	mW	

Notes: (1). All outputs except INTR*, which is open collector.
(2). TCLK = RCLK = 1.554 MHz, outputs open, $V_{IN} = V_{CC}$ or GND, T_A = 25° C, V_{CC} = 5.25 V.
(3). Characterization conditions are: a) Frequency = 1 MHz; b) Unmeasured pins are at GND; c) V_{IN} = +5 V or GND.

Package Information

Mechanical Drawings

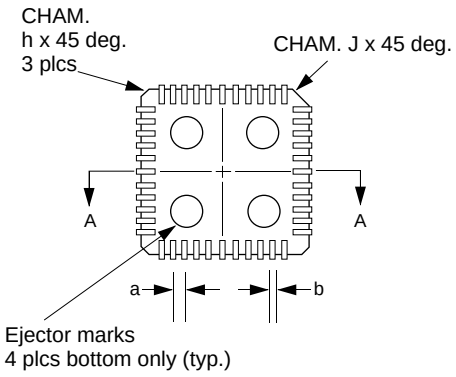
Figure 34. 44-Pin Plastic Lid Chip Carrier (PLCC) Package



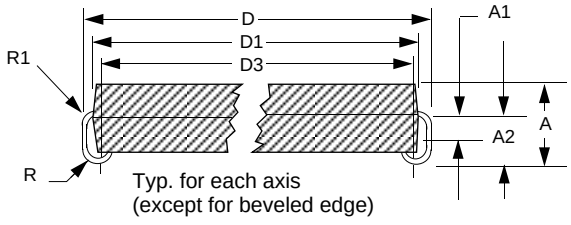
Top View

Side View

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
REF: PD44J/GP00-D166				

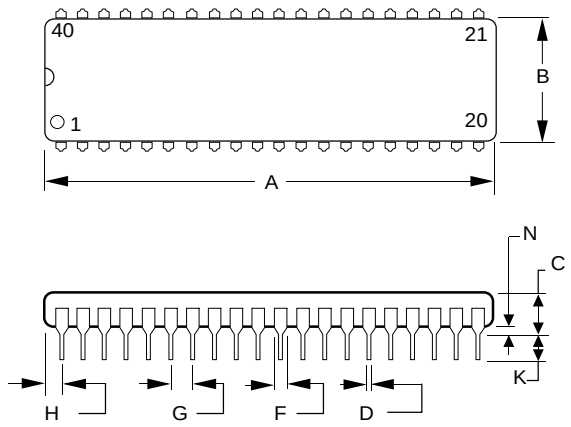


Bottom View



Section A-A

Figure 35. 40-Pin Plastic Dip



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	51.82	52.32	2.040	2.060
B	13.72	13.97	0.530	0.550
C	3.52	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040
REF: PD40P/GP00-D135				

Revision History

Revision	Changes From Previous Revision
A	Initial Release.
B	In the Internal Registers section under LOST on page 37, second sentence changed to read: A loss-of-carrier occurs when *neither* RPOS or RNEG receives a high-level input for 31 consecutive bit times. In Appendix A, Table A-2 on page 80, FLD2 for Frame Number 9 changed from n to –.

Appendix A

TI Overview

General

Information in this appendix is extracted from ANSI T1.403-1989 and applicable sections of CCITT G.704.

Prior to transmission, each voice circuit is sampled at 8 kHz using an 8-bit μlaw companding analog-to-digital converter. The resulting 64 kbps (8 bits x 8 kHz) signal is time-division multiplexed with 23 other sampled channels to produce a frame of 192 bits (24 channels x 8 bits). An extra bit (193rd bit or F-bit) is inserted at the beginning of each frame to define the frame boundaries. Since each voice circuit is sampled at 8 kHz, the frame rate is 125 μs microseconds. To transmit 193 bits in 125 μs requires a bit rate of 1.544 Mbps; hence, the standard T1 clock frequency of 1.544 MHz.

Signalling Data

Signalling data, such as on-hook and off-hook conditions, pulse dialing digits, call setup control, etc. associated with each voice circuit can be transmitted within the voice channel itself. This is known as channel-associated signalling (CAS), as opposed to common channel signalling (CCS), where a single (common) channel is dedicated to carry the signalling data for all the channels.

The signalling data, known as A-bits and B-bits, can be conveyed in the eighth bit position (least significant bit) of each channel. This signalling method is also known as robbed-bit signalling, since the A-bits and B-bits actually displace the original LSB of the voice signal, causing a slight, but insignificant, error in the received signal, imperceptible in voice applications but unacceptable in data applications.

Alarms and Error Conditions

In addition to voice and signalling data, T1 defines several alarm and error conditions that must be monitored and reported. The principal alarms are:

1. Red Alarm
2. Yellow Alarm
3. Blue Alarm (AIS)

A red alarm is produced by a receiver to indicate that it has lost frame alignment. A yellow alarm is returned to the transmitting terminal to report a loss of frame alignment at the receiving terminal. Normally, the MPU will use the receiver's red alarm to indicate that a Yellow Alarm should be transmitted. A Blue alarm, or Alarm Indication System (AIS), is sent as an unframed all-ones condition in the T1 bit stream.

Other error conditions are:

1. Loss of carrier
2. Bipolar violation

A loss of carrier indicates that the received data was zero for 31 consecutive bits. A bipolar violation is a failure to meet the Alternate Mark Inversion (AMI) line code of T1. AMI dictates that ones (marks) are transmitted alternately as positive and negative pulses; zeros are transmitted as zero volts.

Clock Recovery

In order to guarantee adequate clock recovery from the received data, a minimum “ones density” must be observed. B8ZS or bit-7 stuffing methods may be used. B8ZS represents a group of 8 zeros by substituting a predefined code that includes intentional bipolar violations. At the receiver, the code is recognized and the original 8 zeros are restored. The older method of bit-7 stuffing forces bit 7 to a one in an otherwise all-zero channel. This forced one is not coded as a bipolar violation, and the original data cannot be recovered by the receiver.

The BtT9170 supports all major requirements of the T1 system, including channel data recovery, signalling, alarm indication, error reporting, and both methods of zero suppression to satisfy the ones-density requirement.

The three major T1 formats supported by BtT9170 are:

1. Superframe Format (SF)
2. Extended Superframe Format (ESF)
3. Nonsignalling Format (N)

Superframe Format (SF)

The format, SF, is also referred to as the D4 format (Figure A-1).

The requirement for associated signalling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF). (See Table A-1.)

To recap, the SF structure consists of a multiframe of 12 frames; a frame of 24 channels, plus an F bit; and 8 bits per channel, where a channel is equivalent to one voice circuit or one 64 kbps data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating zeros and ones (101010) in odd frames that defines the frame boundaries so that one channel may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

Figure A-1. TI Super Frame PCM Format

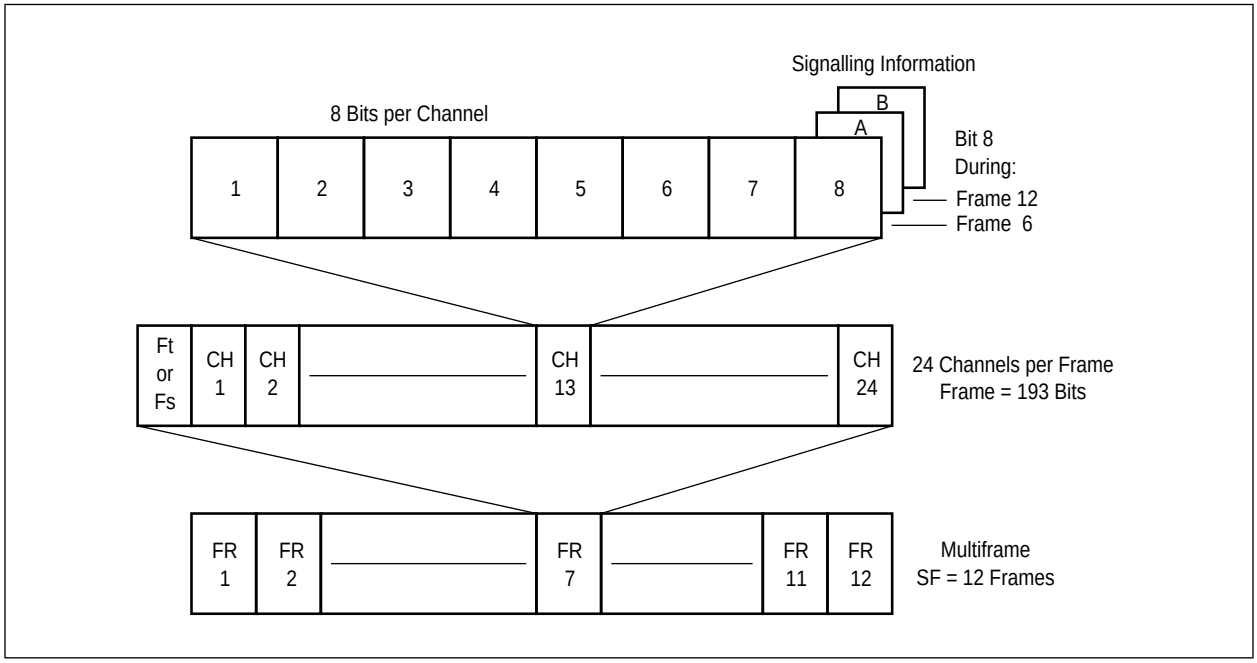


Table A-1. F-Bit Assignment–SF Mode

Frame Number	Bit Number	F-Bit	
		F_s	F_t
1	0	–	1
2	193	0	–
3	386	–	0
4	579	0	–
5	772	–	1
6	965	1	–
7	1158	–	0
8	1351	1	–
9	1544	–	1
10	1737	1	–
11	1930	–	0
12	2123	0	–

Notes: 1. F_s = Signalling Framing (Sequence . . .001110. . .)
2. F_t = Terminal Framing (Sequence . . .101010 . . .)

Extended Superframe Format (ESF)

In ESF (Figure A-2), the multiframe structure is extended to 24 frames (Table A-2). The channel structure is identical to the D4 (SF) format. Robbed-bit signalling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit), and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS) which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL) which allows data such as error performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC) which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

The BtT9170 supports the requirements of ESF, including channel data recovery, signalling, alarm indication, handling of the FDL information performance reporting priority codewords, extracted link data, and both methods of zero suppression satisfying the ones-density requirement.

Figure A-2. T1 Extended Super Frame PCM Format

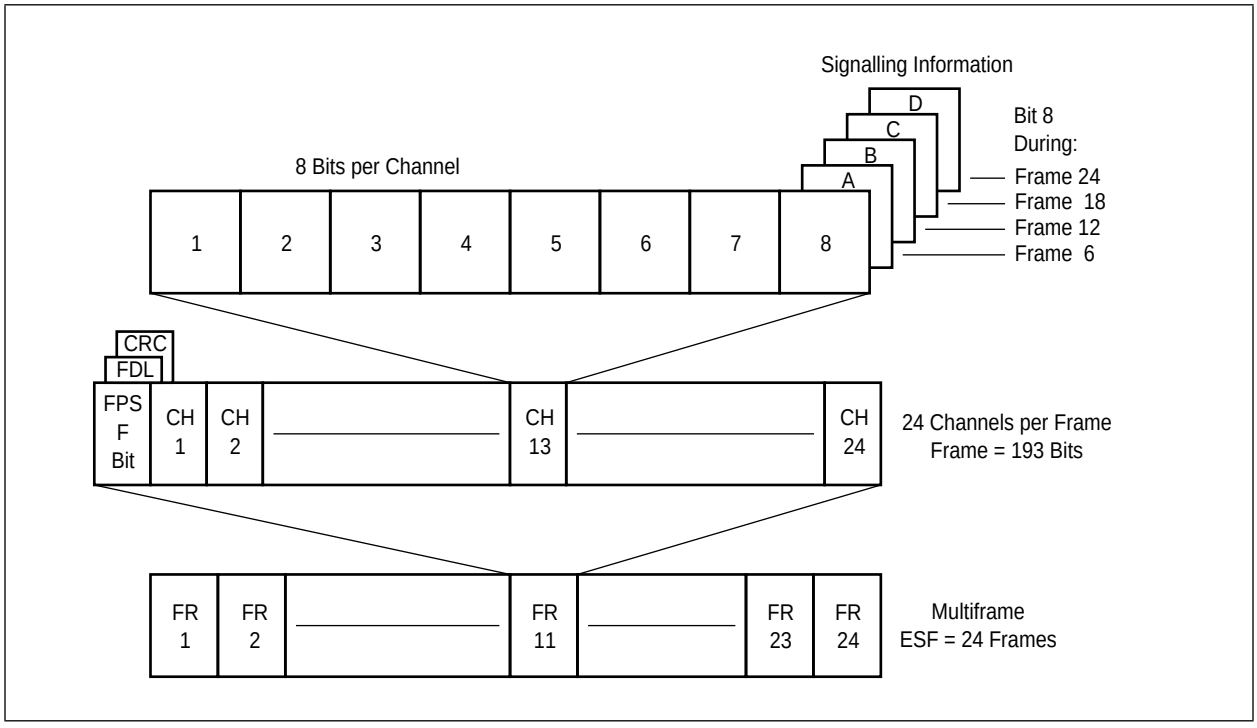


Table A-2. F-Bit Assignment–ESF Mode

Frame Number	Bit Number	FPS	F-bit Assignment		
			FDL1	FDL2	CRC
1	0	–	m	–	–
2	193	–	–	–	CB1
3	386	–	m	n	–
4	579	0	–	–	–
5	772	–	m	–	–
6	965	–	–	–	CB2
7	1158	–	m	n	–
8	1351	0	–	–	–
9	1544	–	m	–	–
10	1737	–	–	–	CB3
11	1930	–	m	n	–
12	2123	1	–	–	–
13	2316	–	m	–	–
14	2509	–	-	–	CB4
15	2702	–	m	n	–
16	2895	0	–	–	–
17	3088	–	m	–	–
18	3281	–	–	–	CB5
19	3474	–	m	n	–
20	3667	1	–	–	–
21	3860	–	m	–	–
22	4053	–	–	–	CB6
23	4246	–	m	n	–
24	4439	1	–	–	–

Notes:
1. FPS = Framing Pattern (Sequence . . . 001011 . . .)
2. FDL1 = 4 kbps Facility Data Link (message bits m)
3. FDL2 = 2 kbps Facility Data Link (message bits n)
4. CRC = CRC-6 Cyclic Redundancy Check (check bits CB1–6)

Nonsignalling Format (N)

This is a simpler version of the SF format. In this format, the Fs bits can be used as a 4 kbps data link for proprietary applications in which robbed-bit signalling is not required. The N format involves four frames per multiframe as depicted in Table A-3.

Table A-3. F-Bit Assignment–N Mode

Frame Number	Bit Number	F-Bit	
		F_s	F_t
1	0	–	1
2	193	X	–
3	386	–	0
4	579	X	–
Note: F_t = Terminal Framing (Sequence ... 101010 ...)			

Appendix B

Facility Data Link (FDL)

The information in this appendix applies only to ESF mode and is extracted from ANSI T1.403-1989.

Bit-Oriented Data (Priority Codeword)

Bit-oriented data is classified into either priority codeword or command/response information. Priority codeword information has the highest priority among all FDL information. Priority codeword information indicates a condition that is affecting the quality of the service, such as yellow alarm. Priority information may be interrupted by software for 100 milliseconds to send maintenance commands. Command/response information is sent by transmitting a minimum of 10 repetitions of the appropriate codeword pattern.

Command/response bit-oriented data transmission initiates action at the remote end. The remote end will respond by sending bit-oriented response message(s) to acknowledge the received commands.

The format of the bit-oriented information is:

MSB LSB
↓ ↓
0XXX XXX0 1111 1111

where the rightmost bit is transmitted first.

The bit-oriented information is also known as codewords. Specific assigned codewords have been specified in documents such as ANSI T1.403-1989 to specifically perform certain functions.

Message-Oriented Data (Performance Reports)

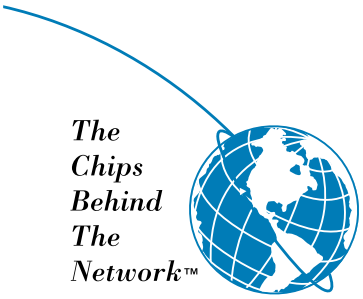
Message-oriented data carries performance information. The status of the transmission quality is reported after each 1-second interval. The performance report is made up of 14 bytes of data. Of these 14 bytes, bytes 1-4 and 13-14 are the performance-report message header, and bytes 5-12 contain data regarding the four most recent 1-second intervals. Error status regarding the events are transmitted for each 1-second interval.

1. **CRC-6 Block Errors**. A CRC-6 block error occurs when a CRC-6 code received from the far end is not identical to the corresponding CRC-6 calculated in the near end.
2. **Severely Errored Framing Event**. A severely errored framing event is the occurrence of two or more framing bit pattern errors within any 3 millisecond period. Contiguous 3 millisecond intervals are examined. The interval may or may not coincide with the frame/multiframe boundaries of the ESF.
3. **Frame Synchronization Bit Error Event**. This event is the occurrence of a Framing Bit Pattern (FPS) error.
4. **Line Code Violation Event**. This event is a bipolar violation of the incoming data. Bipolar violations due to proper operations of B8ZS coding are not counted as line code violation events.
5. **Controlled Slip Event**. This event is a replication or deletion of one or more complete frames by the receiving terminal.

Other information recorded every second is:

1. **Payload Loopback Activated**. This bit informs the receiver that a payload loopback is currently operating.
2. **U1, U2, and R Bits**. These bits are yet to be standardized and default to zero.
3. **Counter Bits**. These 2 bits are used to tag the 1-second interval recorded data to aid the receive end in determining if any report is missing. This is implemented by a modulo-4 count.

A performance report is transmitted every second on the facility data link (unless it is preempted by higher priority FDL messages) and is formatted as depicted in Figure 8, based on information contained in the near-end monitor registers (NEMR1–NEMR6). Message-oriented information received from the distant transmitter is also accessible through the far-end performance registers (FEPR1–FEPR8).



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