Bt8510

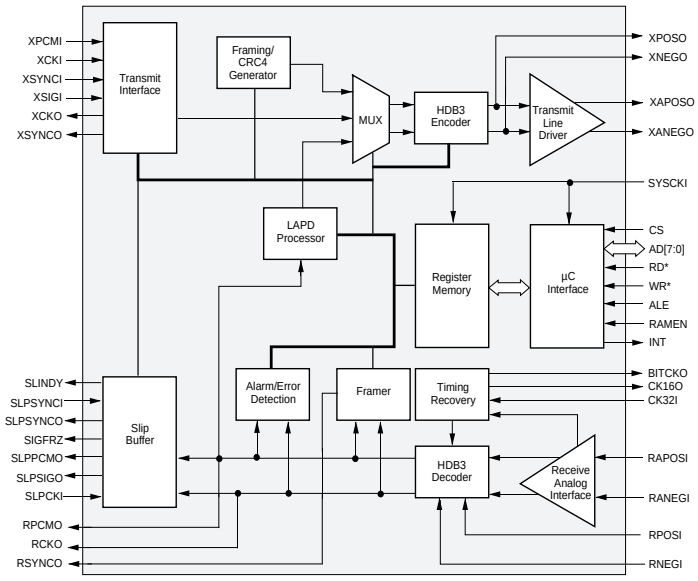
E1 Controller With Physical Line Interface

The Bt8510 is a highly integrated E1/CEPT transceiver that performs framing, control, and monitoring of E1 and Integrated Services Digital Network (ISDN) Primary Rate signals operating at 2.048 Mb/s. The Bt8510 is compatible with popular E1/CEPT framing standards such as ITU-T Recommendations G.704 (PCM-30), G.732 (CAS), and G.706 (CRC-4). The two-frame Pulse Code Modulation (PCM) slip buffer adapts the receive clock and data directly to the system serial bus timing. The signaling buffer provides signaling state freeze as well as resychronization to the system multiframe timing. The integral physical line interface features an adaptive analog receiver for clock and data recovery and a transmit line driver with pulse shaping (per G.703) for connecting to 75 or 120 Ω cables via external transformers.

Comprehensive ISDN D-channel support is provided for Time Slot 16 (TS16) via an integral LAPD controller with separate 16-byte transmit and receive buffers. The LAPD controller features zero stuffing and removal, flag and abort sequence detection and generation, and 16-bit Frame Check Sequence (FCS) generation and detection. Common Channel Signaling (CCS) or unformatted data may be processed through this buffer as well.

A parallel 8-bit microprocessor interface permits access to a series of 8-bit registers for control, error and alarm monitoring, and data link supervision. Error counters accumulate line code violations and CRC-4 and Frame Alignment Signal (FAS) errors. Access to Sa-bits and Far-End Block Error (FEBE) bits is provided for both transmit and receive directions. Per-channel control includes idle code word insertion, signaling insertion, and DS0 loopbacks to the network and equipment sides.

Functional Block Diagram



Distinguishing Features

- Highly integrated E1/primary rate controller (2.048 Mb/s)
- Frames to E1/CEPT formats
  - ITU-T G.704 (PCM-30)
  - ITU-T G.732 (CAS)
  - ITU-T G.706 (CRC-4)
- On-board physical line interface
  - Receive clock and data recovery for up to 15 dB of cable attenuation
  - Transmit line driver with G.703 pulse shaping
  - Compatible with 75 and 120 Ω cables
- Two-frame slip buffer and rate converter
  - Slip frame deletion/repetition
  - Signaling freeze
- Compatible with the Bt8360 T1 controller (1.544 Mb/s)
- FEBE (E-bit) and Sa-bit access
- HDB3 zero-code suppression
- Parallel 8-bit microprocessor interface for control and status monitoring
- ISDN/Common Channel Signaling support
  - 16-byte transmit and receive buffers
  - Time Slot 16 LAPD processor
  - Transparent unformatted mode
- Programmable transmit and receive time slot indication signals
- Counters for LCV, CRC-4, FAS errors
- Extensive per-channel control
  - Programmable code word insertion
  - Signaling insertion and extraction
- Diagnostic loopbacks
  - Payload loopback to network
  - Per DS0 channel loopback to network
  - Local loopback to equipment side

Applications

- PCM Digital Switches
- E1 CSU/DSUs
- E1/E3 Multiplexers
- Digital Access Cross-connect Systems ISDN Primary Rate Access Ports
- SDH Add/Drop Multiplexers
- ATM Switches/Multiplexers

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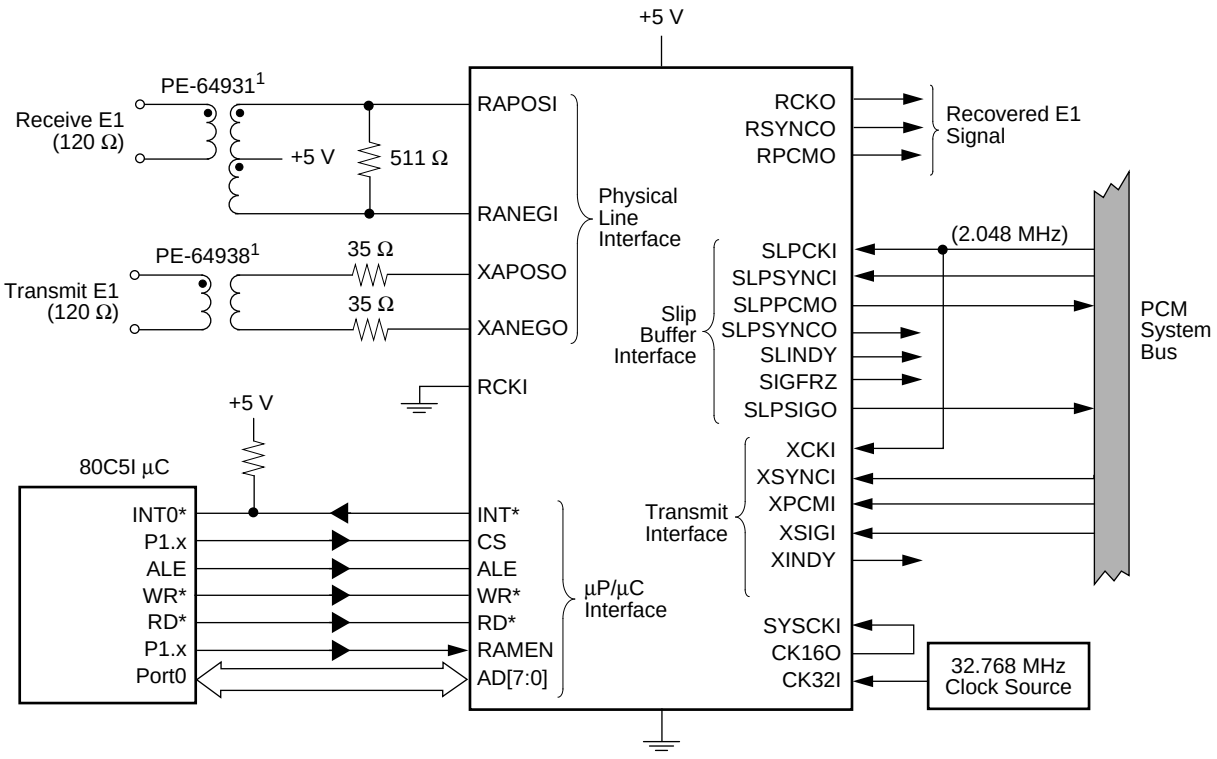
Ordering Information

Model Number	Package	Ambient Temperature Range
Bt8510EPJC	68-Pin Plastic Leaded Chip Carrier (J-Bend)	–40˚ to +85˚ C

Bt8510 Typical Application (Simplified Schematic)



Note 1: Available from Pulse Engineering, San Diego, CA.

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Product Description

Features and Modes of Operation

This specification describes the Bt8510 E1 (often called CEPT or DS1A) frame synchronization, signal generation, and recovery circuit for application in digital terminal interfaces operating at 2.048 Mb/s. Applications for this device include digital cross-connect systems, digital loop concentrators, DCME equipment, customer premise multiplexers, network managers, and PBXs. The circuit operates with Integrated Services Digital Network (ISDN) primary rate digital streams operating at a data rate of 2.048 Mb/s according to ITU-T Recommendation G.703.

The E1 framer is designed to meet the basic requirements of ITU-T Recommendation G.704. It can be used in the development of equipment to conform with ITU-T G.703 (§ 6), G.704 (§ 2.3 and § 3.3), G.705 (§ 3), G.706, G.732, G.735, G.736, G.737, G.761, and G.823 (jitter tolerance).

The physical line interface is included on-chip, accommodating both 75 ohm and 120 ohm cables. Data and clock can be recovered from received signals with up to –12 dB (120 ohm cables) and –15 dB (75 ohm cables) of attenuation. The analog circuits in the physical line interface may be powered-down if unused. Digital logic-level inputs and outputs are also provided for this case.

For ISDN applications, additional functions are provided to meet the requirements of ITU-T I.431, I.604 and G.962. These functions include LAPD formatting in Time Slot 16 (TS16), full access to the Sa bits on a multiframe basis, line loopback, per-DS0 loopbacks, idle code word insertion, and comprehensive CRC-4 functions.

An off-line framer is provided in the receiver. The framer has an average reframe time to the Frame Alignment Signal (FAS) of about 1 ms. Separate multiframe synchronization circuits are provided in the receiver for recovery of received Channel Associated Signaling (CAS) and the CRC-4 multiframe signals. CRC-4 error checking is performed and Far-End Block Error (FEBE) bits are transmitted in accordance with G.706 if these modes are enabled.

Through an 8-bit parallel interface, an external microprocessor or microcontroller can monitor all status conditions, provide configuration control, and access signaling and PCM data. The processor interface uses a multiplexed address/data bus, and can be directly connected to Intel 8051 and Motorola 68HC11 microcontrollers, without glue logic.

Individual 16-byte buffers are provided for both transmit and receive data in Time Slot 16 (one 16-byte buffer per direction). In CAS mode, this corresponds to a full multiframe. In LAPD mode, this may only be a partial message (multiframe synchronization is irrelevant). LAPD flag generation and detection (idle and abort bytes), FCS generation and checking, and zero stuffing and removal are provided. General-purpose unformatted data may be processed through the TS16 buffers including Common Channel Signaling (CCS).

The Bt8510 provides for both transmit and receive synchronization to a multiframe reference. To enable received signal synchronization to a single clock reference, the receive circuitry provides slip buffers and signaling reinsertion. The slip buffer removes all input jitter because slip buffer outputs are synchronized to the local system clock. Signaling freeze is provided during an out-of-frame or -multiframe synchronization condition. This prevents updating of the received signaling bit register from TS16, unless framing is valid. An optional short-delay mode allows specialized use of the slip buffer for delay-sensitive applications such as wireless communication systems.

Fixed PCM idle codes can be optionally inserted in the transmitted PCM data stream from a buffer that is loaded by the host processor. Each of the 32 time slots in the E1 signal has a corresponding control word that allows the transmitted PCM to be set on a DS0 basis. This feature may also be used to insert errors in the transmitted framing pattern. CAS or CCS can be inserted via a 16-byte register that is optionally inserted into TS16, passed through from the Transmit PCM In pin (XPCMI), or inserted serially onto an external pin (XSIGI). This per-channel control word is also used to control the transmit time slot indication signal (XINDY).

Received CAS is recovered from TS16 and loaded into the receive TS16 signaling buffer. This buffer has two multiframes of memory that allow the old signaling information to be retained in the event of an out-of-frame or multiframe synchronization condition. Signaling data is provided on an external pin (SLPSIGO) and also multiplexed in the full rate stream as it is received (it may also be read via the microprocessor port).

PCM insertion of a fixed data pattern is also provided in the receive PCM stream on a DS0 basis. Receive data and signaling insertion can be similarly provided on a per-channel basis.

The Alarm Indication Signal (AIS) consisting of all-ones may be inserted on the full E1 signal or in TS16 only.

Pin Descriptions

The Bt8510 is packaged in a 68-pin Plastic Leaded Chip Carrier (PLCC). Figure 1 illustrates the pinout. Pin assignments are listed in numerical order in Table 1. Figure 2 illustrates a functionally partitioned diagram of the Bt8510. Pin descriptions, labels, and I/O assignments are listed in Table 2. Unused inputs should be tied high or low to avoid floating inputs. No Connect (NC) pins should be left unconnected unless they are connected to signals to provide socket compatibility with the Bt8360 T1 Controller.

Figure 1. Bt8510 Pinout Diagram

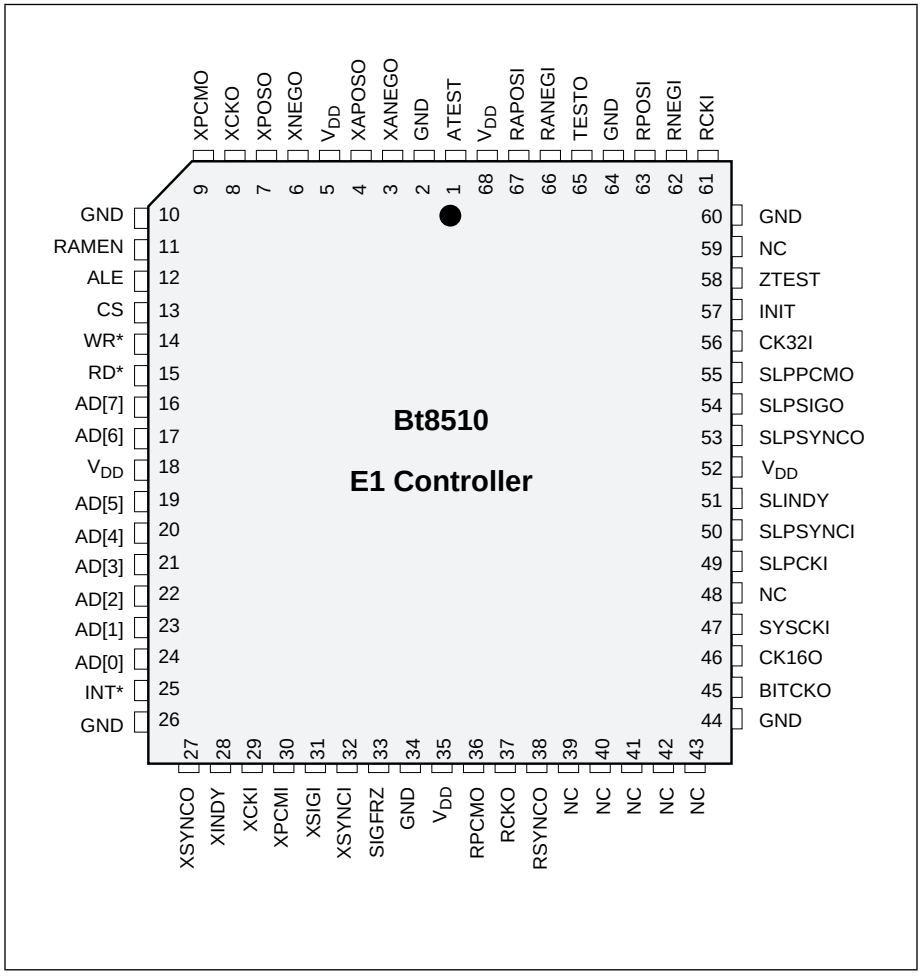


Table 1. Bt8510 Pin Assignments

Pin	Pin Label	I/O	Pin	Pin Label	I/O
1	ATEST	I	35	V_{DD}	I
2	GND	I	36	RPCMO	O
3	XANEGO	O	37	RCKO	O
4	XAPOSO	O	38	RSYNCO	O
5	V_{DD}	I	39	NC	—
6	XNEGO	O	40	NC	—
7	XPOSO	O	41	NC	—
8	XCKO	O	42	NC	—
9	XPCMO	O	43	NC	—
10	GND	I	44	GND	I
11	RAMEN	I	45	BITCKO	O
12	ALE	I	46	CK16O	O
13	CS	I	47	SYSCKI	I
14	WR*	I	48	NC	—
15	RD*	I	49	SLPCKI	I
16	AD[7]	I/O	50	SLPSYNCI	I
17	AD[6]	I/O	51	SLINDY	O
18	V_{DD}	I	52	V_{DD}	I
19	AD[5]	I/O	53	SLPSYNCO	O
20	AD[4]	I/O	54	SLPSIGO	O
21	AD[3]	I/O	55	SLPPCMO	O
22	AD[2]	I/O	56	CK32I	I
23	AD[1]	I/O	57	INIT	I
24	AD[0]	I/O	58	ZTEST	I
25	INT*	O	59	NC	—
26	GND	I	60	GND	I
27	XSYNCO	O	61	RCKI	I
28	XINDY	O	62	RNEGI	I/O
29	XCKI	I	63	RPOSI	I/O
30	XPCMI	I	64	GND	I
31	XSIGI	I	65	TESTO	O
32	XSYNCI	I	66	RANEGI	I
33	SIGFRZ	O	67	RAPOSI	I
34	GND	I	68	V_{DD}	I

Figure 2. Bt8510 Functional Pinout

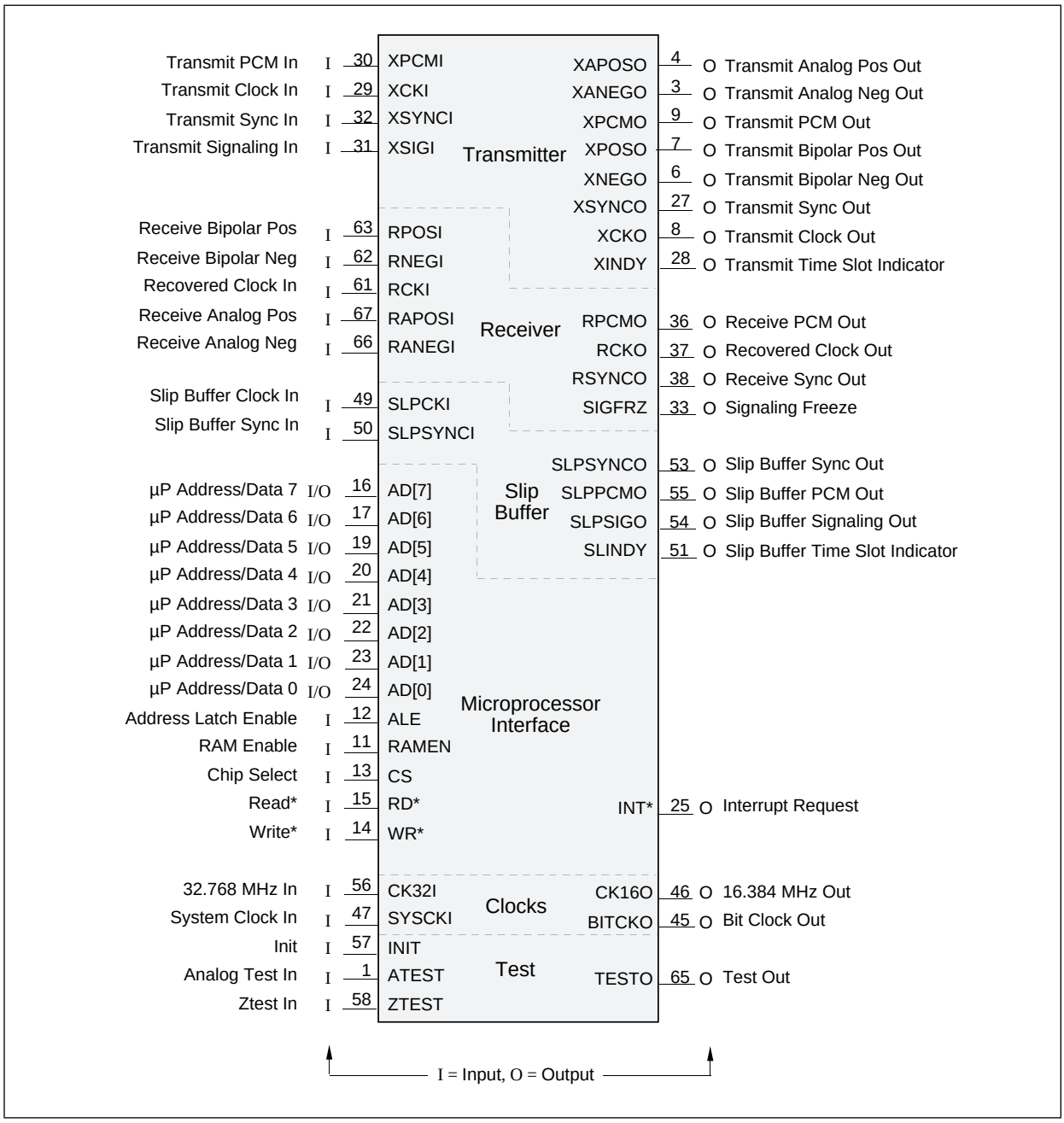


Table 2. Hardware Signal Definitions *(1 of 4)*

	Pin Label	Signal Name	I/O	Definition
Transmitter	XPCMI	Transmit PCM In	I	An input for unipolar transmit data. This data is sampled on the falling edge of the transmit clock, XCKI.
	XCKI	Transmit Clock In	I	The framer transmit clock, nominally 2.048 MHz. The Configuration Register [CR00;0x00] can substitute the receive clock for loopback operation.
	XSYNCI	Transmit Sync In	I	The rising edge establishes the transmit multiframe timing for CAS and the TS0 timing. The falling edge is not relevant, except that the period high and low must be at least one cycle of the transmit clock. This signal may be connected to ground, and the resulting multiframe timing will be indicated by XSYNCO.
	XSIGI	Transmit Signaling In	I	Can be used to insert CAS or CCS mode signaling into the transmit bit stream, rather than from XPCMI or from the internal time slot 16 signaling buffer (TXTS16;0xF0–0xFF).
	XPCMO	Transmit PCM Out	O	Output for the unipolar NRZ data. Data changes on falling edges of XCKO.
	XPOSO	Transmit Bipolar Positive Out	O	Positive NRZ bipolar output. This pin is usually connected to the positive bipolar data input of an external line interface circuit.
	XNEGO	Transmit Bipolar Negative Out	O	Negative NRZ bipolar output. This pin is usually connected to the negative bipolar data input of an external line interface circuit.
	XAPOSO	Transmit Analog Positive Out	O	Analog line driver output for positive pulses on the E1 line. This pin drives a transformer through a series resistor.
	XANEGO	Transmit Analog Negative Out	O	Analog line driver output for negative pulses on the E1 line. This pin drives a transformer through a series resistor.
	XSYNCO	Transmit Sync Out	O	Provides a transmit multiframe sync output. This signal will be derived from the frame sync input, XSYNCI. If XSYNCI is grounded, XSYNCO will free-run at a multiframe rate.
	XCKO	Transmit Clock Out	O	Repeats the transmit clock for timing the transmit outputs. If the receive timing is selected by the control register, that clock will be repeated here.
	XINDY	Transmit Time Slot Indicator	O	Indicates the input timing of those time slots programmed in the Transmit Per-Channel Control Registers [TXCR;0x10–0x1F].

Table 2. Hardware Signal Definitions *(2 of 4)*

	Pin Label	Signal Name	I/O	Definition
Receiver	RPCMO	Receive PCM Out	O	Recovered receive data output that is clocked out on the rising edges of RCKO. No insertion or buffering options are available.
	RCKO	Recovered Clock Out	O	The recovered clock from the internal digital phase-locked loop (DPLL). If internal clock recovery is not enabled, then the receive input clock (RCKI) is repeated.
	RSYNCO	Receive Sync Out	O	Receiver frame sync output. This output transitions high at the beginning of each 256-bit frame.
	RPOSI	Receive Bipolar Positive	I/O	Used as the positive pulse digital input from an external line interface circuit (TTL or CMOS logic-levels) if the internal analog interface is disabled. This input can also be used for unipolar data by grounding the RNEGI pin (or vice-versa). If the internal analog interface is enabled, this pin becomes an output for the positive bipolar pulses detected by the receiver.
	RNEGI	Receive Bipolar Negative	I/O	Used as the negative pulse digital input from an external line interface circuit (TTL or CMOS levels) if the internal analog interface is disabled. This input can also be used for unipolar data by grounding the RPOSI pin (or vice-versa). If the internal analog interface is enabled, this pin becomes an output for the negative bipolar pulses detected by the receiver.
	RAPOSI	Receive Analog Positive	I	Positive pulse from the line interface transformer. If the internal analog interface is disabled, this input should be tied to V_{DD}.
	RANEGI	Receive Analog Negative	I	Negative pulse from the line interface transformer. If the internal analog interface is disabled, this input should be tied to V_{DD}.
	RCKI	Recovered Clock In	I	Sourced by a line interface chip or local system. Optionally, internal timing recovery may be selected by setting the Enable Clock Recovery bit [EnClkRcv;CR00.0] in the Configuration Control Register [CR00;0x00], and supplying a 32.768 MHz clock to the CK32I pin.
	SIGFRZ	Signaling Freeze Active	O	When high, this output indicates the signaling freeze function is active. This signal is real-time and unlatched.

Table 2. Hardware Signal Definitions *(3 of 4)*

	Pin Label	Signal Name	I/O	Definition
Slip Buffer Interface	SLPPCMO	Slip Buffer PCM Out	O	Recovered receive data with slip buffer timing. Idle code, loop-back, and signaling extraction options are available. Synchronization is established by SLPSYNCI and SLPCKI. PCM-controlled frame slips will occur if there is a long-term variation between the slip buffer clock and the receive clock. A short delay mode is also available for delay-sensitive applications.
	SLPCKI	Slip Buffer Clock In	I	Used to read PCM data from the receive buffer memory, and to provide timing for SLPPCMO.
	SLPSYNCI	Slip Buffer Sync In	I	The rising edge on this pin establishes the multiframe sync reference by identifying the position of TS0, frame 0 for the slip buffer output. This input may be connected to ground, and the resulting multiframe timing will be indicated by SLPSYNCO.
	SLPSYNCO	Slip Buffer Sync Out	O	The rising edge indicates the position of TS0 in frame 0 of the multiframe in the slip buffer PCM output, SLPPCMO.
	SLPSIGO	Slip Buffer Signaling Out	O	CAS or CCS mode signaling information is repeated here twice per frame in serial fashion. The TS16 information is always output here in any signaling mode. If there is not a 16-frame signaling multiframe, this output can be ignored.
	SLINDY	Slip Buffer Time Slot Indicator	O	Indicates the output timing of those time slots programmed in the Receive Per-Channel Control Register [RXCR;0x00–0x0F].
Microprocessor Interface	AD[7:0]	Address/Data Bus	I/O	Multiplexed address and data bus to and from the host microprocessor or microcontroller.
	ALE	Address Latch Enable	I	Timing signal from the microprocessor that latches the address onto the multiplexed address/data bus.
	RD*, WR*	Read, Write	I	Active-low signals from the microprocessor that determine if the cycle is a read or write. If the RAMEN input is low, the control registers can be written or read and the status registers can only be read.
	RAMEN	RAM Enable	I	Directs read or write operations to the buffer memory if high. If low, only the control and status registers can be accessed.
	CS	Chip Select	I	Active-high signal from the microprocessor that selects the Bt8510 on a shared bus. If this signal is low, the framer will ignore any activity on the microprocessor bus.
	INT*	Interrupt Request	O	Active-low, open-drain output that interrupts the processor according to the selections made in the Interrupt Control Register [CR09;0x0F] and the Enable LAPD Formatting bit (EnLAPD-Fmt;CR01.7). The interrupt is cleared when the appropriate action has been taken.

Table 2. Hardware Signal Definitions *(4 of 4)*

	Pin Label	Signal Name	I/O	Definition
Clocks	CK32I	32.768 MHz Clock In	I	Drives the internal timing recovery circuit for the receive framer. If external clock recovery is provided, this input can be tied to ground or V_{DD}, or used to generate a system clock (CK16O) for connection to the SYSCKI input.
	SYSCKI	System Clock In	I	System clock for the integrated circuit that is required for any operation. The duty cycle must be 45% to 55%. The frequency must be in the range of 8.0 MHz to 20.0 MHz.
	CK16O	16.384 MHz Clock Out	O	32.768 MHz clock input (CK32I) divided by 2. This signal is present whenever the 32 MHz input is present. It can be connected to SYSCKI, if desired.
	BITCKO	Bit Clock Out	O	System clock (SYSCKI) divided by 8 that can be used as an input clock for the transmitter or slip buffer, as desired.
Test	ATEST	Analog Test In	I	Enables analog test mode. Used for device test only and should be tied to ground.
	ZTEST	ZTest In	I	Active-high input that turns off the AD[7:0] bus three-state outputs. It is used for device and automated board testing. It should be tied low for normal operation.
	INIT	Initialization	I	Active-high input that initializes the internal circuitry to a known state for device testing. It can also be used to synchronize multiple devices for use with a single microprocessor. If XSYNCI or SLPSYNCI are grounded, they will take their timing from the INIT reset pulse.
	TESTO	Test Out	O	Verifies correct operation of the analog interface circuitry during device testing. It is normally three-stated unless ATEST is high.
Power and Ground	V_{DD}	Power		Five pins are provided for power.
	GND	Ground		Seven pins are provided for ground.

Functional Description

Overview

A block diagram of the Bt8510 E1 transceiver is shown in Figure 3 and consists of three major sections: receiver, slip buffer and transmitter. The receiver is comprised of the analog receiver, the timing recovery circuit, the HDB3 decoder and the framer which recovers synchronization and detects alarms and errors. The receive bipolar input data can be obtained from either an external Line Interface Unit (LIU) chip, or by using the internal analog receiver and the timing recovery circuit which consists chiefly of a Digital Phase Locked Loop (DPLL). The analog receiver uses adaptive decision levels to allow for up to 15 dB of cable loss. After clock and data have been recovered, HDB3 decoding is performed to remove zero-code suppression and to convert the bipolar data into a single unipolar data stream. The resulting serial data is then checked by the framer for the G.704 Frame Alignment Signal (FAS), the G.732 Channel Associated Signaling (CAS) multiframe, and the G.706 CRC-4 multiframe, if present.

Errors and alarm status are reported in registers accessible by the microprocessor. Data in time slot 16 (TS16) is routed to the receive TS16 buffer (RXTS16;0x80-0x9F) for microprocessor access to CAS/CCS signaling bits or for processing of message-oriented signaling by the internal LAPD receiver. The recovered serial data stream is made available as unipolar NRZ data on the RPCMO output pin; the receiver sync output (RSYNCO) transitions low-to-high at the beginning of each frame. Data in each received time slot is also written to the internal buffer memory (RXLBUF, RXHBUF;0x40–0x7F) where it is read by either the slip buffer, the transmitter (for payload or per-channel loopbacks), or the microprocessor. Two complete frames of receive data, including TS0 and TS16, are kept in the buffer memory.

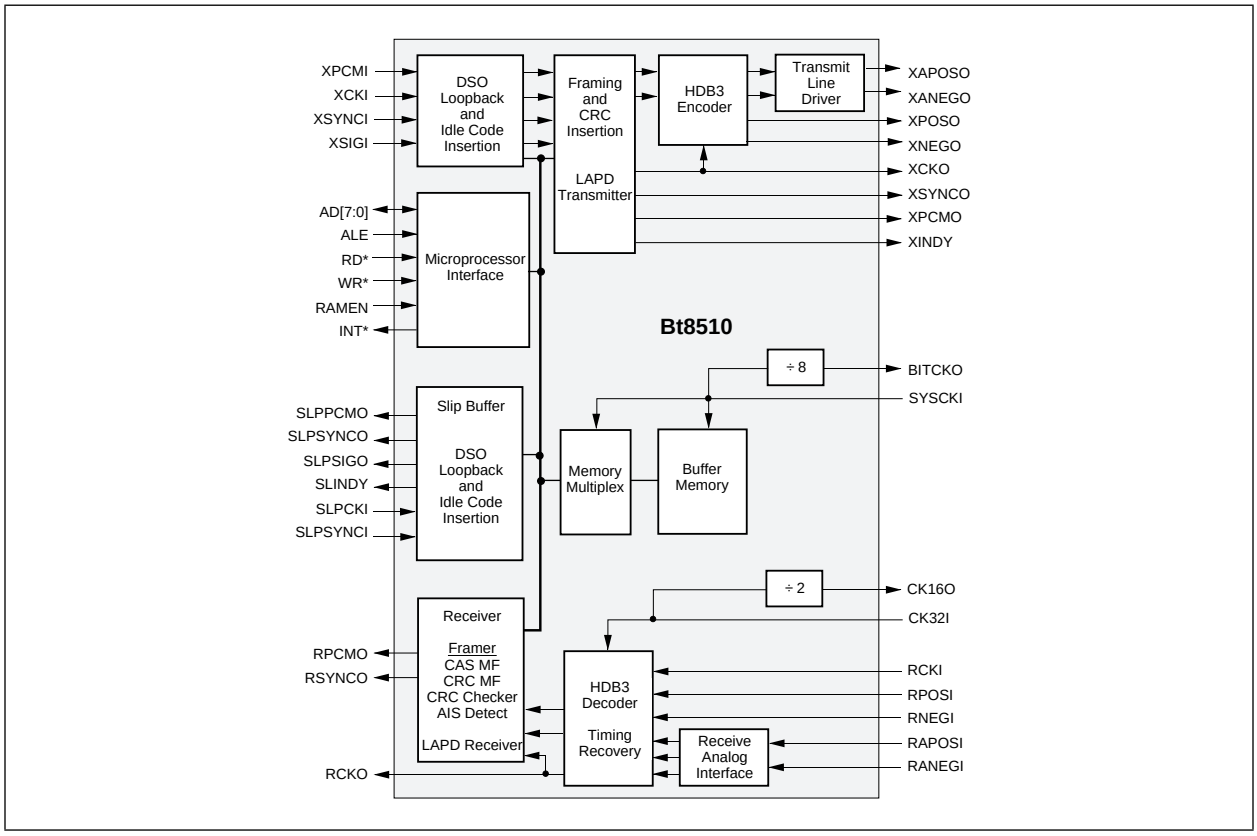
The slip buffer reads the appropriate data from buffer memory and assembles the serial output stream at SLPPCMO. Idle code insertion and loopback functions can be performed only on the slip buffer output. (The receive per-channel controls actually refer to the slip buffer.) Controlled frame slips are performed when the slip buffer skips or repeats a frame (256 bits) of the receive buffer memory. Signaling freeze is also performed here, again by redirecting buffer read operations (and disabling receive data write operations). The slip buffer sync output (SLPSYNCO) is a multiframe sync, and transitions low-to-high at the beginning of TS0, frame 0 of the 16-frame multiframe. This sync output is compatible with the transmit sync input, which allows the direct connection of the slip buffer output to transmit input. The slip buffer time slot indication signal (SLINDY) can be

programmed to indicate any number of time slots for each frame, a feature useful in drop-and-insert applications.

The transmitter section comprises of the DS0, loopback and idle word insertion block; the framing and CRC-4 coding insertion block; the HDB3 encoder; and the differential transmit line driver. Transmit serial data and clock from the host are applied to XPCMI and XCKI, respectively. PCM idle codes, payload loopback, and TS16 insertions are performed under microprocessor control. TS0 insertion data includes the FAS frame sync pattern, CRC-4 information and various reserved bits. TS16 insertion functions include the CAS signaling multiframe alignment pattern and transmit signaling bits. These signaling bits can be sourced from the transmit signaling input (XSIGI), from the buffer memory as microprocessor-supplied data, or embedded in the PCM input data stream at the XPCMI pin. Alternatively, TS16 can be used for transmitting LAPD messages using the internal LAPD transmitter; message data is supplied by the microprocessor via the Transmit TS16 Buffer (TXTS16;0xF0–0xFF). All framing and internal data insertion can be disabled to transparently transmit data. The transmit time slot indication signal (XINDY) can be programmed to indicate any number of time slots for each frame, a feature useful in drop-and-insert applications.

The composite serial data is then routed to the HDB3 encoder which performs zero-code suppression (can be disabled for sending AMI data) as well as conversion to a bipolar data stream. The transmit line driver then interfaces this signal to the physical E1 line via an external transformer and resistors. Compatible with 75 Ω and 120 Ω cables, the line driver performs the necessary pulse template shaping specified in ITU-T G.703. Transmit bipolar (XPOSO, XNEGO) and unipolar NRZ (XPCMO) outputs are also provided for use with an external line interface device.

Figure 3. Functional Block Diagram



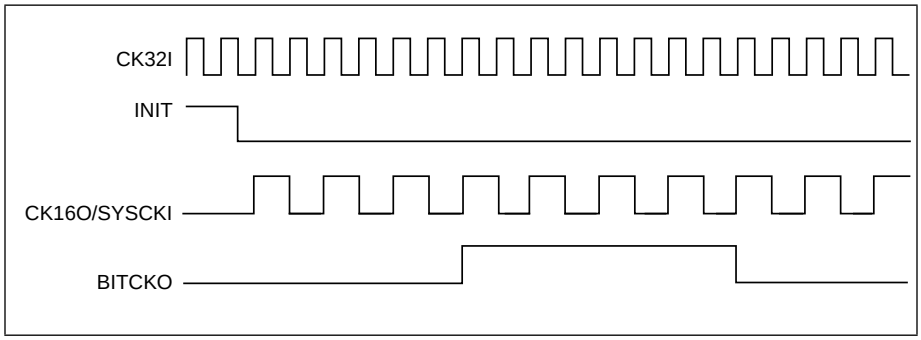
Clock Interface and Synchronization

The Bt8510 has both a 32.768 MHz timing recovery clock input (CK32I) and an 8 MHz to 20 MHz System Clock Input (SYSCKI). The 32.768 MHz clock must have a duty cycle between 25% and 75%, and be accurate to within 0.01%. SYSCKI must have a duty cycle between 45% and 55% and can be in the range of 8.0 MHz to 20.0 MHz. A faster system clock increases the maximum data rate between the microprocessor and the internal RAM memory but at the expense of increased power dissipation. CK32I is used internally only by the internal DPLL for receive clock recovery; if the receive clock recovery is not being used, CK32I is not required. This clock is also divided by 2 and is provided at the CK16O output pin. If present this clock may be connected to SYSCKI when receive clock recovery is enabled.

SYSCKI is further divided by 8 to obtain a 2.048 MHz clock that can be used for the transmit clock, if desired. This signal is provided at the BITCKO output and can be used for other clock inputs such as SLPCKI or XCKI. If a system clock frequency other than 16.384 MHz is used, then the BITCKO output is then SYSCKI divided by 8.

A timing diagram for the clock signals is shown in Figure 4. The initialization signal (INIT) is active-high, and can be used to synchronize the 16.384 MHz outputs for multiple Bt8510 devices on power-up.

Figure 4. Clock Signals



If several integrated circuits are to be synchronized, then the INIT and XSYNCI pins should be tied together. A common 32.768 MHz clock input (or 16.384 MHz clock input if the internal clock recovery is not used) can also be used. Such synchronization can make the collection of status information from a large number of Bt8510s faster and more convenient.

Microprocessor Interface

The framer is managed by an external microprocessor or microcontroller. An integral interface to an Intel 8051-type controller, a Motorola 68HC11-type controller, or equivalent, is provided. A circuit within senses which type of processor (Intel or Motorola) is being used and adjusts itself automatically.

The Bt8510 is connected to a microprocessor exactly like static RAM. Two different kinds of registers can be read or written. *Direct* read and write operations access control and status registers. *Indirect* read and write operations access the 256 bytes of buffer memory when RAMEN is high. These bytes contain information associated with each channel or timeslot of the E1 signal.

Control Interface

The control interface to the Bt8510 consists of 14 pins: Address Latch Enable (ALE), Read Enable (RD*), Write Enable (WR*), Chip Select (CS), RAM Enable (RAMEN), eight multiplexed address/data bits (AD[7:0]), and Interrupt (INT*).

The control interface is designed to allow the direct connection of an Intel 8051-type controller or equivalent, or a Motorola 68HC11-type controller or equivalent. The CS input to the Bt8510 allows the control of multiple devices from a single microprocessor or controller. INT* is used for signaling and monitoring operations. It is active-low, and stays low until the interrupt condition is cleared.

The type of processor used is automatically sensed by looking at the state of the RD* input when ALE is active (high). To use the Bt8510 with an 8051-type controller, connect ALE, WR*, and RD* of the 8051 to the corresponding inputs of the Bt8510. To use the Bt8510 with an HC11-type controller, connect AS of the HC11 to the ALE input of the Bt8510, Enable to RD*, and Read/Write to WR*. In both cases, the CS and RAMEN inputs can be driven by address lines or proper decodes of the address lines.

Detailed timing information is contained in the Electrical and Mechanical Specifications chapter.

Address Map

The register address map for the Bt8510 is given in the Register Summary section of the Registers chapter. There are three types of registers: Control Registers, Status Registers, and Buffer Memory Registers. Control and Status Registers are located at addresses 0x00–0x1F when RAM Enable (RAMEN) is low. Buffer Memory Registers are located at addresses 0x00–0xFF, and require RAMEN to be high. CS must be high to address any registers within the Bt8510.

Microprocessor Interrupts

One explicit interrupt signal (INT*) is provided and can be triggered by one or more sources: an LAPD interrupt, an end-of-multiframe signal, an out-of-frame (OOF) event or a saturation of one of the error counters. The Interrupt Status Register [SR13;0x1F] is provided to aid in determining the source of the interrupt. The Interrupt Control Register [CR09;0x0F] controls the masking of these interrupt sources.

The microprocessor can be interrupted by either the Transmit Multiframe Sync Output signal (XSYNCO) or the Slip Multiframe Sync Output (SLPSYNCO) connected to the interrupt input of the microprocessor. These interrupts can be used to synchronize read and write operations to properly inject and extract TS16 signaling data to and from TS16 buffer memory. If the LAPD formatting operation is enabled, it can interrupt the microprocessor via the INT* pin as well.

Depending on the options selected, an interrupt signal may have several different sources. In this case, the Interrupt Status Register must first be read to determine the source of the interrupt. The processor should be optioned for level-triggered interrupt operation.

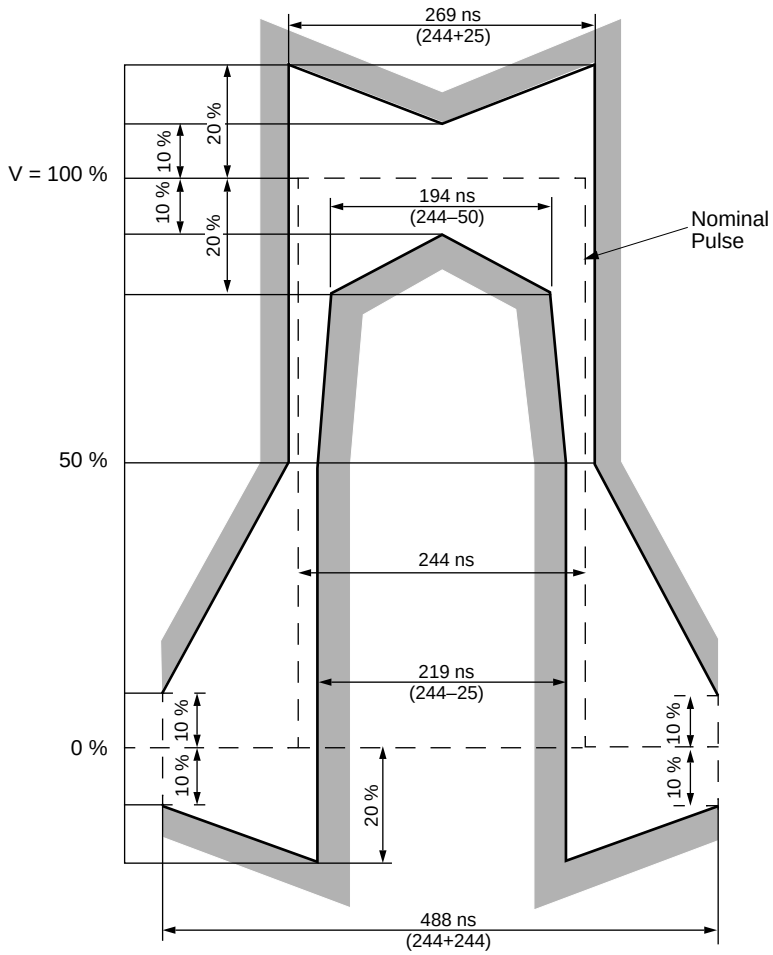
To process status interrupts, read the Interrupt Status Register at each interrupt. If the counter interrupts are enabled in the Interrupt Control Register, read the Framing Pattern Status Register [SR03;0x13] for overflow indications for the LCV, CRC, or FAS error counters. The interrupt condition will clear once this register has been read.

Line Interface

The receive analog interface allows direct connection to the physical E1 line via coupling transformers and two external terminating resistors. Line and local loopbacks are provided for maintenance purposes.

A pulse shaping, differential line driver is provided in the transmitter. This driver is always enabled; however, power drain will be negligible if the outputs are left open. Pulse shaping is performed internally so that with the recommended transformers and resistors, a transmitted signal will meet the pulse template requirements of ITU-T G.703 shown in Figure 5 (measured at the secondary side of the transformer with either a 75 Ω or 120 Ω termination). Refer to Appendices A, C and D of this document for more details about the transmit analog interface.

Figure 5. G.703 Isolated Pulse Template



Note: For 75 Ω Load Impedance: V = 2.37 V; 120 Ω Load Impedance: V = 3.00 V; Operating Data Rate = 2.048 Mb/s.

The analog receiver consists of input filters, adaptive decision thresholds, data slicers, and Loss of Signal (LOS) detection. The maximum sensitivity is –18 dB, although cable characteristics may require a receive equalizer to operate reliably at that level. In general, –12 dB is possible on 120 Ω ABAM cable, and –15 dB on 75 Ω coax, without external equalization. Note that the use of the analog receiver also requires the use of internal clock recovery. A power-down mode reduces power drain from 20 mA (typical) to 0.5 mA (max).

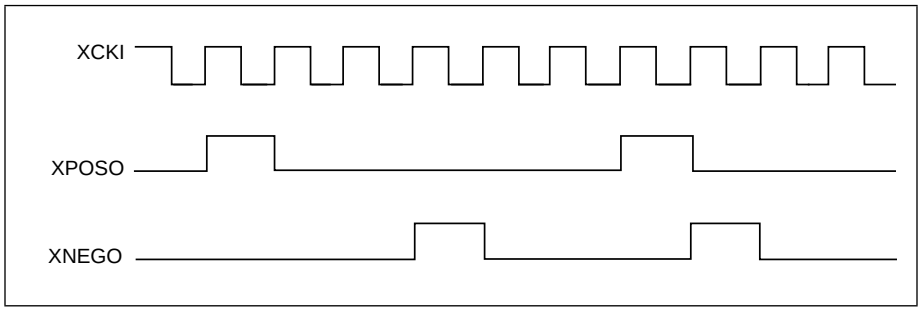
The transmit and receive *digital* interfaces allow connection of +5 V logic-level signals to and from other integrated circuits. The transmit digital interface includes the following logic-level signals: XPCMO (an output for transmit unipolar data), XCKO (the corresponding 2.048 MHz clock), and XPOSO/XNEGO (positive and negative full-width data outputs that may be connected to other physical line interface devices).

The receive digital interface includes the following logic-level signals: RPOSI/RNEGI (inputs for either full-width, clocked data or unclocked variable-width data) and RCKI (the corresponding clock for full-width data). A single unipolar data stream can be fed to either RPOSI or RNEGI as long as one of these two inputs is grounded. Two timing options are provided for the received E1 signals. The analog receiver may be configured via the Enable Clock Recovery bit (EnClkRcv;CR00.0) in the Configuration Register (CR00;0x00) for either clocked (external clock recovery) or unclocked (internal clock recovery) operation. In internal clock recovery mode, a high-performance DPLL adaptively divides the CK32I signal to match the phase and frequency of the incoming E1 signal. The resulting recovered clock samples the E1 signal for data recovery and is also used as write clock signal to the slip buffer and routed to the RCKO pin for use by the system.

Transmit Digital Line Interface

The transmit digital line interface signals are shown in Figure 6, illustrating a portion of a random data sequence (...01001001100...). Separate signal pins provide the appropriate output signal for positive and negative pulses. The outputs change on rising clock transitions of XCKI.

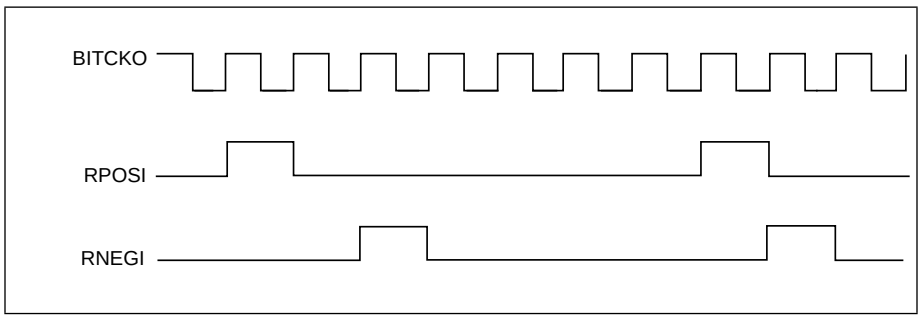
Figure 6. Transmitter Output



Receive Digital Line Interface

The receive digital line interface can be programmed for either clocked or unclocked operation. In clocked mode, an externally derived 2.048 MHz clock must be connected to RCKI. The input logic-level signal at RPOSI and RNEGI is internally sampled on the negative edges of RCKI as shown in Figure 7.

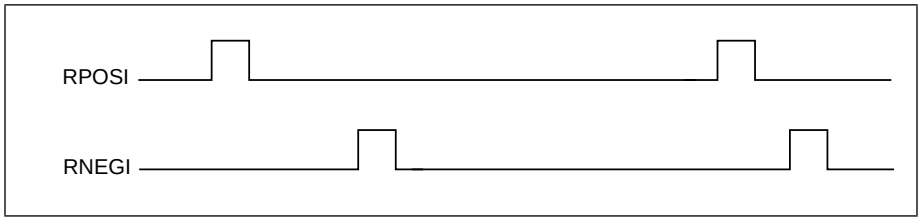
Figure 7. Clocked Receiver Input



If internal clock recovery is enabled (unclocked mode), the RCKI input is ignored, and the bipolar logic-level signals at RPOSI and RNEGI are sampled internally to recover clock and data. Each input pulse at RPOSI and RNEGI must have a duty cycle between 35% and 65%, as shown in Figure 8.

If desired, the receive input may be supplied as a unipolar data stream. In this configuration, the receive data must be clocked, and either the positive or negative input may be used (the unused input must be tied to ground). HDB3 decoding must also be turned off (EnAMI =1 in CR00.5) and the Line Code Violation Counter (SR10;0x1C) should be ignored.

Figure 8. Unclocked Receiver Input



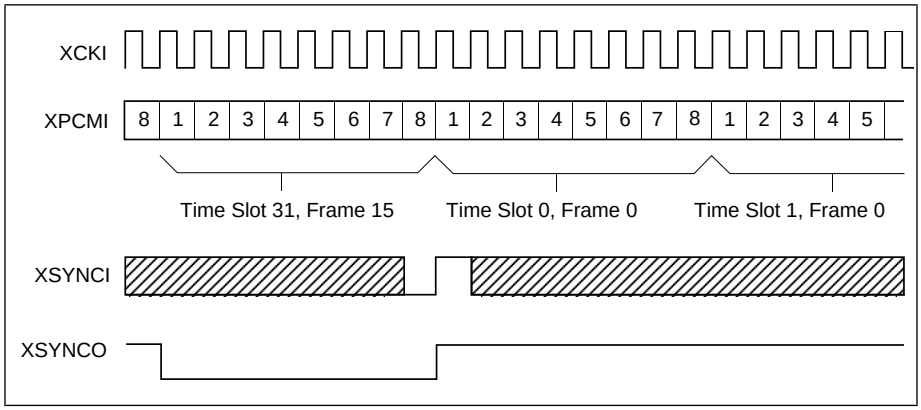
Transmitter Operation

Each transmitter circuit is synchronized to the transmit input data by an external synchronization signal (XSYNCI). This external synchronization signal sets the multiframe reference for transmitted signals.

Input and Synchronization

The transmit inputs for the system PCM bus interface consists of the unipolar transmit input signal (XPCMI), clock (XCKI), and synchronization (XSYNCI). A multiframe synchronization output is provided at XSYNCO. The timing for these signals is shown in Figure 9.

Figure 9. Transmitter Input Timing and Synchronization Output



The system-side data input at XPCMI is synchronized to both the input clock at XCKI and the multiframe synchronization signal at XSYNCI, which can be either externally provided or taken from the multiframe synchronization signal output by the Bt8510 at XSYNCO. The timing of the transmit signals relative to the multiframe is shown in Figure 9. The clock frequency is 2.048 MHz. All transmit system-side inputs are internally sampled on the falling edge of XCKI while the outputs are clocked out on the rising edge.

The transmit synchronization input (XSYNCI) should have a low-to-high transition from the last bit of the multiframe's last frame to the first bit of the multiframe's first frame. If a 2-frame versus 16-frame multiframe is used, the synchronization input can cycle every other frame; however, this will disable the XSYNCO output, and will also continuously reset the CRC-4 multiframe count sequence prematurely. The XSYNCI signal should not transition at a rate faster than every other frame since framing generation errors will result if the Insert Framing bit [InsFrm;CR00.2] of the Configuration Register is enabled.

An alternative method of synchronization is provided when XSYNCI is tied to ground and XSYNCO is used by the system to synchronize the transmit data supplied to XPCMI. XSYNCO then runs at an internally determined 16-frame multiframe rate (a divide-by-4096 of the XCKI clock).

Either of the multiframe synchronization outputs (XSYNCO or SLPSYNCO) can be used as an interrupt to indicate when the receiver status bits are updated. The multiframe synchronization signals transition low-to-high at the beginning of TS0, Frame 0 of the 16-frame multiframe.

Frame Alignment Signal and CRC Generation

The E1 framing insertion circuit includes three types of framing as specified in ITU-T G.704: basic frame alignment (FAS), CRC-4 multiframe alignment, and signaling multiframe alignment. While basic FAS framing is a requirement, the other types of multiframe alignment are optional and could be independent of each other. Signaling multiframe alignment is used only with Channel Associated Signaling (CAS) which employs time slot 16 to carry the signaling information for the 30 channels of PCM data. All automatic framing functions can be disabled in the following sections.

The G.704 E1 frame alignment signal (FAS) is automatically generated if the Insert Framing bit (InsertFrm;CR00.2) is set to a 1. The Sa-bits and the A-bit in TS0 of the Not-FAS frame may be programmed as desired in various control registers. If CRC-4 error checking and framing is desired, it must be enabled by setting the Insert CRC bit (InsertCRC;CR00.1) in the Configuration Register [CR00;0x00]. Automatic CRC-4 performance reporting (FEBE), using the two E-bits in the CRC-4 16-frame multiframe, may be enabled as well. Alternatively, TS0 patterns may be sourced directly from the XPCMI pin or read from the Transmit Idle Codes registers. In the latter case, the host processor would supply the desired TS0 data.

Transmit Per-Channel Idle Code Insertion

The Transmit Idle Code Registers (addresses 0xA0–0xB8) in buffer memory are used to transmit specific idle code ("idle code" refers to any user-specified, fixed data pattern) for each individual channel or time slot. The most significant bit of the register will be transmitted first. Setting the Insert Idle Code bit (InsertIdleTSn) for a specific time slot in the one of the appropriate Transmit Per-Channel Control Registers (addresses 0x10–0x1F) enables transmission in the E1 signal of the byte in the corresponding Transmit Idle Code Register. Therefore, each transmitted channel can contain a unique idle code pattern programmed by the host in lieu of normal PCM data traffic.

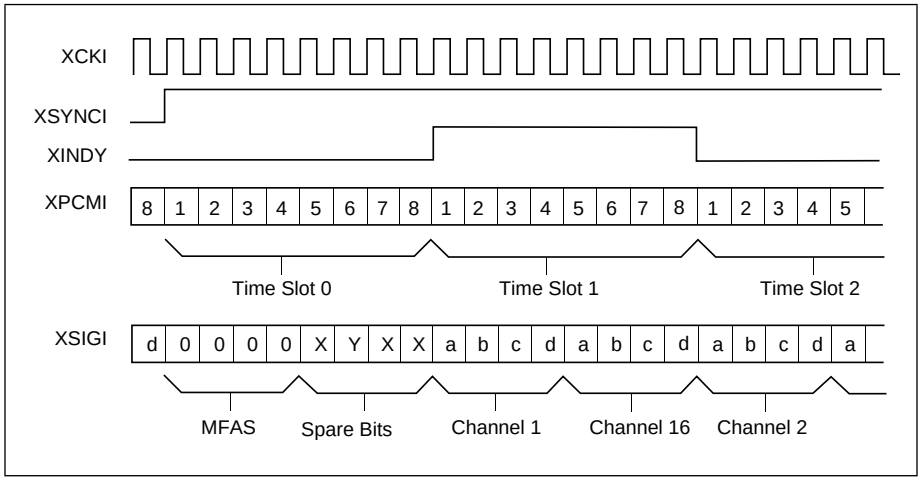
To insert user-specified framing patterns into TS0 from the Transmit Idle Code registers**,** the Insert Framing bit [InsFrm;CR00.2] of the Configuration Register must be cleared to 0 to disable internal framing bit generation.

External Signaling Insertion

Figure 10 illustrates the required timing for external transmit signaling insertion using the external signaling input (XSIGI). Signaling bits for each channel are grouped as 4-bit nibbles. Two signaling nibbles for a pair of PCM channels are required to be input in the same byte as shown. The first 16 time slots of the frame are used for all the signaling information. The bits to be transmitted in TS16 frame 0 are coincident with the TS0 time window, and so on until the signaling channels 15 and 30 are input coincident with the data for TS15. The signaling data *must* be repeated each frame, even though signaling only changes on a multiframe rate. XSIGI is ignored during the remaining 16 time slots of each frame (TS16-TS31).

To insert user-specified framing patterns into TS16 of frame 0 directly from the XSIGI pin, the Insert CAS Framing bit [InsCASFrm;CR02.0] must be disabled in the Time Slot 16 Control Register [CR02;0x02]. If InsCASFrm is enabled, both the CAS multiframe alignment signal and the Transmit X1 [TxX1;CR02.4], Transmit X3 [TxX3;CR02.6], Transmit X4 [TxX4;CR02.7] and Send Multiframe Remote Alarm Indication [Tx16RemAlm;CR02.5] bits will be internally generated for insertion into TS16, frame 0, as programmed in the Time Slot 16 Control Register.

Figure 10. Transmitter External Signaling Insertion



Transmit Time Slot Indication

The transmitter time slot indicator output (XINDY) is a programmable signal that is high or low for selected channels or timeslots. Programming of each time slot is determined by the Transmit Per-Channel Control Registers [TXCR;0x10–0x1F].

NOTE: For the transmitter, the bit must be set in the register two time slots ahead of the one to be actually indicated. For example, to indicate TS1 the bit for TS31 (Indicate Time Slot [IndTS31;TXCR.7 at address 0x1F]) must be set (see Figure 10). Any number of time slots up to 32 may be indicated.

Receiver Operation

The receiver features an off-line framer. Internal timing and data recovery is optionally provided. Both the recovered serial data and frame synchronization, and the slip buffer data and slip multiframe synchronization signals are provided to the user via output pins.

Timing Recovery

The receive E1 analog signal is converted by an internal adaptive-level comparator into a logic-level data stream which is fed to the timing recovery circuit. Timing recovery is accomplished through a Digital Phased Locked Loop (DPLL) using an up-down counter circuit, which operates at the 32.768 MHz (16 x 2.048 MHz) clock rate supplied at CK32I. The timing recovery circuit is designed to center the derived clock edge on each incoming E1 pulse. The phase of the recovered clock signal can be adjusted by $\pm$ 30 ns for each pulse received. The output of the timing circuit is the recovered clock signal at RCKO and the serial data output at RPCMO.

The recovered clock signal at RCKO will have jitter of $\pm$ 30 ns (.062 UI) at a frequency that corresponds to the difference between the receive E1 signal timing and CK32I. Typically, this amount of jitter is small compared to that introduced by the network E1 facility. The total of the network and Bt8510 jitter may make RCKO unsuitable for loop-timed applications without some amount of jitter attenuation via an external narrow-bandwidth Phase Lock Loop (PLL).

In the event of a loss of incoming signal, the recovered clock will continue to free-run at a rate exactly 1/16 of the clock frequency present at CK32I.

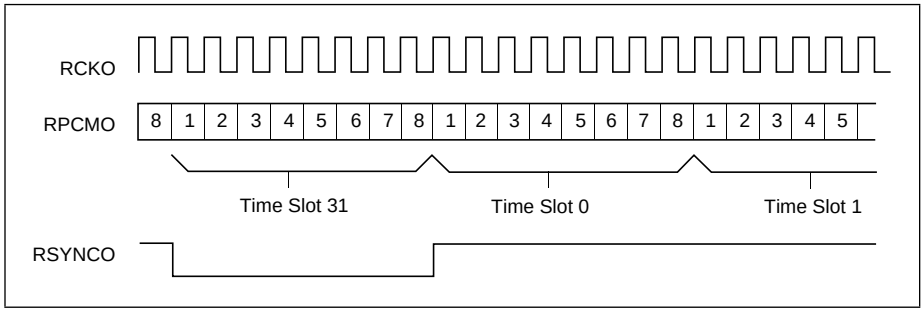
Bipolar-to-Unipolar Conversion

The bipolar-to-unipolar conversion circuit includes the High-Density Binary 3 (HDB3) decoding circuit. Optionally, Alternate Mark Inversion (AMI) coded signals without HDB3 zero suppression may be received and transmitted by setting the Enable AMI bit (EnAMI;CR00.5) to a 1 in the Configuration Register (CR00; 0x00). In AMI mode, no zero code suppression is provided.

Receiver Output Timing

The received unipolar signal is recovered and provided with clock at RPCMO and RCKO respectively. A frame synchronization signal is also provided at RSYNCO. Figure 10 illustrates a timing diagram for the receiver output signals. The RSYNCO signal is low for the 8 bits of the channel output corresponding to TS31 of each frame and then transitions high at the beginning of TS0. Both RPCMO and RSYNCO transition on rising edges of RCKO.

Figure 11. Receiver Output Timing



Framing Operation

The receiver employs an off-line framing algorithm. This means that upon detection of an Out-of-Frame (OOF) condition, the receiver will not change its timeslot, frame, or multiframe alignment until a new frame alignment is found. Data will continue to be written to the same buffer locations as before. Framing is initiated either by an OOF condition (detection of three consecutive FAS errors) or by the setting of the Force Reframing Operation control bit (FrcRefrm;CR01.2) in the Framer/Timing Control Register [CR01;0x01].

The FrcRefrm bit must be written each time a new operation is desired. It is not possible to read back this control bit, as it immediately cleared internally (the process of setting this bit to a 1 sends a momentary pulse to the receive framer which triggers the reframe sequence). The operation of this feature is timed to cause the search for the new frame position to begin immediately after the present frame alignment position. This assures an exhaustive search when CRC-4 errors are excessive, or when a false framing pattern is present.

The receiver can be set to inhibit reframing via the Abort Reframe (AbortRefrm;CR01.1) bit, which prevents an out-of-frame condition from automatically triggering reframing. Setting the AbortRefrm bit also stops a reframing operation already in progress.

Three status indicators that monitor framing functions are provided. If the reframing operation continues for more than 1 ms without identifying a unique framing pattern, the Frame Search Active Longer than 1 ms bit [FrmSch1ms;SR01.1] of the Framer/Timing Status Register [SR01;0x11] will be set. If no framing pattern is present, the FrmSch1ms indicator will be set indefinitely.

When a new frame alignment is found that is different than the old frame alignment, the Change of Frame Alignment bit [COFADet;SR01.4] will be set. This bit is latched at the end of each successful reframe operation. It can be cleared by forcing a reframe which results in no COFA. The Loss of Frame Alignment indicator [LOFAlign;SR01.3] is set and held for one transmit multiframe period if receive FAS frame alignment was lost during the previous transmit multiframe period (as measured by the XSYNCO signal).

Alarm Detection

Alarm and error indicators are provided for E1 link maintenance. These indicators are accessible in various status registers starting at address 0x10.

AIS Signal Detection

AIS Signal Detect [AISDet;SR00.2] is updated each frame interval. It is set to a 1 if all bits in three of the last four frames are a one, and there is an OOF condition present as well. This signal can be integrated by the host processor to declare a received AIS to the system, which normally requires a response on the order of three to four seconds. This bit is located in the Maintenance Status Register [SR00;0x10]

Remote Frame Alarm Detection

Remote Frame Alarm (RemFrmAlm;SR03.5) is updated every other frame interval and is set if bit 3 of the not-FAS word in TS0 is set to a 1. This bit is located in the Framing Pattern Status Register [SR03; 0x13].

Status Data

Loss-of-Signal

Loss-of-Signal Detect [LOSDet;SR00.0] is set when 32 consecutive zeros are received before HDB3 decoding. This bit is set to a 1 as soon as the condition is detected. Receiving a single 1 clears the indication. This bit is located in the Maintenance Status Register.

Out-Of-Frame Alignment

FAS framing bits are monitored to determine errors and OOF conditions. The In Frame [InFrm;SR00.4] bit in the Maintenance Status Register is cleared whenever three consecutive FAS words or three consecutive spoiler bits in not-FAS words are in error. This alarm can be integrated by the host processor to determine if a local maintenance alarm should be declared. Once a valid frame alignment has been established by the reframing process, InFrm will be set to a 1. Checking of the not-FAS spoiler bits can be disabled by setting the Ignore Not-FAS bit [IgnNotFAS;CR03.4] in the Framing Pattern Control Register.

Change of Frame Alignment

Change of Frame Alignment Detection [COFADet;SR01.4] is set whenever a reframe operation changes the state of the receiver's bit 1 (first bit) position of the frame. It is held until the next successful reframe operation. This bit is located in the Framer/Timing Status Register (SR01; 0x11).

The Change of Multiframe Alignment

Change of Multiframe Alignment Detection [COMADet;SR02.1] is set whenever a change in the frame 0 position is detected in Channel Associated Signaling (CAS) mode. It is held until the next successful reframe operation. This signal is located in the TS16 Status Register [SR02;0x12].

Signaling Freeze Set

Signaling Freeze Set [SigFrzSet;SR02.2] is the logical OR of an out-of-frame state (InFrm = 0) and an out-of-multiframe (InMFCAS = 0) state (i.e., SigFrzSet is set if either InFrm or InMFCAS is zero). This bit is located in the TS16 Status Register. The SIGFRZ output pin follows the state of the SigFrzSet bit.

CRC Failure

CRC Failure [CRCFail;SR00.1] is set if the previous 1 ms CRC-4 block had a CRC failure or if the CRC-4 frame alignment pattern is not found. The CRC Error Counter [SR11;0x1D] increments whenever the CRC-4 alignment pattern is correct (InCRCFrm = 1), but the received CRC-4 bits disagree with those calculated by the receiver. The CRCFail bit is located in the Maintenance Status Register.

PCM Controlled Frame Slip

The PCM Controlled Frame Slip [CtrlFrmSlp;SR01.5] bit indicates that a controlled frame slip event has occurred since the last reading of Framer/Timing Status Register [SR01; 0x11]. A PCM controlled slip occurs when the slip buffer repeats or deletes a frame of PCM data due to a long-term frequency difference between the receive and slip buffer clocks.

Uncontrolled Frame Slip

The Uncontrolled Frame Slip [UnctrlSlp;SR01.2] bit indicates that a slip event has occurred since the last reading of the Framer/Timing Status Register, while the slip buffer was in short-delay mode. This bit is located in the Framer/Timing Status Register.

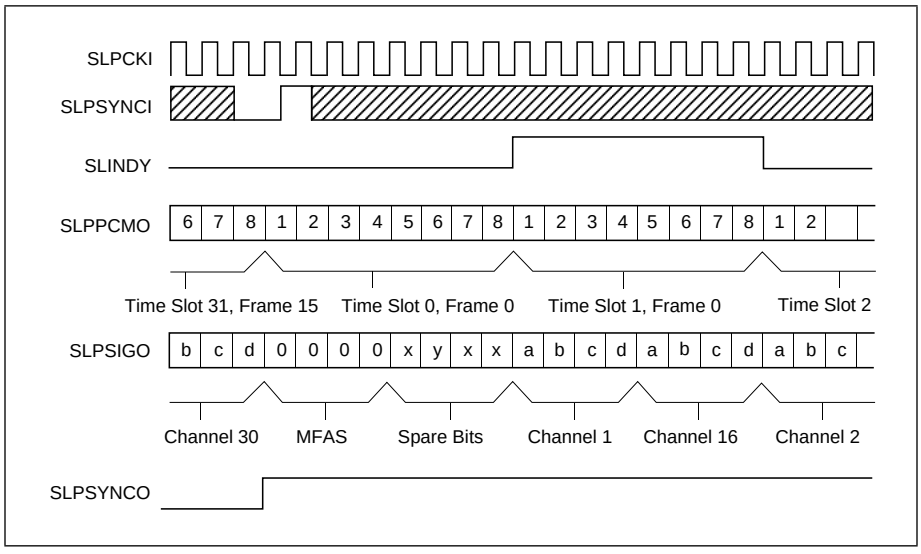
PCM Slip Buffer Operation

The receiver has a two-frame PCM slip buffer to allow synchronization of receive data to the host system timing. The buffer comprises two memory locations (one per frame of data), which are filled and emptied alternately.

Since the buffers are read according to the system timing provided at SLPCKI, all receive jitter is absorbed. The slip buffer outputs are precisely synchronized to the 2.048 MHz clock supplied at SLPCKI.

Figure 12 illustrates a timing diagram for the receive slip buffer output.

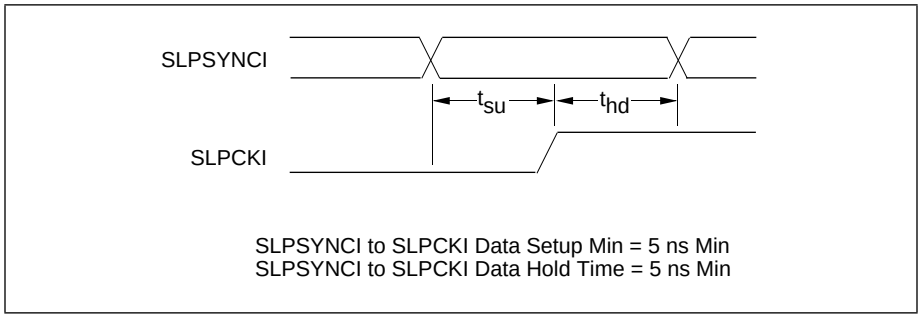
Figure 12. Receive Slip Buffer Outputs



The input to slip buffer consists of the system-provided clock and synchronization timing (SLPCKI and SLPSYNCI, respectively). A multiframe synchronization output is provided at SLPSYNCO which is low for the duration of TS31 of the multiframe's last frame. The output bits are synchronized to the SLPSYNCO signal which will align to the multiframe synchronization present at SLPSYNCI (SLPSYNCO will transition high one-half clock before the SLPSYNCI). If SLPSYNCI is not provided (when the input is grounded), SLPSYNCO will indicate an internally assumed multiframe alignment.

In any case, the embedded TS16 CAS signaling at SLPPCMO is realigned from the receive multiframe reference to the SLPSYNCO multiframe reference. Figure 13 illustrates the timing of the slip buffer signals relative to the multiframe. The SLPCKI clock frequency is 2.048 MHz with the SLPPCMO and SLPSYNCO outputs changing on the rising edge of the SLPCKI. The SLPSYNCI input is sampled on the rising edge of SLPCKI associated with the rising edge of bit 2 of the multiframe.

Figure 13. SLPSYNCI Timing Diagram



A long-term frequency offset in the received and local slip buffer clock rates can cause an entire frame of PCM data to be repeated or deleted (depending upon the direction of the slip). When this occurs, the Controlled Frame Slip (CtrlFrmSlp; SR01.5) bit will be set until it is read.

The PCM slip buffer can also be used to insert a fixed byte in the slip buffer output on a per-channel, DS0 basis. To enable this function, the appropriate Insert Idle Code [InsertIdleTSn] bit in the Receive Per-Channel Control Register [RXCR;0x00-0x0F] for a particular channel or time slot should be set to a 1. After this is done, the desired byte can be written to the corresponding Receive Idle Codes Register [RXIDLE;0x20-0x3F]. When this function is enabled, receive bytes for the given channel can also be sampled by reading from the Receive PCM Buffer [0x40–0x7F].

Slip Buffer Time Slot Indication

The Slip Buffer Time Slot Indicate [IndTSn or IndTSn+16] control bits of the Per-Channel Control Registers can be used to force the SLINDY output high for selected time slots. For the slip buffer, the IndTSn or IndTSn+16 bit must be set in the Receive Per-Channel Control Register corresponding to the time slot to be indicated. In the example in Figure 12, to indicate TS1, the bit for TS1 must be set. Any number of time slots up to 32 may be indicated.

Slip Buffer Short Delay Mode

In certain implementations, a full 256-bit frame slip function is not required, but a jitter FIFO is still required to meet the ±18 Unit Intervals (UI) short-term jitter specification. The slip buffer is provided with a short delay mode to accommodate these systems.

When the slip buffer Short Delay bit [ShrtDly;CR01.3] is enabled in the Framer/Timing Control Register, the slip buffer will initialize to a 30-bit delay position after a receive reframe with a change of frame alignment. This allows the slip buffer to accommodate ± 18 UI of jitter with a minimum of through-put delay. In this mode of operation, if the phase difference between the receive and slip buffer clocks varies by more than ± 18 UI, an uncontrolled frame slip will occur, and the short delay characteristic will be lost until the next successful receive reframe has occurred and a new frame alignment established (COFADet = 1). The slip buffer is reset to a one-frame depth during the search for a new frame alignment. An uncontrolled slip is indicated by the Uncontrolled Slip [UnctrlSlp;SR01.2] bit transitioning to a 1.

Receive Signaling Buffer

The Receive TS16 Buffer Registers [RXTS16;0x80–0x9F] contain the extracted CAS signaling information received in Time Slot 16. The registers are organized as two 16-byte signaling buffers: one located at 0x80–0x8F and the other at 0x90–0x9F. Each register in the buffer is organized into a Time Slot n and a Time Slot n+16 signaling sample (4 signaling bits or nibbles for each channel). In each CAS multiframe, when a new signaling nibble is received, it is received with another channel's nibble and both then written into one of the two signaling buffers. If signaling freeze is set (SigFrzSet =1), this writing is inhibited, and the alternate (old) signaling buffer is used for reading by the slip buffer and by the external microprocessor.

The microprocessor can read the signaling bits in the Receive TS16 Buffer Registers directly. In CCS and CAS signaling modes, the microprocessor must first read the Receive Signaling Sector [RxSigHalf;SR13.7] bit in the Interrupt Status Register [SR13;0x1F] to determine the location of the valid signaling buffer half. When RxSigHalf is cleared, it indicates that the lower half of the buffer [0x80–0x8F] is valid. When set, RxSigHalf indicates that the upper half of the signaling buffer [0x90–0x9F] is valid. If signaling freeze is active (SigFrzSet = 1) in these CCS and CAS signaling modes, the *old* buffer half will be indicated.

The signaling bits are output in TS16 of the slip buffer PCM data stream at SLPPCMO, and in the slip buffer signaling output at SLPSIGO. If signaling freeze is active, the frozen signaling bits from the old signaling buffer will be output instead of the received TS16 bits.

Receive TS16 Signaling Insertion

The Receive TS16 Signaling Insertion Buffer Registers [RXTS16SIG;0xE0–0xEF] permit the host processor to write CAS or CCS signaling data for insertion into TS16 of the SLPPCMO data stream. Each register is organized into 2 signaling nibbles; one nibble per channel. The TS16 data in each register (2 signaling nibbles at a time) can be selectively inserted in the SLPPCMO output by enabling the appropriate bit [InsertSig TSn/TSn+16;RXCR.2] in the Receive Per-Channel Control Register [RXCR;0x00-0x0F].

LAPD Operation

The Bt8510 features an internal LAPD controller for TS16 message processing. This controller manages a 16-byte message buffer for both transmit and receive directions. Idle and abort flag generation, FCS generation and checking, and zero stuffing and removal are also included. These functions are provided according to ITU-T Specification Q.921. Byte synchronization is lost due to zero stuffing, requiring the use of microprocessor interrupts to synchronize the passing of data to and from the TS16 message buffer located at 0x90–0x9F.

In LAPD mode (selected by setting the EnLAPDFmt bit in the Framer/Timing Control Register), TS16 receive data is always written to the Receive TS16 Buffer [RXTS16;0x80-0x9F]. Normal LAPD error detection and recovery procedures are used, and signaling freeze detection is ignored.

There are no restrictions on the total length of the message. Q.921 requires all messages be full 8-bit bytes. The transmitter can only transmit 8-bit bytes. If the receiver is sent a message with a non-integral number of 8-bit bytes, it will indicate an FCS error at the end.

Since the LAPD receiver removes stuffed zeros before writing received data to buffer memory, a loopback of TS16 does not work in LAPD mode. The TS16 data presented at SLPSIGO is undefined, and the TS16 data embedded in the SLPPCMO data output will also be undefined. For these reasons, it is recommended that during LAPD operation, the slip buffer be optioned to output idle code in TS16 of the SLPPCMO data stream.

A 16-byte buffer is provided for both the transmit and receive LAPD channels. Filling and emptying of these buffers is accomplished by the processor on an interrupt-driven basis. The buffer is divided into two halves to reduce the real-time requirements on the processor.

In the transmitter, half of the data buffer is filled and the control word is then set to send this half. As soon as the control word is loaded into the formatter controller, the processor is interrupted to allow loading of the other half of the buffer.

In the receiver, each time one half of the receive buffer is filled, the processor is interrupted. This allows that half to be read while the other half is filled from the TS16 data link.

Transmitter

Upon power up, the LAPD transmitter is in an indeterminate state. It should be initialized to an idle condition by setting the Transmit FCS [TxFCS;CR02.1] bit to a 1 and the Transmit Idle [TxIdle; CR02.0] bit to a 1 in the Time Slot 16 Control Register [CR02;0x02] after LAPD mode is enabled [EnLAPDFmt = 1]. Although normally setting both bits is contradictory, this operation serves to initialize the LAPD formatter properly. LAPD idle flags (01111110) will be continuously transmitted in TS16 until otherwise programmed by the processor. This operation may be used to reinitialize the formatter at any time.

Sending a Message

With the LAPD transmitter in an idle state (as described above), the processor writes the first 16 bytes of message data to the Transmit TS16 Buffer [TXTS16;0xF0–0xFF]. The first byte of data should be in location 0 (address 0xF0) of the buffer. The message is read from memory in ascending order, and the least significant bit in each byte is the first to be transmitted. This buffer may be loaded well before the message is sent, if desired. After this initial block of data is loaded in the buffer memory, the processor writes to the Time Slot 16 Control Register (0x02 with RAMEN low) a value of 0x70 to begin transmission (TxPtr[3:0] = 0111, TxAIS = 0, AbortMsg = 0, TxFCS = 0, TxIdle = 0). The 4-bit nibble TxPtr[3:0] is functionally split into two parts. The most significant bit (CR02.7) indicates to the formatter which half of the buffer to read from next. The three least significant bits indicate the stop location; i.e., where the last message byte is located.

Once new control information in the TS16 Control Register is internally uploaded to the LAPD transmitter, the processor will be interrupted (via LAPDTx [bit 4] in the Interrupt Status Register [SR13;0x1F]) by the INT* output for the next word of control information to be written to this register. The processor will then have several frame periods to write a new control word to the TS16 Control Register and to write the next block of data to the appropriate half of the Transmit TS16 Buffer.

When the end of a message is reached, or in the event of a short message, there may not be exactly 8 bytes remaining. In this case, the processor writes the remaining data to the message buffer. The processor must write the highest location occupied to the nibble TxPtr[3:0] in the upper half of the TS16 Control Register; also, TxFCS is written to a 1 in this control word, which sends the 2-byte FCS after the last block of data.

When this last set of control information is uploaded to the LAPD transmitter circuit, the processor will be interrupted. At this time, a new message may be sent, or idle mode may be selected (TxIdle = 1). If a new message is to be sent immediately, the unused half of the Transmit TS16 Buffer may be loaded, and the TS16 Control Register written accordingly. This will result in only one idle flag being transmitted between messages. If there is no new message ready, the processor must write TxIdle = 1 to the control register. If this is not done, undefined data will be transmitted over the TS16 data link.

Aborting a Message

To abort a message in progress, the controller writes AbortMsg = 1 to the TS16 Control Register. The LAPD transmitter will finish sending the message byte in progress, then transmit an abort flag (11111110). After writing the AbortMsg bit, a second write operation to the Time Slot 16 Control Register may follow after the next interrupt to force the formatter into the idle condition or to transmit another message, In the latter case, the abort flag will be followed by one idle flag, and then the new message will begin. If the TS16 Control Register is not written with a new control word, the formatter will continue to transmit abort flags.

Transmitter Interrupts

The LAPD transmitter generates an interrupt when it has uploaded the present control word from TS16 Control Register and is ready for a new control word to be written by the processor. The Interrupt Status Register [SR13;0x1F] indicates the source of the interrupt, but not the cause. The software must know from the context what response is required. The interrupt condition is cleared by writing to the TS16 Control Register.

If the interrupt is a mid-message interrupt, a new TS16 control word must be written, with TxPtr[3:0] equal to the location of the next message byte. Which half of the Transmit TS16 Buffer should be written to next is indicated by the state of the LAPD Half [LAPDHalf;SR13.6] bit in the Interrupt Status Register. In contrast, the most significant bit of TxPtr[3:0] specifies which half will be transmitted next by the LAPD formatter.

Receiver

The receiver powers up in an indeterminate state. It is initialized by the receipt of an idle flag, which sets RxIdle = 1 in the TS16 Status Register [SR02;0x12]. When a message is received, the receiver removes stuffed zeros and writes the resulting data to the 16-byte upper half of the Receive TS16 Buffer [RXTS16; 0x90–0x9F]. This upper half itself is split into halves, forming two alternate 8-byte buffers which begin at memory locations 0x90 and 0x98. Deformatted data is written to one of the 8-byte buffer halves in ascending order (i.e., 0x90, 0x91, etc.) until all eight memory locations are full. The receiver always begins writing in the 8-byte buffer opposite from where the last message was written.

When the first eight buffer locations are full, the processor is interrupted (via LAPDRx [bit 5] in the Interrupt Status Register) by the INT* output to read the data out of that 8-byte buffer half. The processor normally has eight frame periods to read the data, before it is overwritten with new data. The interrupt is cleared when the processor reads the TS16 Status Register [SR02;0x12]. The TS16 Status Register will indicate a message in progress at this time (RxIdle = 0, RxPtr[3:0] = 0111). If the upper 8-byte half of the buffer had just been filled, then RxPtr[3:0] = 1111 and locations 0x98 through 0x9F must be read during the next eight frames to retrieve the message.

When the last block of data has been received, the processor will again be interrupted. This time, the TS16 Status Register will indicate the end of message (RxIdle = 1, RxPtr[3:0] = n, BadFCS = 0 or 1). The pointer nibble, RxPtr = n, indicates the highest numbered location that was written. Locations 0x90 to 0x90+n or 0x98 to 0x98+n must be read to retrieve the data. The two highest numbered locations contain the FCS that was received at the end of the message.

If the received message is a multiple of 8 bytes, then the processor will be interrupted to read the last block of data before the FCS has yet to be received. In this event, the processor will again be interrupted when the FCS has finally been received and checked, and an idle flag received. The TS16 Status Register will indicate RxPtr[3:0] = 0001, BadFCS = 1 or 0, and RxIdle =1. The FCS that was received will be in locations 0 and 1 of in one of the 8-byte buffers. Again, the data must be read out during the next eight frames, or it may be overwritten by a new message. Alternatively, the FCS data may be ignored, and the state of BadFCS used directly by itself.

If all ones are received in TS16 for 16 consecutive frames, AIS Detect [TS16 AISDet;SR02.3] will be set until a zero is received.

It is important that software strategies allow for the fact that the LAPD receiver cannot recognize the FCS as such until the closing flag is recognized. It can happen that the processor is interrupted to read 8 message bytes, and the next byte received is the closing flag. In this event, the last two bytes read from memory were not message bytes after all, but were actually the FCS.

Interrupts

The LAPD receiver generates an interrupt via the INT* output in response to three events; the current half of the LAPD message buffer is full (indicated by the LAPDRx bit), the end-of-message flag was detected, or an abort flag was detected. After initialization, interrupts should be ignored until an idle flag (end of message) is received.

The TS16 Status Register indicates the cause of each receive LAPD interrupt. The interrupt will be cleared upon the reading of this register. The interrupt status is updated upon a new interrupt even if the previous interrupt has not been cleared.

If an interrupt is due to the current half of the receive message buffer being full, the RxIdle bit will be cleared, and the RxPtr[3:0] nibble will indicate which half of the buffer must be read.

If an interrupt is due to the end-of-message flag being detected, RxIdle = 1, BadFCS will indicate the result of the FCS error check, and RxPtr[3:0] will indicate the last location written. The processor will not be interrupted again until 8 bytes of a new LAPD message have been received.

If an interrupt is due to an abort flag being received, the RxAbort bit will be set. The message buffer does not have to be read in this case. The processor will not be interrupted again until 8 bytes of a new message (or a message shorter than 8 bytes) have been received.

The LAPD interrupts are maskable in the Interrupt Control Register [CR09;0x0F] via the LAPD Interrupt Enable bit (LAPDIE;CR09.4). The receiver LAPD interrupt should be masked if the E1 receiver is out-of-frame (InFrm = 0), because the LAPD receiver considers any byte that is not the idle flag or abort flag to be a message byte. This results in numerous interrupts during out-of-frame events if the interrupt is not masked.

When the message received is 1 byte more than a multiple of 8 bytes and a new message starts immediately after a single flag character, the processor will have only two frame periods to read the previous message buffer. Therefore, receive LAPD processing should have a high priority in interrupt processing.

Registers

NOTE: For a summary of all registers refer to the Register Summary section at the end of this chapter.

Control Registers

There are 10 read/write control registers in the Bt8510 (not counting the per-channel control registers which are included as part of the buffer memory). These control registers are located at addresses 0x00–0x08 and 0x0F. Register contents are listed in the Register Summary section at the end of this chapter.

Control registers are latches set by a write operation by the external processor. Each control register may also be read to confirm its contents. The RAMEN pin must be low during read/write operations to these control registers.

0x00—Configuration Control Register (CR00)

The Configuration Register is located at address 0x00. Table 3 details the operation of the InsertCRC, InsertFrm, and EnFEBE bits of the Configuration Control Register and the InsertIdleTSn [TXCR.1] bit of the Transmit Per-Control Register for TS0 [0x10].

7	6	5	4	3	2	1	0
PayLp	TxRxClk	EnAMI	TxAIS	EnFEBE	InsertFrm	InsertCRC	EnClkRcv

PayLp Payload Loopback—A loopback of the full bit stream to the facility or network side. Setting this bit causes the transmitter to perform a DS0 loopback in every time slot. If InsertFrm is also turned off, the FAS framing bits will also be looped. In LAPD mode, the LAPD transmitter works as usual. If LAPD mode is not enabled, TS16 is looped back transparently. (In CAS mode, multiframe bit insertion may also be turned on or off.)

TxRxClk Transmit/Receive Clock—Enables the loop timing mode when set to a 1. In this mode the receive clock is used for the transmit clock reference instead of the Transmit Clock In (XCKI) signal. If the Enable Clock Recovery (EnClkRcv) bit is set, then the recovered clock is used. This option should be selected simultaneously with the Payload Loopback (PayLp) bit.

If the TxRxClk = 0, the transmitter will default to the XCKI input clock. The transmit clock in use is repeated on Transmit Clock Out (XCKO).

EnAMI Enable Alternate Mark Inversion Line Code—Changes the HDB3 line code to AMI on both receive and transmit. This option disables the Loss of Signal Indicator [LOSDet;SR00.0], and changes the function of the line code violation status and the LCV Counter [SR10;0x1C]

TxAIS Transmit AIS —Causes the unframed all-ones AIS signal to be transmitted. This option dominates over all other transmitter options.

EnFEBE Enable Far-End Block Error (FEBE)—Enables the use of the E-bits in the CRC-4 multiframe alignment signal for the automatic reporting of a CRC error received during the previous multiframe (FEBE function). Both InsertFrm and InsertCRC bits must be enabled. See Table 3.

InsertFrm Insert Framing—Enables the internal insertion of the FAS framing bits in TS0. See Table 3.

InsertCRC Insert CRC—Enables the internal CRC-4 generation circuit of the framer. The CRC-4 bits are inserted by the framer into TS0 as per ITU-T G.704 and G.706. See Table 3.

EnClkRcv Enable Clock Recovery—Enables the timing recovery circuit in the receiver. If EnClkRcv =1, a 32.768 MHz clock must be provided at 32CKI. If EnClkRcv =0, the inputs to the receiver must be clocked via a 2.048 Mhz clock at RCKI, and the 32CKI must be connected to ground or V_{DD}. Refer to the Line Interface section in the Functional Description chapter for timing details.

Table 3. Time Slot 0 Control

Control Register Bits				Source of Transmitted Information Bits					Description
InsertIdleTS0 (TXCR.2; Addr 0x10)	InsertFrm CR00.2	InsertCRC CR00.1	EnFEBE CR00.3	FAS Word	Si	A	E	Sa4–Sa8	
0	0	x	x	XPCMI	XPCMI	XPCMI	XPCMI	XPCMI	All TS0 information can be inserted through XPCMI input.
1	0	x	x	TXIDLE Register	TXIDLE Register	TXIDLE Register	TXIDLE Register	TXIDLE Register	All TS0 information can be inserted from the Transmit Idle Code Register (TXIDLE) for TS0.
0	1	0	x	x0011011	1	CR03.5	1	CR04–CR08	Automatic insertion of the FAS pattern with all CRC-4 bits set to 1.
0	1	1	0	x0011011	CRC-4	CR03.5	CR03.6,7	CR04–CR08	Automatic insertion of the FAS pattern and the CRC-4 pattern.
0	1	1	1	x0011011	CRC-4	CR03.5	E-bits	CR04–CR08	Automatic remote CRC-4 error reporting capability via the E-bits (FEBE).

0x01—Framer/Timing Control Register (CR01)

The Framer/Timing Control Register is located at address 0x01. If none of the EnCAS, EnCCS, or EnLAPDFmt bits are enabled to a 1, the Time Slot 16 (TS16) data is treated as any other data channel (sometimes referred to as channel 31 operation). This mode can also be used to pass through CCS signaling.

7	6	5	4	3	2	1	0
EnLAPDFmt	EnCAS	EnCCS	EnBitSlip	ShrtDly	FrcRefrm	AbortRefrm	AltCAS

EnLAPDFmt Enable LAPD Formatting—Enables LAPD message processing over TS16 in both transmit and receive directions. LAPD operation requires the use of the LAPD microprocessor interrupt, and the use of the Transmit and Receive TS16 Buffers. This is because multiframe synchronization is lost due to zero stuffing and FCS transmission. Note that selection of this option changes the meaning of the TS16 Control Register [CR02;0x02] and TS16 Status Register [SR02;0x12]. This signal controls both the transmitter and receiver.

EnCAS Enable CAS—Enables the Channel Associated Signaling (CAS) mode. The receiver will look for a multiframe signal (four zeros in the upper nibble of TS16, frame 0). If signaling freeze is enabled, a valid multiframe pattern must be found before any information will be written to the Receive TS16 Buffer. This signal controls both transmitter and receiver.

EnCCS Enable CCS—Enables the Common Channel Signaling (CCS) mode. The signaling is transmitted from the Transmit TS16 Buffer, and received signaling is written to the Receive TS16 Buffer. The InsertIdleTsn bit in the Per-Channel Control Registers must also be set for TS16 to enable this mode (Note that in CCS mode, the Transmit Idle Code Register for TS16 [0xB0] is ignored). Signaling freeze may be asserted by the host processor, but since multiframe information is assumed to be nonexistent, the Enable Signaling Freeze [EnSigFrz;CR02.1] must be cleared. The half of the Receive TS16 Buffer that is being used is indicated by the RxPtr[3] bit in TS16 Status Register [SR02;0x12], and in conjunction with the Receive CAS MF Interrupt [RxCASMFItr;SR13.0] bit or the 2 ms Receive Clock [2msRxClk;SR01.7] bit, can be used to synchronize data transfers to and from the host processor. EnCCS controls both transmitter and receiver.

EnBitSlip Enable Bit Slip—Modifies the framer algorithm to allow a single bit slip upstream. If the framing pattern in TS0 is detected to have moved plus or minus a single bit position, the receiver is immediately realigned and the occurrence of the bit slip is indicated by the Bit Slip bit (BitSlip;SR01.0] in the Framer/Timing Status Register [SR01;0x11]. This occurrence will not be counted as an FAS error.

ShrtDly Slip Buffer Short Delay Mode—When ShrtDly = 1, the receive-in-to-slip-buffer-out delay is set to be 30 bits or 14.64 µsec. This option allows the use of the slip buffer for short-term jitter absorption (±18 unit intervals) without incurring unnecessary delay. Each time the receiver reframes and there is a Change of Frame Alignment (COFA), the slip buffer is reset to this position. In CAS signaling mode, if the EnSigFrz bit is set, there will still be a one multiframe delay for signaling to allow the freeze function to operate. If the EnSigFrz bit is cleared, the signaling will have the same delay as the data. If the slip buffer clock (SLPCKI) is allowed to vary by more than ±18 clock cycles, the buffer will perform a controlled frame slip, and the short delay characteristic will be lost until the next receive COFA.

FrcRefrm Force Reframing Operation—Forces a reframe operation on the E1 signal. This control can be used to force reframing on an E1 signal, which has a very high CRC or FAS error count but is not generating an out-of-frame condition. This signal is timed so the new frame search will begin immediately after the present frame bit 1 position.

AbortRefrm Inhibit/Abort Reframing—Stops a framing operation on the receive E1 signal if in progress and prevents the framer from trying to reframe. This input can be used to discontinue a framing operation and to force the framer to ignore an unassigned or idle E1 line.

AltCAS Alternate CAS Multiframe Alignment—If AltCAS = 1, the transmitter will align the CAS multiframe pattern with the not-FAS word in TS0. If AltCAS = 0, the CAS multiframe will be aligned with the FAS word in TS0.

0x02—TS16 Control Register (CR02)

The TS16 Control Register is located at address 0x02. Time Slot 16 may be used for either CAS, CCS, or D-channel signaling using the LAPD format. CAS is formatted according to ITU-T G.732. In CCS mode, the data from the XPCMI, XSIGI, or the TS16 buffer space is simply transmitted to the other end of the E1 link. LAPD formatting includes FCS generation and checking, zero stuffing and removal, and flag generation and detection. LAPD formatting may only be used with data written to and read from the TS16 Buffers, and requires the use of the microprocessor interrupt for synchronization. Controls labeled as only working in CAS mode are ignored in other modes.

CAS/CCS Mode Operation

7	6	5	4	3	2	1	0
TxX4	TxX3	Tx16RemAlm	TxX1	TxTS16AIS	FrzSig	EnSigFrz	InsertCASFrm

TxX4 Transmit X4—Sets the current state of the x4 bit (bit 8) in frame 0 of TS16. This is a CAS mode function only.

TxX3 Transmit X3—Sets the current state of the x3 bit (bit 7) in frame 0 of TS16. This is a CAS mode function only.

Tx16RemAlm Send Multiframe Remote Alarm Indication—Forces the Y bit (bit 6) of TS16 to 1, indicating a remote multiframe alarm. This is a CAS mode function only.

TxX1 Transmit X1—Sets the current state of the x1 bit (bit 5) in frame 0 of TS16. This is a CAS mode function only.

TxTS16AIS Transmit TS16 AIS—Causes the AIS all-ones signal to be transmitted in TS16 only. This signal is dominant over the Per-Channel Control Register bits. This function works in any signaling mode.

FrzSig Freeze Signaling—Freezes the current state of the Receive TS16 Buffer and redirects the reading of TS16 data by the slip buffer. This function works in both CCS and CAS modes. When the processor reads this data, it should read from the TS16 buffer half indicated by the Receive Signaling Sector [RxSigHalf;Sr13.7] bit of the Interrupt Status Register [SR13;0x1F]. Refer to Receive Signaling Buffer description the Receiver Operation section of the Functional Description chapter.

EnSigFrz Enable Signaling Freeze—Enables the signaling freeze function. Update of the signaling bits in the Receive TS16 Buffer will be inhibited if the receiver either frame (FAS) or multiframe (CAS) synchronization. In this case, the old signaling bits from the previous multiframe will be output in TS16 in the slip buffer PCM output (SLPPCMO) and the slip buffer signaling output (SLPSIGO). This function only works in CAS mode. If this function is enabled in other signaling modes, writes to the Receive TS16 Buffer will be inhibited unless a valid CAS multiframe pattern is found.

InsCASFrm Insert CAS Framing—When InsCASFrm = 1, the Bt8510 will automatically generate the CAS multiframe pattern and optional bits in TS16, frame 0. This bit must be low for TS16 clear channel mode.

LAPD Mode Operation

LAPD operations are detailed in the LAPD Operation section in the Functional Description chapter.

7	6	5	4	3	2	1	0
TxPtr[3]	TxPtr[2]	TxPtr[1]	TxPtr[0]	TxTS16AIS	AbortMsg	TxFCS	TxIdle

TxPtr[3] Transmit Pointer[3]—Informs the LAPD formatter of the Transmit TS16 Buffer 8-byte half-buffer from which to start reading the data. TxPtr[3] = 0 selects the lower half (starting at address 0xF0) while TxPrt[3] = 1 selects the upper half (starting at address 0xF8). TxPtr[3] must be updated each time the TS16 Control Register is written.

TxPtr[2:0] Transmit Pointer[2:0]—Informs the LAPD formatter of where to stop reading message bytes from the Transmit TS16 Buffer. All messages must be an integral number of bytes in length. The first byte to be sent is in address 0xF0 or 0xF8, and the formatter counts up to the value in bytes. When the last byte is read, the processor will be interrupted for more data unless TxFCS is set (indicating the end of this message), in which case the processor will be interrupted after the sending of the last byte of the FCS.

TxTS16AIS Transmit AIS—Causes the AIS all-ones signal to be transmitted in TS16 only. This signal is dominant over the Per-Channel Control Register bits.

AbortMsg Abort Message—Causes the abort flag (11111110) to be transmitted and the current message is abandoned. The transmitter will then go to idle mode, transmitting idle flags until new instructions are received.

TxFCS Transmit FCS—Causes the 16-bit ITU-T Q.921 FCS to be calculated and inserted in the last 2 bytes of a message. The setting of this bit also signals the last block of data in a message.

TxIdle Transmit Idle Code—Causes the LAPD idle flag sequence (01111110) to be continuously transmitted on TS16 until new instructions are received from the microprocessor.

0x03—Framing Pattern Control Register (CR03)

The Framing Pattern Control Register is located at address 0x03.

7	6	5	4	3	2	1	0
Si1	Si0	TxRemAlm	IgnNotFAS	EnLocLp	EnLineLp	EnExtSig	EnAnalog

Si1, **Si0** Si or E bits—Part of the CRC alignment pattern described in G.704 §2.3.3.4. Si1 (E1) is the E-bit transmitted during the not-FAS word in CRC MF frame 15. Si0 (E0) is the E-bit transmitted during the not-FAS word in CRC-4 MF frame 13. Both bits are normally set to one, or may be used for automatic remote CRC error reporting (FEBE) by setting the Enable FEBE bit [EnFEBE;CR00.3] of the Configuration Control Register [CR00;0x00]. In that case, the bit setting in this register is ignored.

TxRemAlm Transmit Remote Alarm Indication—Forces the A-bit of the not-FAS word in TS0 to a one. The Insert Framing bit [InsFrm;CR00.2] of the Configuration Control Register must be enabled.

IgnNotFAS Ignore Not-FAS—Setting IgnNotFAS = 1, forces the receive framer to ignore the checking of the spoiler bit of the not-FAS word (bit 2 in the frame not containing the FAS) in the out-of-frame (OOF) detection circuit once the framer has acquired frame alignment.

EnLocLp Enable Local Loopback —Causes the full-rate E1 signal to be looped from transmit to receive, including the framer circuit. The slip buffer outputs will also return the transmit data. For proper data clocking either the internal clock recovery must be enabled or the XCKO pin must be externally looped to the RCKI pin. Idle code insertion still works in both transmit and receive directions. This control will only work with line loopback disabled (EnLineLp = 0). Figure 13 illustrates the local loopback operation.

EnLineLp Enable Line Loopback—Causes the full-rate E1 signal to be looped from the receive analog or digital input to the analog transmitter output prior to any processing. The received signal is recovered and transmitted unchanged. The receive analog interface must be enabled. The digital transmitter outputs are unaffected by this control. Figure 14 illustrates the line loopback operation.

EnExtSig Enable External Signaling Insertion—Enables the XSIGI input for transmit signaling insertion. When this option is used, signaling idle code insertion and DS0 loopback can no longer be performed with the Per-Channel Control Registers.

EnAnalog Enable Analog—Applies power to the analog interface circuits. The digital input pins RPOSI and RNEGI become outputs, and repeat the recovered data. The analog receiver outputs are connected to the framer inputs internally. With analog enabled, the receiver will only work with internal clock recovery enabled.

Figure 14. Local Loopback

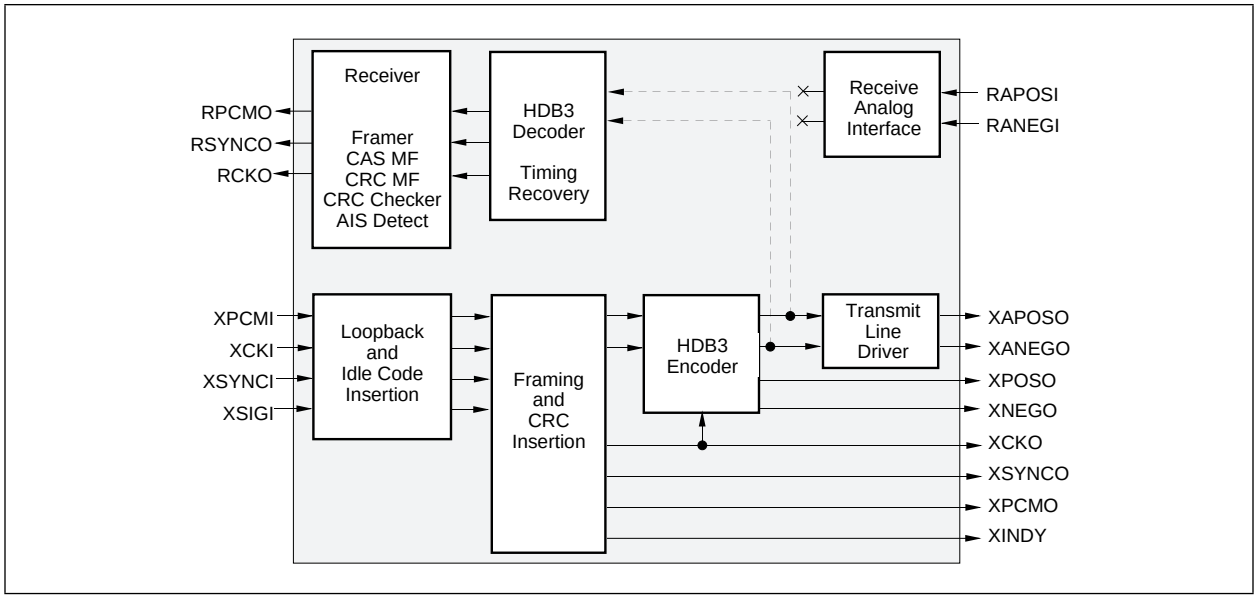
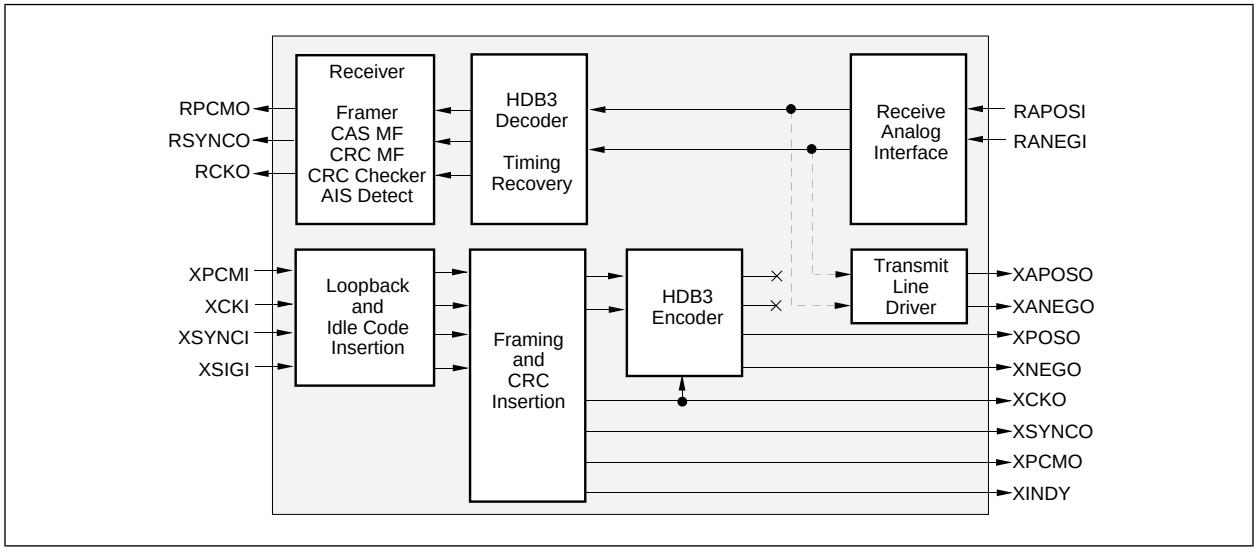


Figure 15. Line Loopback



Sa-Bit Registers

To aid ISDN and facility data link implementations, five registers are provided to minimize processor overhead for processing the Sa4-Sa8 bits. Each register controls the transmission of a particular Sa bit for an entire CRC-4 multiframe (there are 8 Sa4 bits, 8 Sa5 bits, etc., per CRC-4 multiframe). The Sa-bits are defined in ITU-T G.704 as additional spare bits reserved for international use. A simple discussion of the protocol is given in Appendix B.

0x04—Sa4 Bits (CR04)

Control Register 04 controls the Sa4 bits and is located at address 0x04. Each bit is transmitted in the not-FAS word in the assigned frame of the CRC-4 multiframe. The 8 bits retain a fixed relationship to the CRC-4 multiframe.

7	6	5	4	3	2	1	0
TxSa4Frm15	TxSa4Frm13	TxSa4Frm11	TxSa4Frm9	TxSa4Frm7	TxSa4Frm5	TxSa4Frm3	TxSa4Frm1

0x05—Sa5 Bits (CR05)

Control Register 05 controls the Sa5 bits and is located at address 0x05. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is transmitted in the assigned frame.

7	6	5	4	3	2	1	0
TxSa5Frm15	TxSa5Frm13	TxSa5Frm11	TxSa5Frm9	TxSa5Frm7	TxSa5Frm5	TxSa5Frm3	TxSa5Frm1

0x06—Sa6 Bits (CR06)

Control Register 06 controls the Sa6 bits and is located at address 0x06. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is transmitted in the assigned frame.

7	6	5	4	3	2	1	0
TxSa6Frm15	TxSa6Frm13	TxSa6Frm11	TxSa6Frm9	TxSa6Frm7	TxSa6Frm5	TxSa6Frm3	TxSa6Frm1

0x07—Sa7 Bits (CR07)

Control Register 07 controls the Sa7 bits and is located at address 0x07. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is transmitted in the assigned frame.

7	6	5	4	3	2	1	0
TxSa7Frm15	TxSa7Frm13	TxSa7Frm11	TxSa7Frm9	TxSa7Frm7	TxSa7Frm5	TxSa7Frm3	TxSa7Frm1

0x08—Sa8 Bits (CR08)

Control Register 08 controls the Sa8 bits and is located at address 0x08. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is transmitted in the assigned frame.

7	6	5	4	3	2	1	0
TxSa8Frm15	TxSa8Frm13	TxSa8Frm11	TxSa8Frm9	TxSa8Frm7	TxSa8Frm5	TxSa8Frm3	TxSa8Frm1

0x0F—Interrupt Control Register (CR09)

The Interrupt Control Register is located at address 0x0F and serves as a mask for enabling/disabling interrupt sources to trigger the INT* output to transition low. Interrupt sources defined by the bits in this register are logically ORed in triggering the INT* output.

7	6	5	4	3	2	1	0
LCVIE	CRCIE	FASIE	LAPDIE	RxOOFIE	TxCRCMFIE	RxCRCMFIE	RxCASMFIE

LCVIE LCV Interrupt Enable—Enables an interrupt upon overflow of the Line Code Violation Counter [SR10;0x1C]. Reading the Framing Pattern Status Register [SR03;0x13] clears the interrupt without affecting the counter. Reading the counter clears the counter.

CRCIE CRC Interrupt Enable—Enables an interrupt upon overflow of the CRC4 Error Counter [SR11;0x1D]. Reading the framing pattern Status Register clears the interrupt without affecting the counter. Reading the counter clears the counter.

FASIE FAS Interrupt Enable—Enables an interrupt upon overflow of the FAS error counter. Reading the Framing Pattern Status Register clears the interrupt without affecting the counter. Reading the counter clears the counter.

LAPDIE LAPD Interrupt Enable—Enables the LAPD interrupts. Clearing this bit in LAPD mode will prevent spurious interrupts from the LAPD receiver during out-of-frame conditions.

RxOOFIE Receive OOF Interrupt Enable—Enables an interrupt signaling the loss-of-frame alignment in the receiver.

TxCRCMFIE Transmit CRC MF Interrupt Enable—Enables an interrupt at the beginning of each transmit CRC-4 multiframe. The interrupt is cleared when the Interrupt Status Register [SR13;0x1F] is read. This signal will reflect both CAS and CRC-4 multiframe alignment, unless Alternate CAS Multiframe Alignment [AltCAS;CR01.0] in the Framer/Timing Control Register [CR01;0x01] has been selected. This signal is used to time the writing of the Sa-bit registers, and signaling insertion registers. These interrupts will occur (if enabled) on a 16-frame boundary regardless of the status of the Insert CRC bit [InsCRC;CR00.1] in the Configuration Control Register [CR00;0x00].

RxCRCMFIE Receive CRC MF Interrupt Enable—Enables an interrupt at the beginning of each receive CRC-4 multiframe. The interrupt is cleared when the Interrupt Status Register is read. This signal will change its timing with a change in frame alignment. This interrupt is used to time the reading of the Sa-bit registers. These interrupts will occur (if enabled) on a 16-frame boundary regardless of the status of the In CRC Frame [InCRCFrm;SR00.7] bit in the Maintenance Status Register [SR00;0x10].

RxCASMFIE Receive CAS MF Interrupt Enable—Enables an interrupt at the beginning of each receive CAS multiframe. The interrupt is cleared when the Interrupt Status Register is read. This signal will change its timing with a change in frame or CAS multiframe alignment. These interrupts will occur (if enabled) on a 16-frame boundary regardless of the status of the In Multiframe CAS bit [InMFCAS;SR02] in the TS16 Status Register [SR02;0x12]

Status Registers

The Bt8510 has 10 status registers located in addresses 0x10–0x19. The contents of these registers are listed in the Register Overview Summary section at the end of this chapter. The status signals are contained in latches and are applied to the microprocessor data bus on the appropriate read command.

Many of the status bits are updated at 2 ms intervals. This interval is timed by the transmit clock circuitry so that it is not affected by reframes. This also synchronizes the status indications when E1s from multiple integrated circuits are being monitored. Some status bits are updated as they happen. The indication period for each bit is given with each description.

Driving an interrupt to the microprocessor with the XSYNCO output provides a convenient way to time the sampling of the status registers every 2 ms.

0x10—Maintenance Status Register (SR00)

The Maintenance Status Register is located at address 0x10 and contains the major E1 maintenance indicators.

7	6	5	4	3	2	1	0
InCRCFrm	LCVDet	FASErr	InFrm	HDB3Det	AISDet	CRCFail	LOSDet

InCRCFrm In CRC Frame—Set high when a correct CRC-4 multiframe alignment signal (001011) has been detected during the previous multiframe. This indication is updated every 16 frames according to the receive CRC-4 multiframe alignment signal. A loss of basic frame alignment (FAS) causes an immediate loss of CRC-4 multiframe alignment.

If there has been a change in the CRC-4 alignment (not merely an error), InCRCFrm will go high on the second correct alignment signal.

LCVDet Line Code Violation Detection—Set high if there was a Line Code Violation (LCV) during the previous multiframe. In HDB3 mode, this is a bipolar violation that is the same polarity as the previous bipolar violation per ITU-T Recommendation O.161 §2.2. In AMI mode, any bipolar violation will be counted as an LCV per O.161 §2.1. This indication is latched every 2 ms by the falling edge of XSYNCO.

FASErr FAS Error—Set high if there was a Frame Alignment Signal (FAS) error during the previous multiframe. This indicator is enabled only when in frame alignment (InFrm = 1). It is latched every other frame and held for two frames following the error.

InFrm In Frame—Set high if the receive framer is locked onto a valid FAS framing pattern. A minimum of three frames is required to validate a new framing pattern (2 FAS words and 1 not-FAS word). Once in frame, a minimum of six frame intervals is required to lose frame (3 consecutive FAS words in error). This indicator is not latched, but always indicates the current FAS frame alignment status of the receiver.

HDB3Det HDB3 Signature Detect—Set high if a legal HDB3 signature per ITU-T Recommendation O.162 was present during the previous transmit multiframe. The indicator is active regardless of the setting the Enable AMI Line Code bit [EnAMI;CR00.5] in the Configuration Control Register. This indication is latched every 2 ms by the falling edge of XSYNCO.

AISDet AIS Detect—Set high if the receiver is out-of-frame (InFrm =0) and three of the last four frames were all-ones. It is latched each frame. This signal may need to be further integrated by the microprocessor to decide if an AIS signal is actually present.

CRCFail CRC Failure—Set high for 1 ms (one CRC-4 block) if the CRC check for the CRC block fails. The CRC Error Counter (SR11; 0x1D) will increment each time a block is in error. If the receiver has not found a valid CRC-4 multiframe pattern, this bit will be set and CRC errors will be reported to the far-end if FEBE is enabled (EnFEBE; CR00.3). However, the CRC-4 Error Counter will not count errors unless the receiver is in CRC-4 multiframe alignment (InCRCFrm =1). The CRC Error Counter will usually (15 of 16 times) count one error as the CRC-4 multiframe alignment is lost.

LOSDet Loss-of-Signal Detect —Indicates that the received signal has been absent for at least 32 clock cycles (prior to HDB3 decoding), meaning that the E1 line signal has been lost. This alarm indicator is valid only when HDB3 line code is selected (EnAMI = 0). This signal is set when 32 consecutive zeros have been detected. It is cleared by the receipt of a 1 of either polarity.

0x11—Framer/Timing Status Register (SR01)

The Framer/Timing Status Register is located at address 0x11 and contains status information about the receive framer.

7	6	5	4	3	2	1	0
2msRxClk	2msTxClk	CtrlFrmSlp	COFADet	LOFAlign	UnctrlSlp	FrmSch1ms	BitSlip

2msRxClk 2 ms Receive Clock—Shows the timing derived by the framer from the receive signal. This signal may change its timing due to reframes on the receive signal. It is high for eight frames, then low for eight frames. In CAS signaling mode, it follows the CAS multiframe alignment. In other signaling modes, it counts modulo-16 frames from the latest new frame event.

2msTxClk 2 ms Transmit Clock—Used to synchronize the scanning of the status indications. This synchronization signal can be used as a 2 ms (one multiframe) indicator. It is high for eight frames, then low for eight frames. This signal is independent of the type of signaling present.

CtrlFrmSlp Controlled Frame Slip—Set when the slip buffer performs a PCM controlled frame slip due to a long-term variation in the phase relationship of the receive and the slip buffer clocks. This indication will be issued once for every 256 bits or 125 µs of phase slip between the received clock (recovered or RCKI) and the slip buffer clock (SLPCKI), and is held until this register is read.

COFADet Change of Frame Alignment Detection—Set when a reframe changes the receiver bit 1 position in the frame counter. This indicator changes only upon reframe and thus indicates the result of the last reframe operation. It is cleared by a reframe which results in no COFA.

LOFAlign Loss of Frame Alignment—Set if basic frame alignment (FAS) was lost at any time during the previous transmit multiframe period. This indication is latched every 2 ms by the falling edge of XSYNCO.

UnctrlSlp Uncontrolled Slip—Indicates that a slip event occurred since the last reading of this register, while the slip buffer was in short delay mode (ShrtDly = 1).

FrmSch1ms Frame Search Active Longer than 1 ms—Indicates a frame search operation has taken longer than the indicated interval. It is set during a frame operation at the occurrence of the interval and cleared when the framing operation is finished or aborted. If this appears on several consecutive 1 ms samples, it is possible that a PCM or data channel is emulating the FAS, or that no valid FAS framing pattern exists.

BitSlip Bit Slip—Indicates the framing pattern moved plus or minus one bit position on the receive E1 signal, during the previous transmit multiframe period. This indication is held for one transmit multiframe. This indication is latched every 2 ms by the falling edge of XSYNCO.

0x12—TS16 Status Register (SR02)

The TS16 Status Register is located at address 0x12. Time Slot 16 can be used for CAS, CCS, or D-Channel Signaling using the Q.921 LAPD format. CAS is formatted according to G.732. In CCS mode, the only valid status indications are TS16AISDet and SigFrzSet. LAPD formatting includes FCS generation and checking, zero-bit insertion and deletion, and flag generation and detection. LAPD messages can only be read or written from the Receive and Transmit TS16 Buffers, and require the use of the microprocessor interrupt (INT*) to synchronize the transfer of message data between the framer and the host microprocessor.

CAS/CCS Mode

7	6	5	4	3	2	1	0
RxX4	RxX3	MFRemAlm	RxX1	TS16AISDet	SigFrzSet	COMADet	InMFCAS

RxX4 Receive X4—The received x4 bit (bit 8 of TS16 in frame 0). In CCS mode, this bit is meaningless and should be ignored.

RxX3 Receive X3—The received x3 bit (bit 7 of TS16 in frame 0). In CCS mode, this bit is meaningless and should be ignored.

MFRemAlm Multiframe Remote Alarm Indication—Indicates the state of the Multiframe Remote Alarm Indication bit (the Y bit or bit 6 of TS16 in frame 0). In CCS mode, this bit is meaningless and should be ignored.

RxX1 Receive X1—Is the received x1 bit (bit 5 of TS16 in frame 0). In CCS mode, this bit is meaningless and should be ignored.

TS16AISDet TS16 AIS Detect—Set when the all-ones signal is detected in TS16 for a full multiframe after multiframe alignment has been lost.

SigFrzSet Signaling Freeze Set—When enabled, this bit is the logical OR of the out-of-frame (InFrm = 0) and out-of-multiframe (InMFCAS = 0) states. It indicates that the received signaling buffer is not being updated, and that the slip buffer is being directed to read the old half of the Receive TS16 Buffer.

COMADet Change of Multiframe Alignment Detection—Set for one multiframe when the signaling multiframe alignment signal is first lost, then detected in a frame other than frame 0. This event may indicate an upstream frame slip. In CCS mode this bit is meaningless and should be ignored.

InMFCAS In Multiframe CAS—Set when the signaling multiframe alignment signal (CAS) is found in TS16. It is latched during frame 0 of each multiframe. This bit is meaningless and should be ignored in CCS mode.

LAPD Mode Operation

7	6	5	4	3	2	1	0
RxPtr[3]	RxPtr[2]	RxPtr[1]	RxPtr[0]	TS16AISDet	RxAbort	BadFCS	RxIdle

RxPtr[3] Receive Pointer [3]—Informs the microprocessor of which half of the Receive TS16 Buffer to read each time. The receiver will alternate halves. RxPtr[3] = 0 means that the lower half-buffer starting at 0x90 should be read; RxPtr[3] = 1 means that upper half-buffer starting at 0x98 should be read.

RxPtr[2:0] Receive Pointer [2:0]—A pointer indicating the highest numbered location in the Receive TS16 half-buffer that was written by the LAPD receiver. All messages must be an integral number of bytes in length. The receive circuit writes the first data byte received into location 0 (of the half-buffer), and counts upward.

TS16AISDet TS16 AIS Detect—Set when the all-ones signal is detected on TS16 for 16 frames.

RxAbort Receive Abort Flag—Indicates an abort flag (11111110) was received. The message in progress was aborted by the originator.

BadFCS Bad FCS—Indicates an erroneous Frame Check Sequence (FCS) was received at the end of the preceding message. It will remain set until a valid FCS is received.

RxIdle Receive Idle Code—Indicates the LAPD idle flag sequence (01111110) was received on TS16.

0x13—Framing Pattern Status Register (SR03)

The Framing Pattern Status Register contains the Reserved for International Use (Si bits) and the Remote Alarm Indication (referred to as the A-bit in G.704) bits in the framing pattern that was received during the most recent frame or multiframe. These bits are specified in ITU-T G.704 and G.706.

The host processor must read this register to recover the FEBE information received on the two E bits, once per CRC-4 multiframe. The Transmit or Receive CRC-4 Multiframe Interrupts [TxCRCMFItr, RxCRCMFItr;SR13.2,1] in the Interrupt Status Register [SR13.0x1F] may be used to time the reading of these bits. The Remote Alarm Indication is contained in the not-FAS word and is received and updated every other frame.

Also in this register are the error counter overflow indications. Each counter overflow interrupt status bit is cleared when the Framing Pattern Status Register is read, and does not affect the counter's operation.

7	6	5	4	3	2	1	0
Si1	Si0	RemAlmInd	Rsvd	IntOOMF	LCVOvfl	CRCOvfl	FASOvfl

Si1 Si1—The E-bit received during the not-FAS word in CRC MF frame 15.

Si0 Si0—The E-bit received during the not-FAS word in CRC MF frame 13.

RemAlmInd Remote Alarm Indication—Set high if the received A-bit is high. The A-bit is bit 3 of time slot 0 in not-FAS frames.

Rsvd Reserved—Used to enhance testability. It may change, but is functionally meaningless and should be ignored.

IntOOMF Integrated OOMF—High if two or more consecutive CAS multiframe alignment signal errors have been detected. This bit is cleared when valid CAS multiframe alignment has been found.

LCVOvfl LCV Error Counter Overflow—High when the Line Code Violation Counter [SR10;0x1C] equals 255, and is cleared when read. The counter will roll over to zero on the next error and resume counting, independent of when (or if) this bit is read.

CRCOvfl CRC Error Counter Overflow—High when the CRC Error Counter [SR11;0x1D] equals 255, and is cleared when read. The counter will roll over to zero on the next error and resume counting, independent of when (or if) this bit is read.

FASOvfl FAS Error Counter Overflow—High when the Frame Alignment Signal Error Counter [SR12;0x1E] equals 255, and is cleared when read. The counter will roll over to zero on the next error and resume counting, independent of when (or if) this bit is read.

Sa-Bit Registers

To aid ISDN and facility data link implementations, five registers are provided to minimize processor overhead for Sa-bit processing. Each register saves the state of each Sa-bit over the last CRC-4 multiframe. The Sa-bits are defined in ITU-T G.704 as additional spare bits reserved for international use.

Each bit is updated as it is received. The Receive CRC MF Interrupt signal [RxCRCMFItr;SR13.1] can be used to synchronize the reading of these bits. This ensures that the bits for each multiframe are read together as one word. Note that this process needs to be completed before the start of frame 1 when the new bits start to overwrite the old bits.

0x14–Sa4 Bits (SR04)

Status Register 0x04 records the Sa4 bits and is located at address 0x14. The bits retain a fixed relationship to the CRC-4 multiframe. Each bit is updated in turn when received.

7	6	5	4	3	2	1	0
RxSa4Frm15	RxSa4Frm13	RxSa4Frm11	RxSa4Frm9	RxSa4Frm7	RxSa4Frm5	RxSa4Frm3	RxSa4Frm1

0x15—Sa5 Bits (SR05)

Status Register 05 records the Sa5 bits and is located at address 0x15. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is updated in turn when received.

7	6	5	4	3	2	1	0
RxSa5Frm15	RxSa5Frm13	RxSa5Frm11	RxSa5Frm9	RxSa5Frm7	RxSa5Frm5	RxSa5Frm3	RxSa5Frm1

0x16—Sa6 Bits (SR06)

Status Register 06 records the Sa6 bits and is located at address 0x16. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is updated in turn when received.

7	6	5	4	3	2	1	0
RxSa6Frm15	RxSa6Frm13	RxSa6Frm11	RxSa6Frm9	RxSa6Frm7	RxSa6Frm5	RxSa6Frm3	RxSa6Frm1

0x17—Sa7 Bits (SR07)

Status Register 07 records the Sa7 bits and is located at address 0x17. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is updated in turn when received.

7	6	5	4	3	2	1	0
RxSa7Frm15	RxSa7Frm13	RxSa7Frm11	RxSa7Frm9	RxSa7Frm7	RxSa7Frm5	RxSa7Frm3	RxSa7Frm1

0x18—Sa8 Bits (SR08)

Status Register 08 records the Sa8 bits and is located at address 0x18. The individual bits retain a fixed relationship to the CRC-4 multiframe. Each bit is updated in turn when received.

7	6	5	4	3	2	1	0
RxSa8Frm15	RxSa8Frm13	RxSa8Frm11	RxSa8Frm9	RxSa8Frm7	RxSa8Frm5	RxSa8Frm3	RxSa8Frm1

0x19—Part Number and Hardware Version Register (SR09)

The Part Number and Hardware Version Register is located at address 0x19. This register allows the processor to verify which Brooktree product is working, and if that product is working with the correct integrated circuit revision. The part number is located in the upper nibble of the register. The revision number in the lower nibble. The revision number will be incremented with any change in circuitry within the integrated circuit.

7	6	5	4	3	2	1	0
Part[3]	Part[2]	Part[1]	Part[0]	Ver[3]	Ver[2]	Ver[1]	Ver[0]

Part[3:0] Part Number—A unique 4-bit code assigned to the Bt8510.

Ver[3:0] Version Number—Gives the version number of the part and is updated with each functional revision of the part starting with 0.

Part Number	Value	Former $Base_2$ Part Number
Bt8510EPJ	0x10	UGA-510
Bt8510EPJB	0x11	UGA-510-2
Bt8510EPJC	0x12	N/A

Error Counters

To aid certain implementations, three error counters are provided to minimize processor overhead. Interrupts can be enabled to activate upon overflow of one or more of the counters. Alternatively, the counters can be polled on a regular basis. If a loss of framing alignment is detected, the FAS and CRC error counters are disabled (but not cleared) until in frame alignment (InFrm = 1) is declared. The counters are cleared each time they are read by the microprocessor.

0x1C—Line Code Violation Counter (SR10)

The Line Code Violation Counter is located ar address 0x1C. In AMI mode (EnAMI = 1), all line code violations including bipolar violations will be counted. If the HDB3 decoder is enabled (EnAMI = 0), each bipolar violation with the same polarity of the previous bipolar violation will increment the counter per ITU-T Recommendation O.162. The counter has 8-bits, and will indicate 0–255 errors. If the counter overflows, the LCV Counter Overflow bit [LCVOvfl;SR03.2] in the Framing Pattern Status Register [SR03;0x12] will be set, and held until it is read. In this event, the counter will roll over and continue counting. An interrupt may be enabled upon overflow. The counter is cleared each time it is read.

7	6	5	4	3	2	1	0
LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]

0x1D—CRC Error Counter (SR11)

The CRC Error Counter is located at address 0x1D and is incremented upon each CRC-4 block error (one possible every 8 frames). The counter has 8 bits, and indicates 0–255 errors. If the counter overflows, the CRC Error Counter Overflow bit [CRCOvfl;SR03.1] in the Framing Pattern Status Register will be set and held until it is read. In this event, the counter will roll over and continue counting. An interrupt may be enabled upon overflow. The counter is cleared each time it is read. If CRC-4 multiframe alignment is lost, the counter is disabled until CRC-4 multiframe alignment is re-established. The counter typically records one error upon loss of CRC-4 multiframe alignment.

7	6	5	4	3	2	1	0
CRC4[7]	CRC4[6]	CRC4[5]	CRC4[4]	CRC4[3]	CRC4[2]	CRC4[1]	CRC4[0]

0x1E—Frame Alignment Signal Error Counter (SR12)

The Frame Alignment Signal Error Counter is located at address 0x1E and increments upon each FAS word in error. The counter has 8 bits, and indicates 0–255 errors. If the counter overflows, the FAS Error Counter Overflow bit [FASOvfl;SR03.0] in the Framing Pattern Status Register will be set, and held until it is read. In this event, the counter will roll over and continue counting. An interrupt may be enabled upon overflow. The counter is cleared each time it is read. System requirements will determine how often it must be read. If three consecutive FAS words are in error, the hardware will force a reframe operation unless the Inhibit/Abort Reframing bit [AbortRefrm;CR01.1] is set.

7	6	5	4	3	2	1	0
FAS[7]	FAS[6]	FAS[5]	FAS[4]	FAS[3]	FAS[2]	FAS[1]	FAS[0]

0x1F—Interrupt Status Register (SR13)

The Interrupt Status Register is located at address 0x1F and enables the microprocessor to quickly determine the interrupt source when several interrupts are enabled. LAPD interrupt sources and other indicators are also found in this register. All interrupts reported here are cleared when this register is read with the following exception: LAPD Receiver (bit 5) is cleared when the TS16 Status Register [SR02;0x12] is read.

7	6	5	4	3	2	1	0
RxSigHalf	LAPDHalf	LAPDRx	LAPDTx	RxOOFItr	TxCRCMFItr	RxCRCMFItr	RxCASMFItr

RxSigHalf Receive Signaling Sector (CAS or CCS)—Indicates the location of the valid signaling buffer half. A zero indicates the lower half [0x80–0x8F] and a one indicates the upper half [0x90–0x9F].

LAPDHalf LAPD Transmit Buffer Sector—Indicates which half of the transmit TS16 buffer should be written to. A one indicates the upper half [0xF8–0xFF] and a zero indicates the lower half [0xF0–0xF7].

LAPDRx LAPD Receiver—Indicates that a LAPD receiver has received a new message. This interrupt is cleared when the TS16 Status Register [SR02;0x12] is read.

LAPDTx LAPD Transmitter—Indicates that the LAPD transmitter is available to accept the next set of controls in the TS16 Control Register. This interrupt is cleared upon writing to the TS16 Control Register [CR02;0x02].

RxOOFItr Receive OOF Interrupt—Indicates a out-of-frame alignment state (InFrm = 0) in the receiver. This interrupt is cleared when the Interrupt Status Register is read.

TxCRCMFItr Transmitter CRC MF Interrupt—Indicates the beginning of each transmit multiframe. This interrupt is cleared when the Interrupt Status Register is read.

RxCRCMFItr Receive CRC MF Interrupt—Indicates the beginning of each receive CRC multiframe. This interrupt is cleared when the Interrupt Status Register is read.

RxCASMFItr Receive CAS MF Interrupt—Indicates the beginning of each receive CAS multiframe. This interrupt is cleared when the Interrupt Status Register is read.

Buffer Memory Registers

The microprocessor interface allows the indirect reading and direct writing of 256 locations in the RAM buffer memory. For any access to this memory space, RAMEN must be high.

When a write operation is performed, the Bt8510 latches the address and data and performs the write operation within the next microsecond. When a read operation is performed, the address is latched, and the read operation takes place within the next microsecond. A second read operation must then be performed to obtain the desired data at the controller.

The read operations can be pipelined. If 30 locations are to be read, the first operation should have the address of the first location. On the second read operation, the second address is presented and the data corresponding to the first location is returned to the controller. In this way N+1 operations are required to read N buffer locations. A read operation does not affect the contents of the memory. Write operations may be interleaved with pipelined read operations.

The maximum rate at which the buffer memory can be accessed is 1 MHz (976 ns clock period). This limitation does not apply to the control and status registers, only to accesses to the buffer memory registers. This rate may be doubled by using a 16.384 MHz system clock.

There are nine sets of buffer registers. Each set of registers contains a buffer register for each E1 channel, except for the TS16 Buffers. The functions of each register are:

- Receive Per-Channel Control
- Transmit Per-Channel Control
- Receive Idle Code
- Receive PCM Buffer
- Receive TS16 Buffer
- Transmit Idle Code
- Transmit PCM Buffer
- Receive TS16 Signaling Insertion Buffer
- Transmit TS16 Buffer

These are also described in the RAM address map in Table 6 through Table 14.

0x00–0x0F, 0x10–0x1F—Per-Channel Control Registers (RXCR, TXCR)

The Per-Channel Control Registers are located at addresses 0x00–0x0F for the receive time slots (RXCR), and addresses 0x10–0x1F for the transmit time slots (TXCR). Since these addresses are located in RAM buffer memory, the RAM Enable (RAMEN) pin must be high during the configuration accesses. The lower 3 bits of the address correspond to the *channel pair* number. Signaling control bits are grouped by channel pairs, as they are in the receive bit stream. For example, in location 0x0A the signaling controls operate on both channel 10 and 25 signaling bits, and are always contained in Time Slot 10. These registers must be initialized by the microprocessor upon power-up. Note that telephone channel number 25 is contained in Time Slot 26. Please see ITU-T Recommendation G.704, Table 9 for an explanation of the telephone channel numbering system. Note that because signaling bits are organized in channel pairs, both loopback and insert signaling are effective for the signaling associated with both Time Slot n, and Time Slot n+16.

7	6	5	4	3	2	1	0
IndTS TSn+16	IndTS TSn	InsertIdle TSn+16	EnLpDS0 TSn+16	LpSig TSn/TSn+16	InsertSig TSn/TSn+16	InsertIdle TSn	EnLpDS0 TSn

IndTS TSn+16 Indicate Time Slot (Time Slot n+16)—Enables the marking of the time slot on one of the time slot indication outputs, XINDY or SLINDY. For a transmit time slot, this register actually controls the indication for Time Slot n+16+2. That is, to indicate Time Slot 21, bit 7 in Per-Channel Control Register 5 (address 0x15) must be set. For a receive channel, no offset is required.

IndTS TSn Indicate Time Slot (Time Slot n)—Enables the marking of the time slot on one of the time slot indication outputs XINDY or SLINDY. For a transmit time slot, this register actually controls the indication for Time Slot n + 2. That is to indicate transmit Time Slot 7, bit 6 in Per-Channel Control Register 5 (address 0x15) must be set. For a receive channel, no offset is required.

InsIdle TSn+16 Insert Idle Code (Time Slot n+16)—Same function as for InsertIdleTSn but for the time slot n+16.

EnLpDS0 TSn+16 Enable DS0 Loopback (Time Slot n+16)—Enables the DS0 loopback for the selected time slot. For a receive channel, this causes a loopback toward the equipment. For a transmit channel, this causes a loopback toward the line.

LpSig TSn/TSn+16 Loopback Signaling (Time Slot n and n+16)—Loopback Signaling enables the signaling loopback for the signaling associated with the selected time slot. For a receive channel, this causes a loopback toward the equipment. For a transmit channel, this causes a loopback toward the line.

InsertSig TSn/ TSn+16 Insert Signaling (Time Slot n and n+16)—Causes the transmitter to read the Transmit TS16 Buffer for transmit data in TS16. Proper signaling information must have been previously written to these locations. On the receive side, the slip buffer will read the Receive TS16 Signaling Insertion Buffer for TS16 data inserted into the SLPPCMO output.

InsertIdle TSn Insert Idle Code (Time Slot n)—Causes the Transmit or Receive Idle Code Buffer for the selected time slot to be read, and that data transmitted. If InsertIdleTSn =0, the data is passed through from the serial input. The InsertIdleTSn bits for the transmit time slots control the idle code insertion into the transmitted E1 signal; the InsertIdleTSn bits for the receive time slots control the idle code insertion into the slip buffer data output (SLPPCMO). Unique idle codes for each of the 32 receive and 32 transmit time slots may be used simultaneously.

EnLpDS0 TSn Enable DS0 Loopback (Time Slot n)—Enables the DS0 loopback for the selected time slot. For a receive channel, this causes a loopback toward the equipment. For a transmit channel, this causes a loopback toward the line.

0x20–0x3F—Receive Idle Code (RXIDLE)

The Receive Idle Code Registers are located at addresses 0x20–0x3F. These registers contain the idle codes for insertion in the slip buffer output (SLPPCMO). Idle codes are inserted into the selected time slots as determined by the Receive Per-Channel Control Registers.

Receive Idle Code Word Format

7	6	5	4	3	2	1	0
RxIdle[7]	RxIdle[6]	RxIdle[5]	RxIdle[4]	RxIdle[3]	RxIdle[2]	RxIdle[1]	RxIdle[0]

0x40–0x5F—Receive PCM Buffer Low (RXLBUF)

The Receive PCM Buffer Low is located at addresses 0x40–0x5F. These registers make up the lower half of the slip buffer. The detailed operation is described in the Receiver Operation section of the Functional Descriptions chapter.

Low Slip Buffer PCM Word Format

7	6	5	4	3	2	1	0
RxLBuf[7]	RxLBuf[6]	RxLBuf[5]	RxLBuf[4]	RxLBuf[3]	RxLBuf[2]	RxLBuf[1]	RxLBuf[0]

0x60–0x7F—Receive PCM Buffer High (RXHBUF)

The Receive PCM Buffer High is located at addresses 0x60–0x7F. These registers make up the upper half of the slip buffer. The detailed operation is described in the Receiver Operation section of the Functional Description chapter.

High Slip Buffer PCM Word Format

7	6	5	4	3	2	1	0
RxHBuf[7]	RxHBuf[6]	RxHBuf[5]	RxHBuf[4]	RxHBuf[3]	RxHBuf[2]	RxHBuf[1]	RxHBuf[0]

0x80–0x9F—Receive TS16 Buffer (RXTS16)

The Receive TS16 Buffer is located at addresses 0x80–0x9F. These registers make up two halves of the Receive TS16 Buffer. In CCS and CAS signaling modes each buffer is alternately written by the framer for each multiframe. In LAPD mode, only the upper half of the buffer is written to by the LAPD receiver. The detailed operation is described in the Receiver Operation section of the Functional Description chapter.

CAS or CCS Signaling Format

7	6	5	4	3	2	1	0
RxTS16A	RxTS16B	RxTS16C	RxTS16D	RxTS16A	RxTS16B	RxTS16C	RxTS16D
TSn+16				TSn			

LAPD Message Byte Format

	6	5	4	3	2	1	0
LAPDMsg[7]	LAPDMsg[6]	LAPDMsg[5]	LAPDMsg[4]	LAPDMsg[3]	LAPDMsg[3]	LAPDMsg[2]	LAPDMsg[1]

0xA0–0xBF—Transmit Idle Code (TXIDLE)

The Transmit Idle Code registers are located at addresses 0xA0–0xBF. These registers contain the idle codes for insertion in the transmitter output. Idle codes are inserted into the selected time slots as determined by the Transmit Per-Channel Control Registers.

Transmit Idle Code Word Format

7	6	5	4	3	2	1	0
TxIdle[7]	TxIdle[6]	TxIdle[5]	TxIdle[5]	TxIdle[4]	TxIdle[2]	TxIdle[1]	TxIdle[0]

0xC0–0xDF—Transmit PCM Buffer (TXBUF)

The Transmit PCM Buffer Registers are located at address 0xC0–0xDF and contain the transmit PCM input data. Beginning address 0xC0 corresponds to timeslot 0 while ending address 0xDF corresponds to timeslot 31.

Transmit PCM Word Format

7	6	5	4	3	2	1	0
TxBuf[7]	TxBuf[6]	TxBuf[5]	TxBuf[4]	TxBuf[3]	TxBuf[2]	TxBuf[1]	TxBuf[0]

0xE0–0xEF—Receive TS16 Signaling Insertion Buffer (RXTS16SIG)

The Receive TS16 Signaling Insertion Buffer is located at addresses 0xE0–0xEF. These registers contain the signaling bits provided by the host for insertion into the slip buffer output (SLPPCMO). Signaling is inserted into the proper TS16 nibble position for selected time slot as determined by the Receive Per-Channel Control Registers.

Receive TS16 Signaling Format

7	6	5	4	3	2	1	0
RxTS16SigA	RxTS16SigB	RxTS16SigC	RxTS16SigD	RxTS16SigA	RxTS16SigB	RxTS16SigC	RxTS16SigD
TSn+16				TSn			

0xF0–0xFF—Transmit TS16 Buffer (TXTS16)

The Transmit TS16 Buffer is located at addresses 0xF0–0xFF. Signaling information is inserted into the proper TS16 nibble position for the selected time slot as determined by the Transmit Per-Channel Control Registers. In LAPD operation the 16-byte buffer is divided into halves, which are alternately read by the framer. The detailed operation is described in the LAPD Operation section in the Functional Description chapter.

CAS or CCS Signaling Format

7	6	5	4	3	2	1	0
TxTS16SigA	TxTS16SigB	TxTS16SigC	TxTS16SigD	TxTS16SigA	TxTS16SigB	TxTS16SigC	TxTS16SigD
TSn+16				TSn			

LAPD Message Byte Format

	6	5	4	3	2	1	0
LAPDMsg[7]	LAPDMsg[6]	LAPDMsg[5]	LAPDMsg[4]	LAPDMsg[3]	LAPDMsg[2]	LAPDMsg[1]	LAPDMsg[0]

Register Summary

Table 4. Control Registers

ADDR	Register Label	Read/ Write	Bit Number							
			7	6	5	4	3	2	1	0
0x00	CR00	R/W	PayLp	TxRxClk	EnAMI	TxAIS	EnFEBE	InsertFrm	InsertCRC	EnClkRcv
0x01	CR01	R/W	EnLAPDFmt	EnCAS	EnCCS	EnBitSlip	ShrtDly	FrcRefrm	AbortRefrm	AltCAS
0x02	CR02	R/W	TxX4	TxX3	Tx16RemAlm	TxX1	TxTS16AIS	FrzSig	EnSigFrz	InsertCASFrm
			TxPtr[3]	TxPtr[2]	TxPtr[1]	TxPtr[0]	TxTS16AIS	AbortMsg	TxFCS	TxIdle
0x03	CR03	R/W	Si1	Si0	TxRemAlm	IgnNotFAS	EnLocLp	EnLineLp	EnExtSig	EnAnalog
0x04	CR04	R/W	TxSa4Frm15	TxSa4Frm13	TxSa4Frm11	TxSa4Frm9	TxSa4Frm7	TxSa4Frm5	TxSa4Frm3	TxSa4Frm1
0x05	CR05	R/W	TxSa5Frm15	TxSa5Frm13	TxSa5Frm11	TxSa5Frm9	TxSa5Frm7	TxSa5Frm5	TxSa5Frm3	TxSa5Frm1
0x06	CR06	R/W	TxSa6Frm15	TxSa6Frm13	TxSa6Frm11	TxSa6Frm9	TxSa6Frm7	TxSa6Frm5	TxSa6Frm3	TxSa6Frm1
0x07	CR07	R/W	TxSa7Frm15	TxSa7Frm13	TxSa7Frm11	TxSa7Frm9	TxSa7Frm7	TxSa7Frm5	TxSa7Frm3	TxSa7Frm1
0x08	CR08	R/W	TxSa8Frm15	TxSa8Frm13	TxSa8Frm11	TxSa8Frm9	TxSa8Frm7	TxSa8Frm5	TxSa8Frm3	TxSa8Frm1
0x0F	CR09	R/W	LCVIE	CRCIE	FASIE	LAPDIE	RxOOFIE	TxCRCMFIE	RxCRCMFIE	RxCASMFIE

Table 5. Status Registers

ADDR	Register Label	Read/ Write	Bit Number							
			7	6	5	4	3	2	1	0
0x10	SR00	R	InCRCFrm	LCVDet	FASErr	InFrm	HDB3Det	AISDet	CRCFail	LOSDet
0x11	SR01	R	2msRxClk	2msTxClk	CtrlFrmSlp	COFADet	LOFAlign	UnctrlSlp	FrmSch1ms	BitSlip
0x12	SR02	R	RxX4	RxX3	MFRemAlm	RxX1	TS16AISDet	SigFrzSet	COMADet	InMFCAS
			RxPtr[3]	RxPtr[2]	RxPtr[1]	RxPtr[0]	TS16AISDet	RxAbort	BadFCS	RxIdle
0x13	SR03	R	Si1	Si0	RemAlmInd	Rsvd	IntOOMF	LCVOvfl	CRCOvfl	FASOvfl
0x14	SR04	R	RxSa4Frame15	RxSa4Frame13	RxSa4Frame11	RxSa4Frame9	RxSa4Frame7	RxSa4Frame5	RxSa4Frame3	RxSa4Frame1
0x15	SR05	R	RxSa5Frame15	RxSa5Frame13	RxSa5Frame11	RxSa5Frame9	RxSa5Frame7	RxSa5Frame5	RxSa5Frame3	RxSa5Frame1
0x16	SR06	R	RxSa6Frame15	RxSa6Frame13	RxSa6Frame11	RxSa6Frame9	RxSa6Frame7	RxSa6Frame5	RxSa6Frame3	RxSa6Frame1
0x17	SR07	R	RxSa7Frame15	RxSa7Frame13	RxSa7Frame11	RxSa7Frame9	RxSa7Frame7	RxSa7Frame5	RxSa7Frame3	RxSa7Frame1
0x18	SR08	R	RxSa8Frame15	RxSa8Frame13	RxSa8Frame11	RxSa8Frame9	RxSa8Frame7	RxSa8Frame5	RxSa8Frame3	RxSa8Frame1
0x19	SR09	R	Part[3]	Part[2]	Part[1]	Part[0]	Ver[3]	Ver[2]	Ver[1]	Ver[0]
0x1C	SR10	R	LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]
0x1D	SR11	R	CRC4[7]	CRC4[6]	CRC4[5]	CRC4[4]	CRC4[3]	CRC4[2]	CRC4[1]	CRC4[0]
0x1E	SR12	R	FAS[7]	FAS[6]	FAS[5]	FAS[4]	FAS[3]	FAS[2]	FAS[1]	FAS[0]
0x1F	SR13	R	RxSigHalf	LAPDHalf	LAPDRx	LAPDTx	RxOOFItr	TxCRCMFItr	RxCRCMFItr	RxCASMFItr

Table 6. Receive Per-Channel Control Registers

ADDR	Register Label	Read/ Write	Bit Number							
			7	6	5	4	3	2	1	0
0x00–0x0F	RXCR	R/W	IndTS TSn+16	IndTS TSn	InsertIdle TSn+16	EnLpDS0 TSn+16	LpSig TSn/TSn+16	InsertSig TSn/TSn+16	InsertIdle TSn	EnLpDS0 TSn

Table 7. Transmit Per-Channel Control Registers

ADDR	Register Label	Read/ Write	Bit Number							
			7	6	5	4	3	2	1	0
0x10–0x1F	TXCR	R/W	IndTS TSn+16	IndTS TSn	InsertIdle TSn+16	EnLpDS0 TSn+16	LpSig TSn/TSn+16	InsertSig TSn/TSn+16	InsertIdle TSn	EnLpDS0 TSn

Table 8. Receive Idle Code

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0x20–0x27	RXIDLE	R/W	Time Slot 7	•	•	•	•	•	•	Time Slot 0
0x28–0x2F		R/W	Time Slot 15	•	•	•	•	•	•	Time Slot 8
0x30–0x37		R/W	Time Slot 23	•	•	•	•	•	•	Time Slot 16
0x38–0x3F		R/W	Time Slot 31	•	•	•	•	•	•	Time Slot 24

Table 9. Receive PCM Buffer Low and High

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0x40–0x47	RXLBUF	R/W	Time Slot 7	•	•	•	•	•	•	Time Slot 0
0x48–0x4F		R/W	Time Slot 15	•	•	•	•	•	•	Time Slot 8
0x50–0x57		R/W	Time Slot 23	•	•	•	•	•	•	Time Slot 16
0x58–0x5F		R/W	Time Slot 31	•	•	•	•	•	•	Time Slot 24
0x60–0x67	RXHBUF	R/W	Time Slot 7	•	•	•	•	•	•	Time Slot 0
0x68–0x6F		R/W	Time Slot 15	•	•	•	•	•	•	Time Slot 8
0x70–0x77		R/W	Time Slot 23	•	•	•	•	•	•	Time Slot 16
0x78–0x7F		R/W	Time Slot 31	•	•	•	•	•	•	Time Slot 24

Table 10. Receive TS16 Buffer

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0x80–0x87	RXTS16	R/W	Time Slot 16 Frame 7	•	•	•	•	•	•	Time Slot 16 Frame 0
0x88–0x8F		R/W	Time Slot 16 Frame 15	•	•	•	•	•	•	Time Slot 16 Frame 8
0x90–0x97		R/W	Time Slot 16 Frame 23	•	•	•	•	•	•	Time Slot 16 Frame 16
0x98–0x9F		R/W	Time Slot 16 Frame 31	•	•	•	•	•	•	Time Slot 16 Frame 24

Table 11. Transmit Idle Code

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0xA0–0xA7	TxIDLE	R/W	Time Slot 7	•	•	•	•	•	•	Time Slot 0
0xA8–0xAF		R/W	Time Slot 15	•	•	•	•	•	•	Time Slot 8
0xB0–0xB7		R/W	Time Slot 23	•	•	•	•	•	•	Time Slot 16
0xB8–0xBF		R/W	Time Slot 31	•	•	•	•	•	•	Time Slot 24

Table 12. Transmit PCM Buffer

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0xC0–0xC7	TXBUF	R/W	Time Slot 7	•	•	•	•	•	•	Time Slot 0
0xC8–0xCF		R/W	Time Slot 15	•	•	•	•	•	•	Time Slot 8
0xD0–0xD7		R/W	Time Slot 23	•	•	•	•	•	•	Time Slot 16
0xD8–0xDF		R/W	Time Slot 31	•	•	•	•	•	•	Time Slot 24

Table 13. Receive TS16 Signaling Insertion Buffer

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0xE0–0xE7	RXTS16SIG	R/W	Time Slot 16 Frame 7	.	.	.	.	.	.	Time Slot 16 Frame 0
0xE8–0xEF		R/W	Time Slot 16 Frame 15	.	.	.	.	.	.	Time Slot 16 Frame 8

Table 14. Transmit TS16 Buffer

ADDR	Register Label	Read/ Write	Byte Number							
			7	6	5	4	3	2	1	0
0xF0–0xF7	TXTS16	R/W	Time Slot 16 Frame 7	.	.	.	.	.	.	Time Slot 16 Frame 0
0xF8–0xFF		R/W	Time Slot 16 Frame 15	.	.	.	.	.	.	Time Slot 16 Frame 8

AC Characteristics

All signal outputs are guaranteed to settle beyond both TTL and CMOS worst-case input thresholds into a load capacitance of up to 50 pF within 40 ns of the corresponding clock transition. See Table 15 and Table 16.

Table 15. Delay Characteristics

Section	Description	Max	Units
Transmitter	XCKI to XCKO	20	ns
	XCKI to XSYNCO	20	ns
	XCKI to XINDY	20	ns
	XPCMI to XPCMO	14	Cycles of XCKO
	XPCMI to XPOSO and XNEGO	18	Cycles of XCKO
Receiver	RCKI to RCKO	20	ns
	RCKI to RPCMO	20	ns
	RPOSI and RNEGI to RPCMO	6	Cycles of RCKO [1]
Slip Buffer	SLPCKI to SLINDY	20	ns
	SLPCKI to SLPPCMO	20	ns
	SLPCKI to SLPSYNCO	20	ns
	RPCMO to SLPPCMO	30	Cycles of SLPCKI [2]
General	CK32I to CK160	20	ns
	SYSCKI to BITCK0	20	ns

1. This refers to internal or external clock recovery
2. Slip buffer short delay mode, initial delay upon reframe

Table 16. Analog Interface Characteristics

Parameter	Minimum	Maximum	Units
Operating Temperature Range	–40	+85	°C
Supply Voltage	4.75	5.25	Volts
Cable Impedance	75	120	Ohms
Signal Level	2.40	3.0	Volts Peak
Input Impedance	5,000	—	Ohms
ESD Protection	3,000	—	Volts
Latch-up Protection	150	—	mA
Power-Down Current	—	500	µA

DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. All outputs are CMOS drive levels and can be used with CMOS or TTL logic. Specific characteristics are given in Table 17 and apply over a temperature range of –40° C to +85° C and a supply voltage of 4.75 to 5.25 volts unless otherwise noted.

Table 17. DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{OH}	Output Voltage High	I_{OH} = – 20 uA	2.4	–	–	V
V_{OL}	Output Voltage Low	I_{OL} = – 4 mA	–	0.2	0.4	V
V_{IH}	Input Voltage High		2.0	–	–	V
V_{IL}	Input Voltage Low		–	–	0.8	V
I_{DD}	Supply Current	Analog Receiver/Transmitter Active and Line Driver Sending AIS (all 1's).	–	45	100	mA
I_{IL}	Input Leakage Current		–	±1.0	±10	uA
C_{IN}	Input Capacitance		–	–	10	pF
C_{OUT}	Output Capacitance	All Output and I/O Pins	–	–	10	pF
–	ESD Protection	MIL-STD-883C Method 3015	2	>3	–	kV
–	Latch-up Input	JEDEC JC-40.2	150	>400	–	mA

Microprocessor Interface – 68HC11

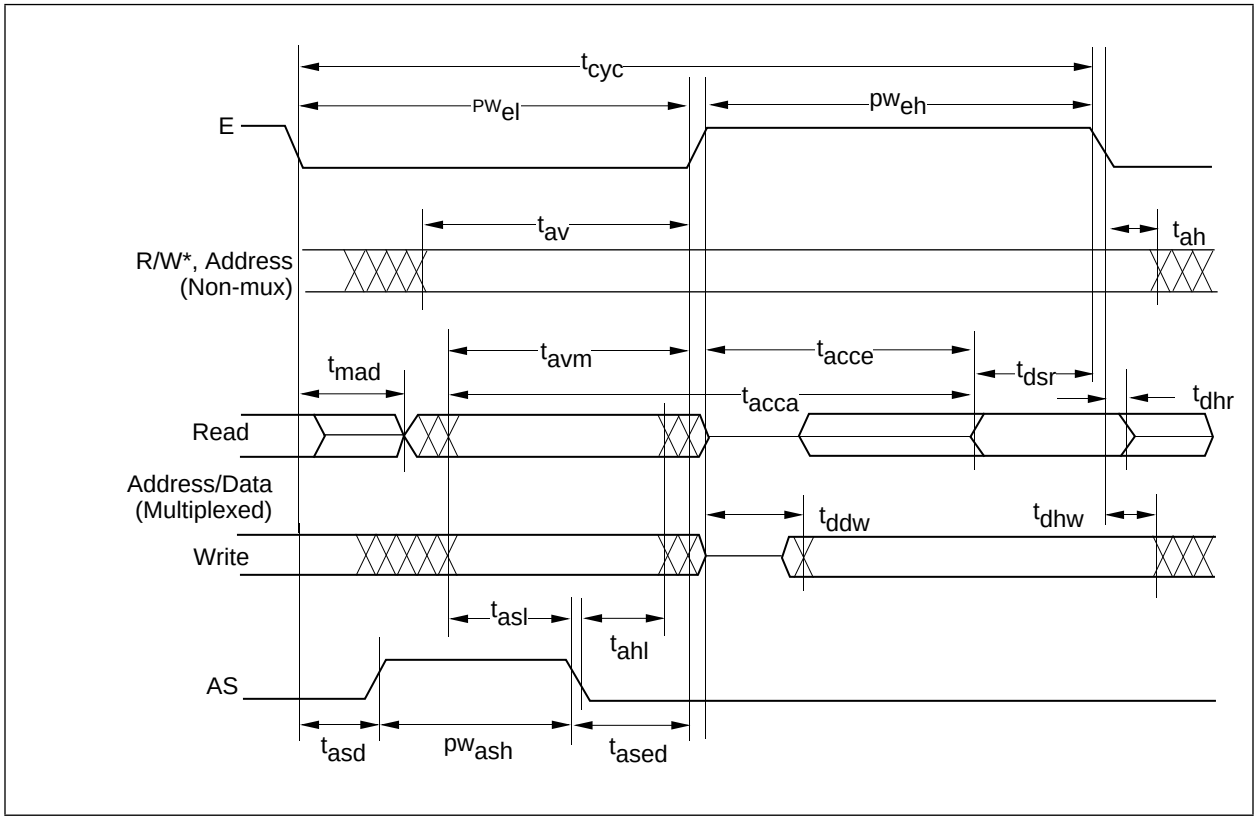
These specifications are taken from *Motorola Microprocessor, Microcontroller, and Peripheral Data Vol. 2 (Q3/88)* for an MC68HC11A8 running at 2.1 MHz E clock frequency. Timing of other versions may differ. See characteristic timing in Table 18 and Figure 16.

All clock inputs should have a duty cycle of between 45% and 55%. Although most internal functions are clocked on the rising edge, some do use the falling edge. To guarantee enough time between rising and falling edges, this requirement should be met.

Table 18. 68HC11 MPU Bus Interface Characteristics

Symbol	Parameter (Times in Nanoseconds)	68HC11 Spec	Bt8510 Spec
t_{cyc}	Cycle Time	476 min	154 min
pw_{el}	Pulse Width E Low	215 min	77 min
pw_{eh}	Pulse Width E High	210 min	77 min
t_{av}	Non-muxed Address Valid to E Rise	85 min	30 min
t_{ah}	Address Hold Time	30 min	0 min
t_{mad}	Muxed Address Delay	80 min	0 min
t_{avm}	Muxed Address Valid to E Rise	75 min	0 min
t_{acce}	MPU Access Time	180 max	36 max
t_{acca}	MPU Address Access Time	275 min	100 min
t_{dsr}	Read Data Setup Time	30 min	40 min
t_{dhr}	Read Data Hold Time	10 to 80	12 min–32 max
t_{ddw}	Write Data Delay Time	125 max	0 min
t_{dhw}	Write Data Hold Time	30 min	5 min
t_{asl}	Muxed Address Valid Time to AS Fall	20 min	5 min
t_{ahl}	Muxed Address Hold Time	30 min	5 min
t_{asd}	Delay Time, E to AS Rise	50 min	10 min
pw_{ash}	Pulse Width, AS High	90 min	34 min
t_{ased}	Delay Time, AS to E Rise	50 min	20 min
t_{rf}	All Rise and Fall Times	20 max	25 max

Figure 16. 68HC11 Timing Diagram



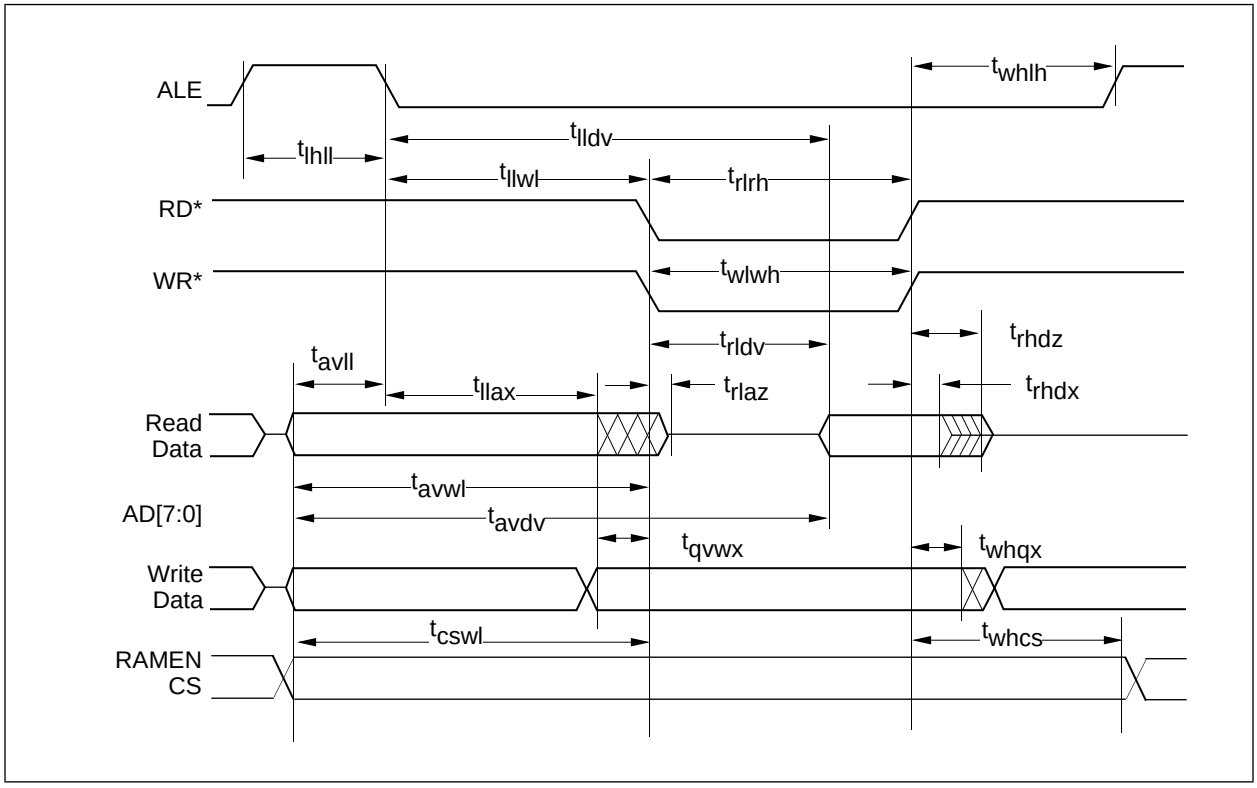
Microprocessor Interface – 80C51

These specifications are taken from *Intel 8-Bit Embedded Controllers, 1990* for an 80C31BH-1 running at a 16 MHz oscillator frequency. Timing of other versions may differ. See Table 19 and Figure 17.

Table 19. 80C51 MPU Bus Interface Characteristics

Symbol	Parameter (Times in Nanoseconds)	80C51 Spec	Bt8510 Spec
t_{lhll}	ALE Pulse Width	85 min	10 min
t_{avll}	Address Valid to ALE Low	7.5 min	5 min
t_{llax}	Address Hold After ALE Low	27.5 min	5 min
t_{rlrh}	RD* Pulse Width	275 min	25 min
t_{wlwh}	WR* Pulse Width	275 min	25 min
t_{rldv}	RD* Low to Valid Data In	147.5 min	36 max
t_{rhdx}	Data Hold After RD*	0 min	12 min
t_{rhdz}	Data Float after RD*	55 Max	32 max
t_{lldv}	ALE Low to Valid Data In	350 Max	n/a[1]
t_{avdv}	Address to Valid Data In	397 Max	n/a[1]
t_{llwl}	ALE Low to RD* or WR* Low	137–238	5 min
t_{avwl}	Address Valid to RD* or WR* Low	120 Min	n/a[1]
t_{qvwx}	Data Valid to WR* Transition	2.5 Min	n/a[1]
t_{whqx}	Data Hold after WR*	12.5 Min	5 min
t_{rlaz}	RD* Low to Address Float	0 Max	5 max
t_{whlh}	RD* or WR* High to ALE High	22.5–102.5	8 min
t_{cswl}	CS, RAMEN to RD* or WR* Low	n/a	15 min
t_{whcs}	RD* or WR* High to CS, RAMEN	n/a	15 min
1. The circuit is not affected by this specification			

Figure 17. 80C51 Timing Diagram



Environmental Conditions

Power Requirements and Temperature Range

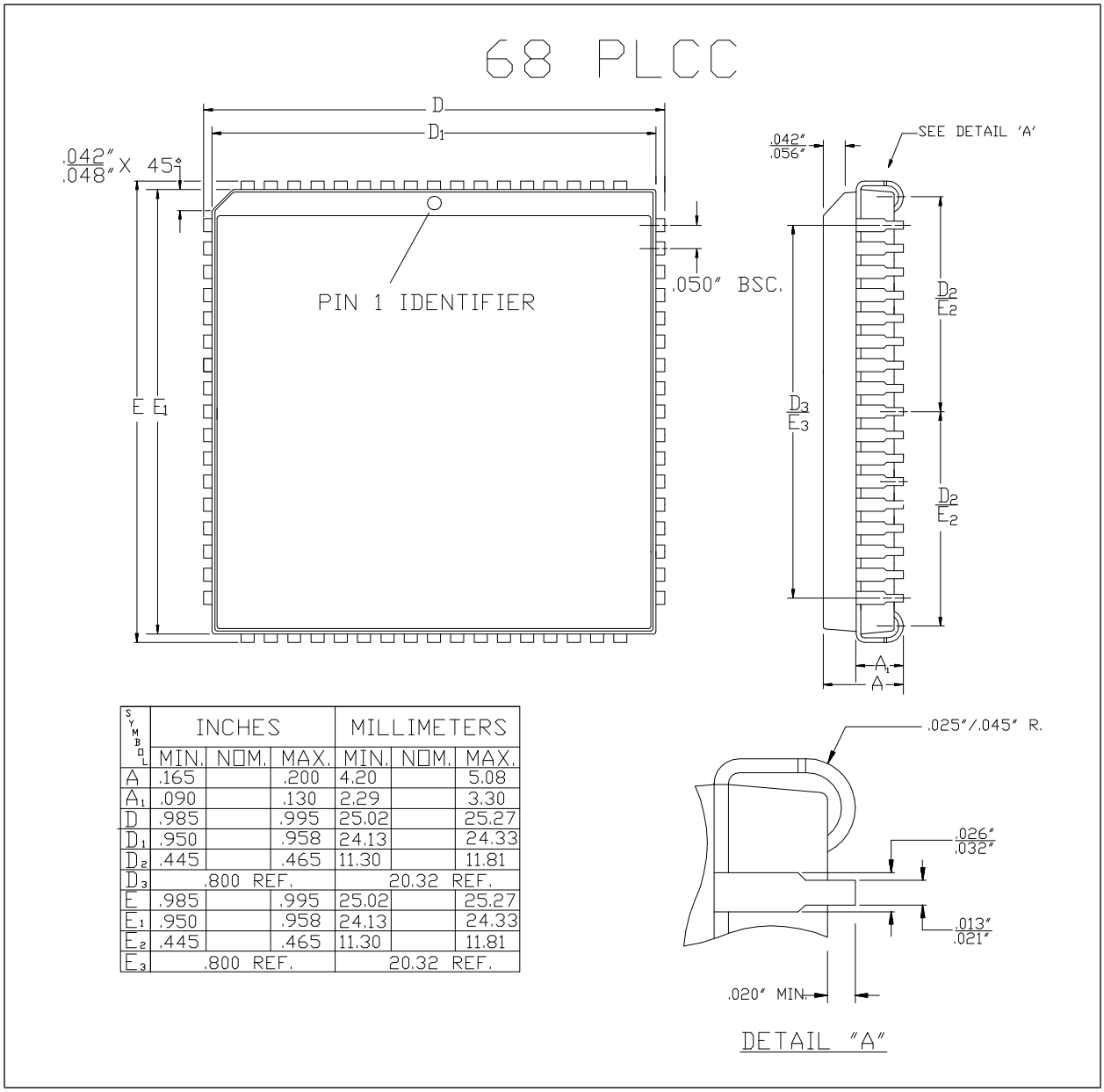
Stresses above those listed as *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. See Table 20.

Table 20. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC Power Supply Voltage	–0.5 to 7.0	Volts
V_{IN}, V_{OUT}	DC Input, Output Voltage	–0.5 to V_{DD} + 0.5	Volts
I	DC Current Drain Per Pin, Any Input or Output	25	mA
T_{STG}	Storage Temperature	–55 to +150	°C
T_L	Lead Temperature (less than 10 second soldering)	250	°C
T_{OPER}	Operating Temperature	–40 to +85	°C

Mechanical Specifications

Figure 18. 68-Pin Plastic Leaded Chip Carrier (J-Bend)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D_1	.950		.958	24.13		24.33
D_2	.445		.465	11.30		11.81
D_3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E_1	.950		.958	24.13		24.33
E_2	.445		.465	11.30		11.81
E_3	.800 REF.			20.32 REF.		

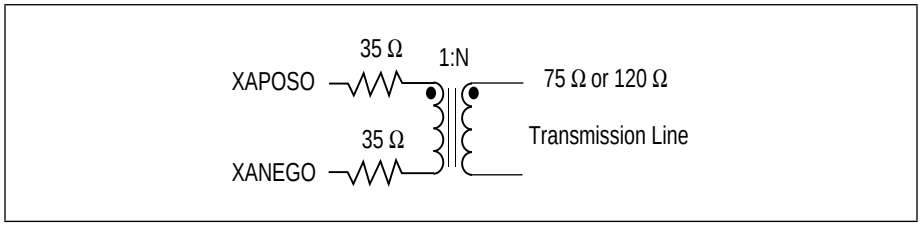
Appendix A

Application Circuits

Transmitter

The circuits in Figure A–1 and Figure A–2 illustrate how to interface the transmitter and receiver analog interface to E1 lines through separately packaged transformers. Return loss information is given in Appendix C.

Figure A–1. Transmitter Transformer

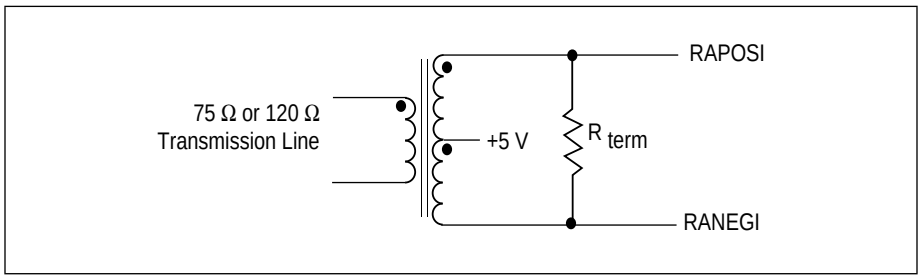


- Transformer is Pulse Engineering PE-64934 or equivalent, 1:1 ratio.
- For a 75 Ω line the transformer is Pulse Engineering PE-64934 or equivalent, 1:1 ratio (N = 1).
- For a 120 Ω line the transformer is Pulse Engineering PE-64938 or equivalent, 1:1.26 ratio (N = 1.26)
- For a configurable application, dual transformers, such as the Pulse Engineering PE-65389 (1:1:1.26 ratio), are available.

Receiver

For receive termination information refer to Appendix C.

Figure A–2. Receiver Transformer



- Transformer is Pulse Engineering PE-64931 or equivalent, 1:1:1 or 1:2CT ratio.
- $R_{term} = Z_{line}$ X 4 = 301 Ω, 1% for 75 Ω line = 511 Ω, 1% for 120 Ω line.

Appendix B

Bt8510 Analog Drop and Insert in a Local Area Network

Introduction

This appendix describes an analog drop-and-insert local area network multiplexing 31 PCM voice channels onto a 2.048 Mb/s digital line. Each station can be separated by up to 500 feet with no additional components. The digital line uses the ITU-T standard protocols (CEPT or E1) detailed in G.703, G.704, G.706, and G.732.

A ring network is described and a possible control protocol is presented. A simple form of line compression is used by assigning time slots to each station on a request basis. This allows any 31 of a possible 255 stations to be active at one time.

The time slot indicators can be used to interface an analog codec directly. A multiplexer is required in the transmit direction to insert the transmit data.

Performance

Voice quality is standard A-law PCM voice coding, as per ITU-T G.711. By using the short delay mode in the framer's slip buffer, the through delay for each active station is about 20 µsec. For a fully active network of 31 channels, the total delay is 610 µsec. A station not in use is looped from receive to transmit to avoid adding additional delay.

Network Timing

Digital timing recovery from the 2.048 Mb/s line is included in the analog interface on-chip. Jitter must be filtered from this clock to provide a clean transmit clock. This is done in a catalog part, a 4046 CMOS phase-locked loop.

Signaling and Control Protocol

A dedicated pin must be provided on the microcontroller to sense on-hook and off-hook states. All other signaling is done in-band using the DTMF functions in the telephone.

Control of individual stations is accomplished using the Sa-bits in the standard CEPT framing format. Together, they form a control channel of 20 kb/s bandwidth. Forty Sa bits are updated every 2 ms and are simultaneously known to every station throughout the network. A simple possible protocol follows:

The managing entity is called the Head-of-Bus (HOB). The convention for each station is that if the required word is received as zero, it may be used. If it is anything but zero, it must be repeated to the transmitter. The station will not be able to use the control bandwidth until that word is received as all zeros, indicating that no station upstream is using it. This does give some priority to those stations nearest the head of bus.

Sa4[7:0] This word conveys a message from a station by sending the HOB its station number in this slot, and the request in another field. The request would usually be for a time slot assignment due to an off-hook condition, or the conveyance of an on-hook (user hung up).

Sa5[7:0] This word addresses a station by the HOB. The instruction from the HOB is in one of the other fields.

Sa6[7:0] This word conveys a time slot assignment from the HOB to the station. Transmit and receive functions use the same time slot.

Sa7[7:0] This word specifies the request from a station, and also reports an error rate or other functional problems for maintenance.

Sa8[7:0] This word is reserved for future use.

Maintenance

Each station is assigned a number by setting a dip switch upon installation. The control protocol includes identification of a faulty station by station number, allowing prompt service. While in service, a partially failed station may be instructed to go into loopback mode to avoid losing the entire ring. A manual switch can switch out a totally failed station. The microprocessor reads the dip-stick setting upon power-up, enabling the use of a common software module for all stations.

To avoid the problem of one failed unit killing the entire network due to the serial connection, a bypass relay can be used to bypass a failed station. By wiring the relay to bypass when unenergized, a power failure will automatically take the failed station out of the circuit. A watchdog timer can be employed to cause a loopback any time a *sanity* signal from the local processor stops toggling.

Appendix C

Bt8510 Return Loss, Receive Termination, and Receiver Jitter Tolerance

Return Loss

The general formula for calculating return loss is:

$$Return\ Loss\ =\ 20\log\left(\frac{|Z_s - Z_t|}{Z_s + Z_t}\right)$$

where Z_t is the terminating impedance and Z_s is the source impedance.

Receiver

For the receiver, Z_s is the line impedance and is nominally either 75 or 120 ohms. A receiver terminating resistor, R_{term}, is chosen such that $Z_t = R_{term}/4$ in order to match the terminating impedance to the line through the 1:1:1 transformer. For a 75 ohm line, a 301 Ω ±1% resistor is chosen for R_{term}, while a 511 Ω ±1% value is used for the 120 ohm line impedance.

Ignoring the framer input impedance and assuming a perfect transformer, the 1% variation of R_{term} combined with the error in choosing the closest 1% value will cause the return loss to be –43.6 dB for the 75 ohm line and –31.6 dB for the 120 ohm line.

The actual terminating impedance is a function of the terminating resistor, R_{term}, in parallel with the input impedance of the receiver inputs. This input impedance is specified to be at least 5 kΩ per pin which degrades the return loss to –34.8 dB for the 75 ohm line. The 120 ohm line return loss improves to –38.9 dB. Note that taking the chip input impedance into account reduces the effective R_{term} value. This explains why a 511 Ω resistor is a better choice than a 475 Ω value.

ITU–T Recommendation G.703, paragraph 6.3.3 provides for a minimum return loss value of –18 dB from 102 kHz to 2,048 kHz. A typical transformer will be guaranteed to meet this minimum return loss requirement (see Pulse Engineering Application Note AN906-8, 11/90). From the above analysis it should be clear that the transformer will be the dominant factor in determining the return loss at the line interface.

Transmitter

For the transmitter, we have a driver specified to have an output impedance of 5 ±2 Ω. We also have two 35.7 Ω ±1% resistors in series for both the 75 and 120 ohm cable interfaces. This gives a total series resistance of between 117.0 Ω and 125.6 Ω. From transformer theory we know Z_s is the turns ratio squared times the series resistance through the transmitter outputs.

The 75 ohm line uses a transformer with a turns ratio of 1:1 yielding a worst case return loss of –31.5 dB, ignoring the transformer return loss. Since zeros and ones are driven equally (that is, zeros are not three-stated), this is a steady value. Again, the transformer will dominate the return loss measured at the line interface.

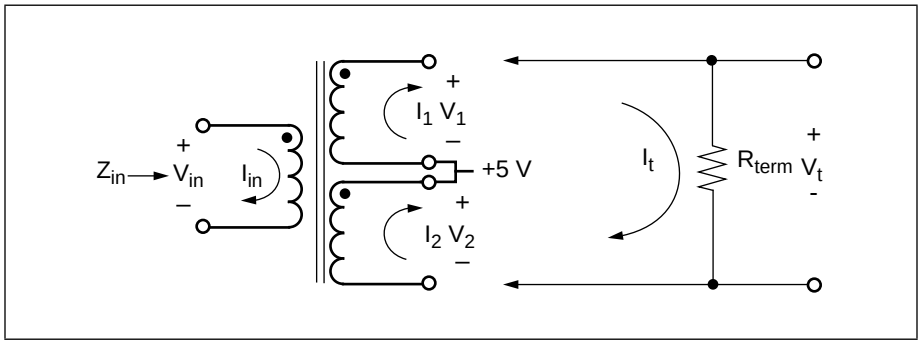
The 120 ohm line uses a 1:1.26 transformer giving a worst case return loss of –32.8 dB, ignoring the transformer return loss. Once again, the transformer will dominate the return loss measured at the line interface.

Since the transformer is the critical component in the design for this parameter, return loss is not directly specified in the Bt8510 interface specification. The board designer must choose a transformer that is good enough to meet the specifications, and must also ensure that the layout is clean enough to not further degrade return loss.

Receive Termination

In Figure 1, the line impedance is given as Z_{in} and the receiver terminating resistor is R_{term}. The transformer is a 1:1:1 or a 1:2 with center tap.

Figure C–1. Bt8510 Receive Termination Equivalent Circuit



Therefore

$$I_t = I_1 = I_2$$

from transformer theory

$$I_{in} = I_1 + I_2$$

So

$$I_t = I_{in} / 2$$

Also

$$V_1 = V_2 = V_{in}$$

So

$$V_t = V_1 + V_2$$

or

$$V_t = 2\ V_{in}$$

and

$$Z_{in} = V_{in} / I_{in}$$

We want Z_{in} to equal the cable impedance, so choose a value of R_{term} where

$$R_{term} = V_t / I_t$$

substituting

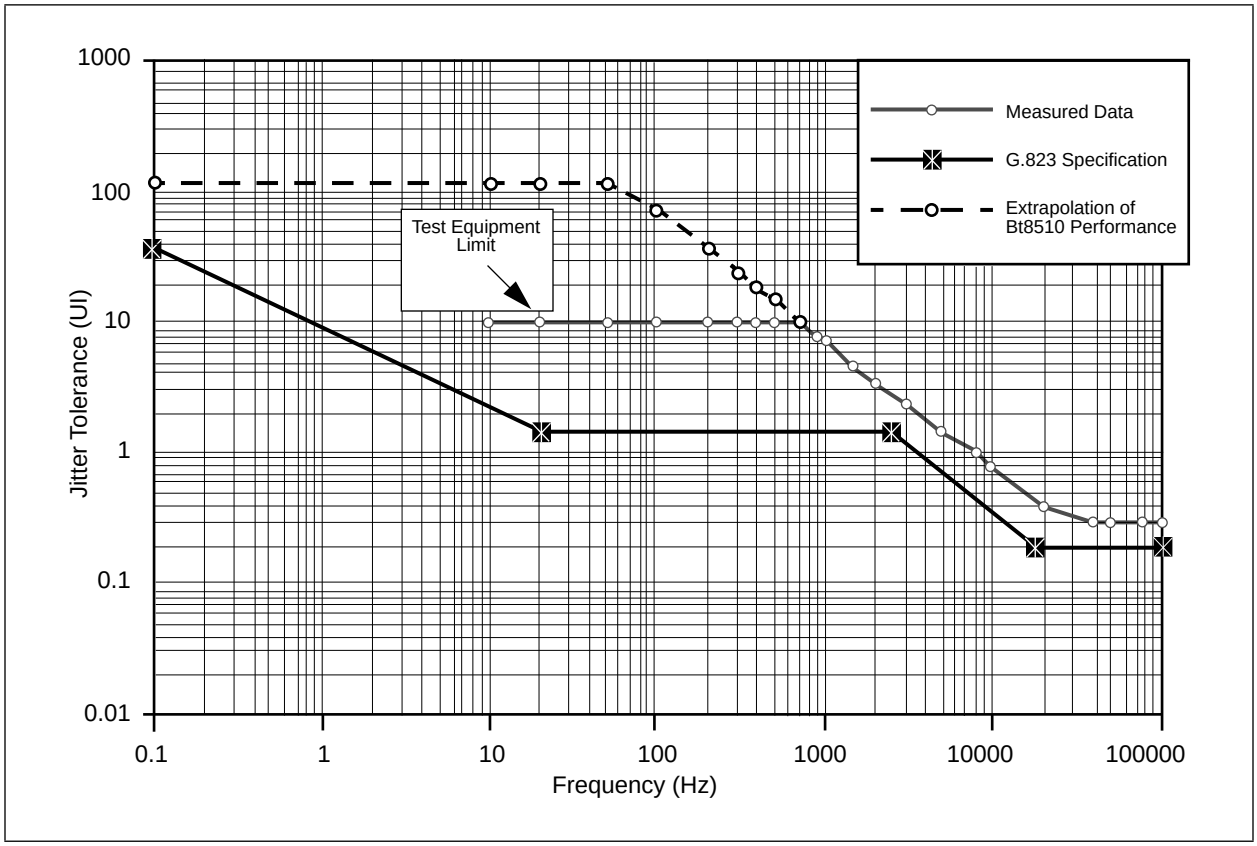
$$R_{term} = 2\ V_{in} / (I_{in} / 2) = 4\ V_{in} / I_{in}$$
$$= 4\ Z_{in}$$

In other words, for a 75 ohm line use a 301 Ω, 1% resistor and for a 120 ohm line use a 511 Ω, 1% value.

Receiver Jitter Tolerance

The jitter tolerance of the digital clock recovery circuit on the Bt8510 has been tested with an HP-3785B jitter test set. This test set is limited to a maximum of 10 Unit Intervals (UIs) of jitter. The nature of the clock recovery circuit is such that it will tolerate a product of the frequency and amplitude of jitter at low frequencies, and that is the basis of the extrapolation presented on the chart. The maximum jitter tolerated is 118 UI, which is the depth of the slip buffer. Jitter amplitudes greater than 118 UI cause controlled frame slips and, therefore, errors. As is apparent from the chart in Figure C–2, the digital clock recovery circuit on the Bt8510 easily meets the minimum jitter tolerance specified in ITU-T Specification G.823.

Figure C–2. Bt8510 Receiver Jitter Tolerance Graph



Appendix D

Bt8510 Receiver Sensitivity and Signal Reflection Immunity

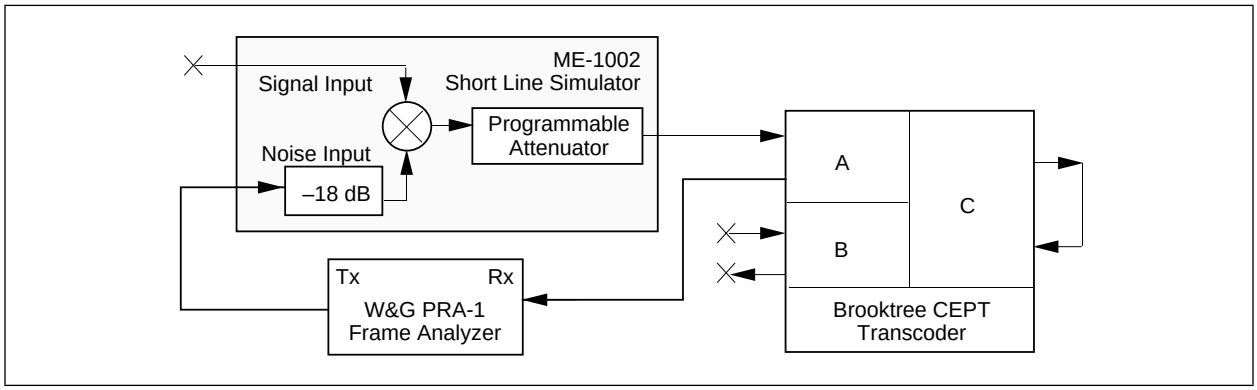
Introduction

According to ITU–T Recommendation G.703, paragraphs 6.3.1 and 6.3.4, an input port must be designed to accommodate a signal-to-interference ratio of 18 dB which is attenuated by the characteristic of an interconnecting pair in the range of 0 to 6 dB.

Receiver Sensitivity

The data pattern generated by the W&G PRA-1 Frame Analyzer is passed through the ME-1002 Short Line Simulator and into the Bt8510 receiver on the Brooktree CEPT Evaluation Board. The signal is then passed through the CEPT transcoder C port via a clear channel and returned to the W&G PRA-1 receiver. A continuous 64 kb/s Bit Error Rate (BER) test is run on the data in order to monitor errors in the transmission path. This setup is shown in Figure D-1.

Figure D–1. Receiver Sensitivity Test Set-Up



The maximum programmable attenuation on the ME-1002 is 15.5 dB. At this level the Bt8510 had zero errors. To decrease the signal level further, we fed the signal into the ME-1002 via the noise input port. This provided a fixed 18 dB of attenuation. The signal could then be attenuated further by the programmable attenuator. The Bt8510 receiver was able to recover the data error free with an additional 2 dB of attenuation. This is summarized as follows:

Signal to Interference Ratio (S/I) = ∞,
Attenuation with 0 BER ≥ 20 dB

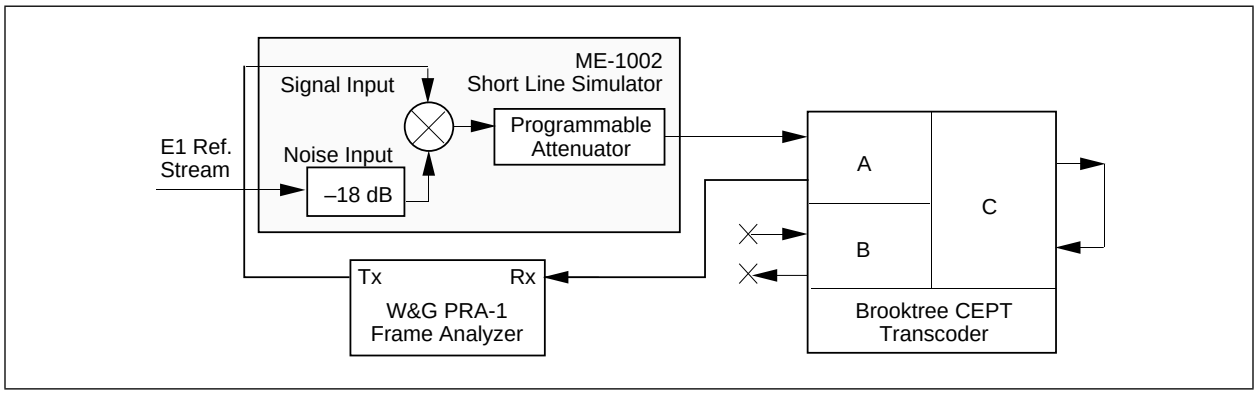
Signal Reflection Immunity

The signal reflection immunity test setup is similar to the receiver sensitivity test (see Figure D-2). The W&G PRA-1 output is connected to the signal input of the ME-1002, and the E1 reference stream (noise source) is a Brooktree Bt8510 Evaluation Board transmitting idle code.

The Bt8510 receiver was able to recover the data error free under these conditions with the programmable attenuator set to the maximum 15.5 dB. This is summarized below. This documents that the ITU–T G.703 requirement of at least 6 dB of attenuation is accommodated by the Bt8510.

Signal to Interference Ratio (S/I) = 18 dB,
Attenuation with 0 BER ≥ 15.5 dB

Figure D–2. Signal Reflection Immunity Test Set-Up



Equipment

ME-1002 Short Line Simulator
Mountain Engineering & Technology
123 Genesee Ct.
Boulder, CO 80303
(303) 494-9120

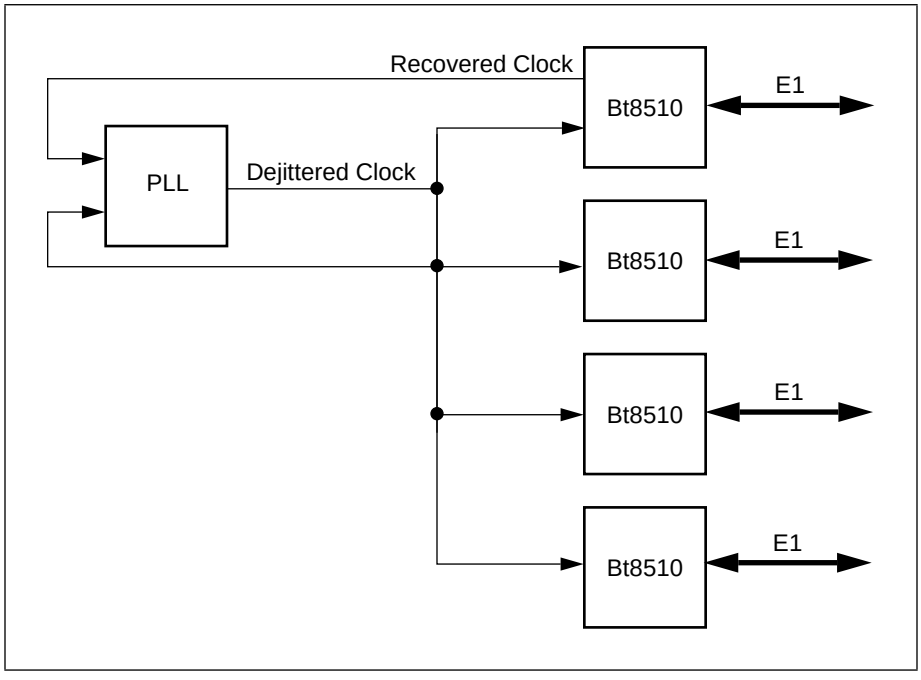
W&G PRA-1 Frame Analyzer
Wandel and Golterman Inc.
990 North Bowser Road, Suite 780
Richardson, TX 75081
(214) 231-8923

Appendix E

A Phase-Locked Loop (PLL) to Meet ITU–T G.823 Jitter Attenuation Requirements

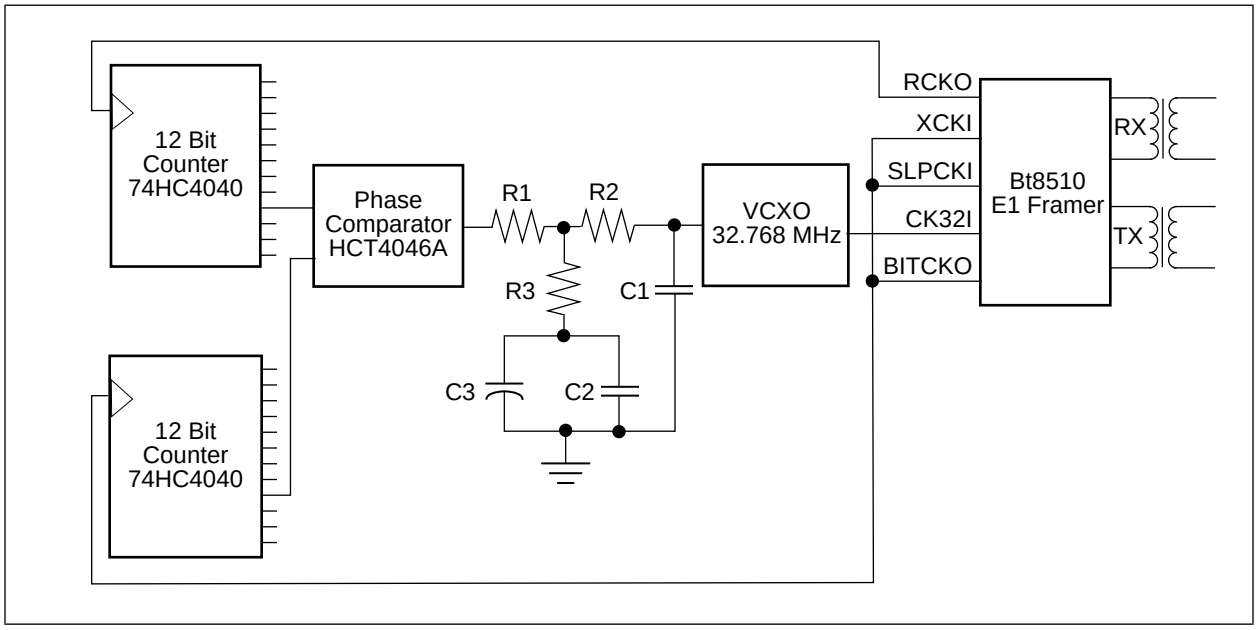
In certain loop timing configurations, a system may require a phase-locked looped in order to provide jitter attenuation and clock smoothing. A system might have a bank of framers where one will be selected to provide timing for the unit. Figure E–1 illustrates such a configuration.

Figure E–1. System Clock Dejittering



A common PLL implementation uses a VCXO. This PLL offers excellent jitter attenuation as a result of the inherent VCXO characteristics. The Bt8360/8510 EVM Evaluation Module employs such a circuit. This circuit, shown below in Figure E–2, uses a 32.768 MHz VCXO, two counters, a phase comparator and a passive loop filter. The recovered clock, RCKO, is used for one counter. The VCXO output divided by 16 (performed by the Bt8510) is used for the other counter. The counters ensure that the phase detector will not miss an edge in the presence of high amplitude jitter. The two counter outputs are routed to the phase comparator. The output of the phase comparator is filtered and used to drive the VCXO. The output of the VCXO sources the Bt8510 input, CK32I. CK16O can then be used as the Bt8510 system clock, SYSCKI. The VCXO replaces the need for a 16.384 MHz crystal oscillator. BITCKO provides the source for the Transmit clock and the Slip Buffer clock.

Figure E–2. 32.768 MHz VCXO



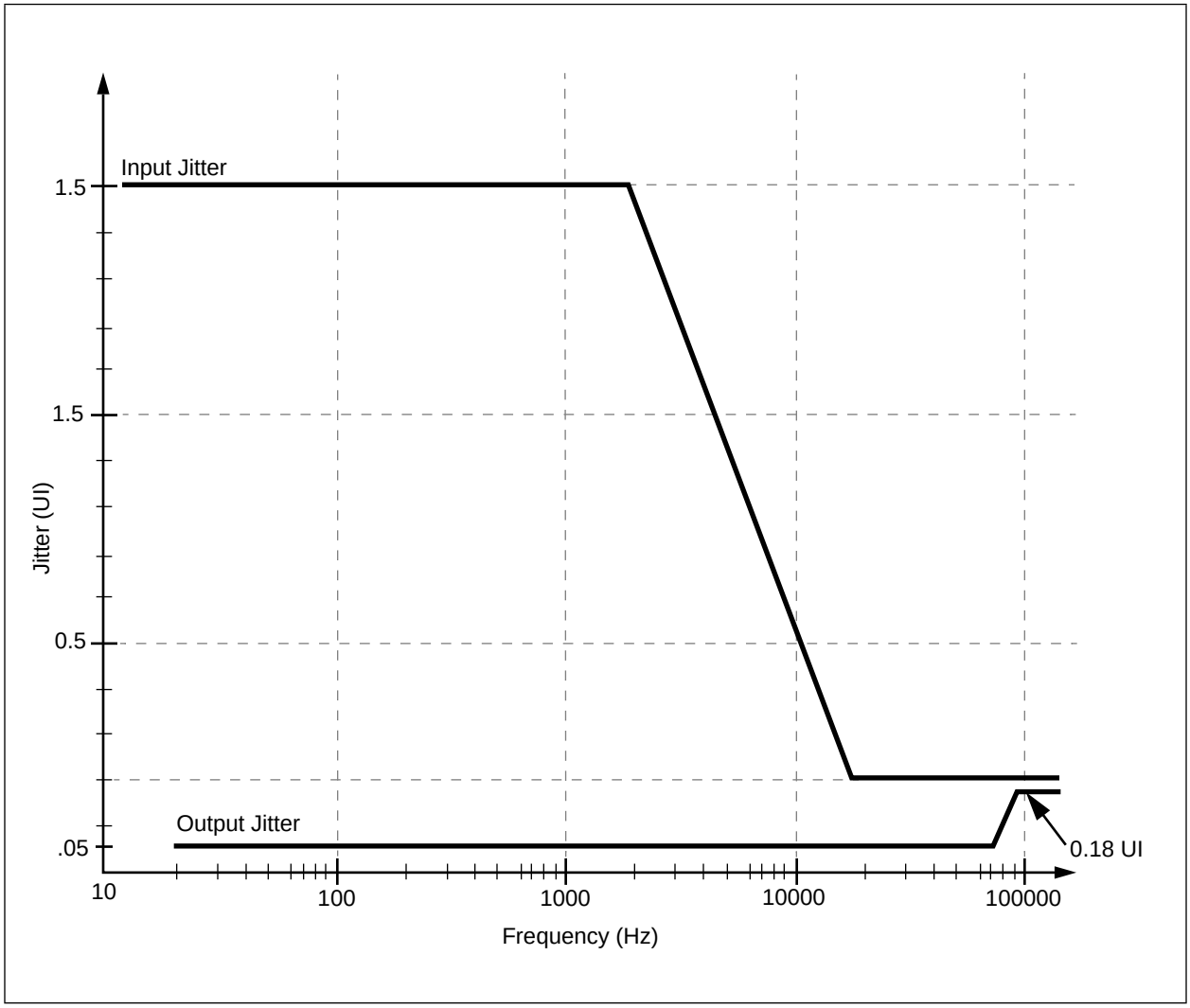
R1 = 10KΩ	R2 = 1KΩ	R3 = 4.7KΩ
C1 = 0.015µF	C2 = 0.1µF	C3 = 4.7µF

Brooktree recommends the following manufacturer for the VCXO:

Connor-Winfield Oscillators
2111 Comprehensive Drive
Aurora, IL 60505
TEL: 1 (708) 851-4722
FAX: 1 (708) 851-5040
Part # HV53-200
Freq: 32.768MHz

Performance of this circuit was measured and found to meet or exceed CCITT G.823 requirements. Figure E–3 show G.823 specification and circuit performance.

Figure E–3. G.823 Specification and Circuit Performance



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