

BB303C

Build in Biasing Circuit MOS FET IC
VHF/UHF RF Amplifier

HITACHI

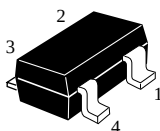
ADE-208-698B (Z)
3rd. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- High forward transfer admittance;
($|y_{fs}| = 42 \text{ mS typ. at } f = 1 \text{ kHz}$)
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 250V at $C=200\text{pF}$, $R_s=0$ conditions.
- Provide mini mold packages; CMPAK-4 (SOT-343 var.)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "CW –".
 2. BB303C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

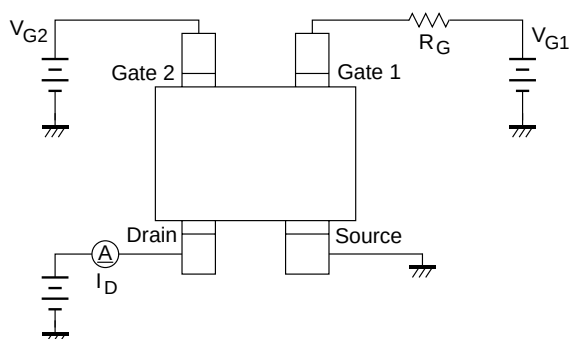
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	7	V
Gate1 to source voltage	V_{G1S}	− 0/ +7	V
Gate2 to source voltage	V_{G2S}	− 0/ +7	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Electrical Characteristics (Ta = 25°C)

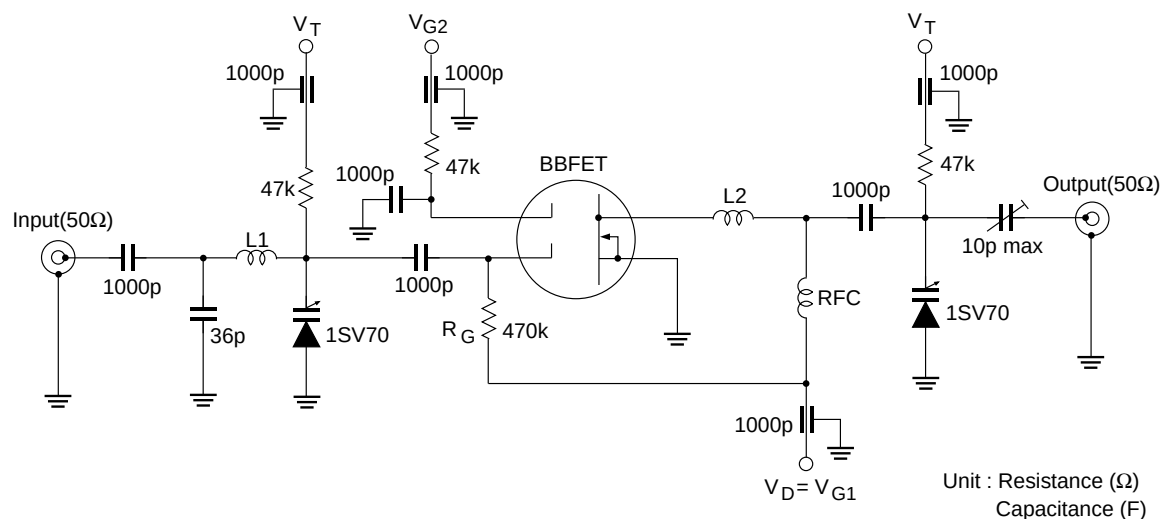
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	7	—	—	V	$I_D = 200\mu A$ $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+7	—	—	V	$I_{G1} = +10\mu A$ $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+7	—	—	V	$I_{G2} = +10\mu A$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.3	0.6	0.9	V	$V_{DS} = 5V$, $V_{G2S} = 4V$ $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.8	1.1	V	$V_{DS} = 5V$, $V_{G1S} = 5V$ $I_D = 100\mu A$
Drain current	$I_{D(op)}$	9	14	20	mA	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$, $R_G = 470k\Omega$
Forward transfer admittance	$ y_{fs} $	35	42	50	mS	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$ $R_G = 470k\Omega$, $f = 1kHz$
Input capacitance	C_{iss}	2.6	3.3	4.0	pF	$V_{DS} = 5V$, $V_{G1} = 5V$
Output capacitance	C_{oss}	1.7	2.1	2.5	pF	$V_{G2S} = 4V$, $R_G = 470k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.025	0.05	pF	$f = 1MHz$
Power gain	PG1	28	32	—	dB	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$, $R_G = 470k\Omega$
Noise figure	NF1	—	1.0	1.6	dB	$f = 200MHz$
Power gain	PG2	12	16.5	—	dB	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$, $R_G = 470k\Omega$
Noise figure	NF2	—	2.85	3.7	dB	$f = 900MHz$

Main Characteristics

Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)

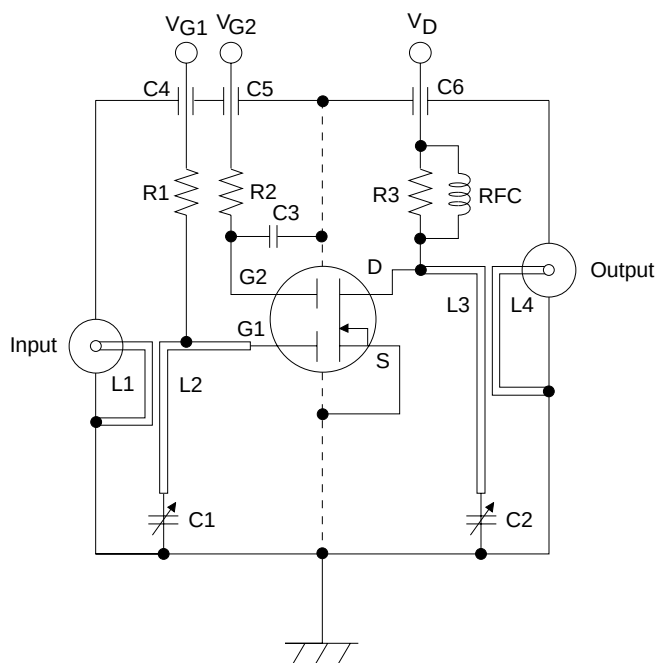


200MHz Power Gain, Noise Figure Test Circuit



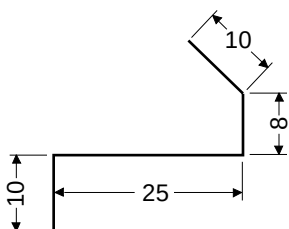
L1 : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 10mm, 2Turns
L2 : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 10mm, 2Turns
RFC : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 5mm, 2Turns

900MHz Power Gain, Noise Figure Test Circuit

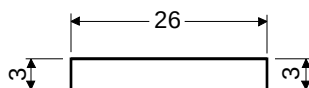


- C1, C2 : Variable Capacitor (10pF MAX)
 C3 : Disk Capacitor (1000pF)
 C4 to C6 : Air Capacitor (1000pF)
 R1 : 470 Ω
 R2 : 47 k Ω
 R3 : 4.7 k Ω

L1 :

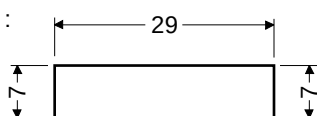


L2 :

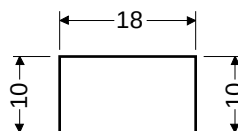


(ϕ 1mm Copper wire)
Unit : mm

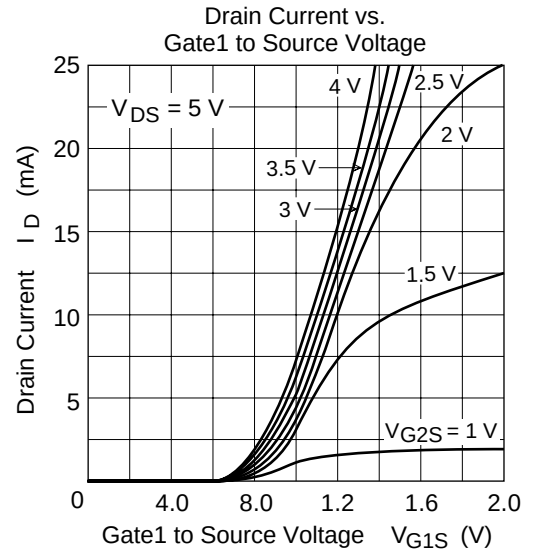
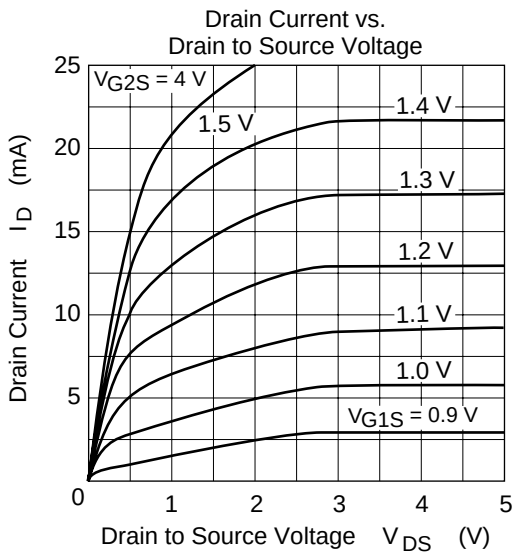
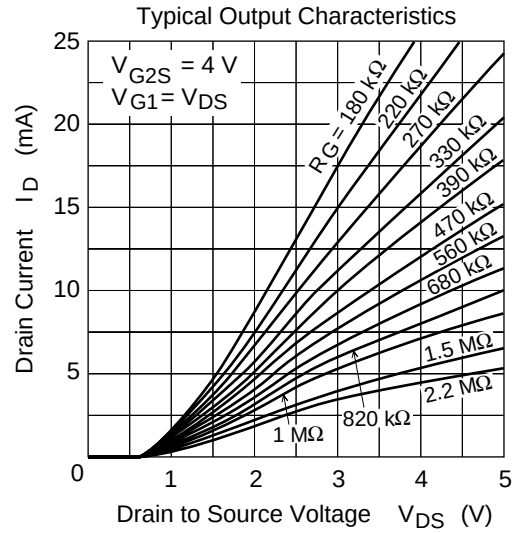
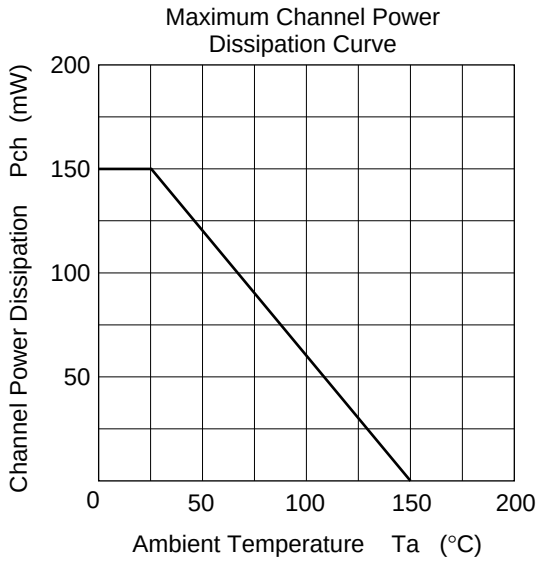
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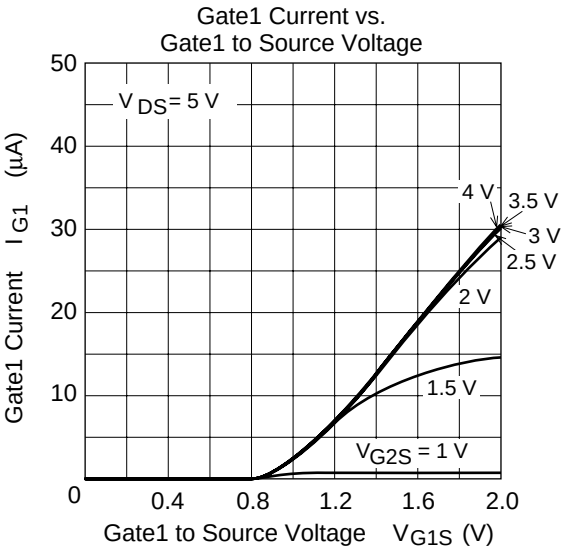
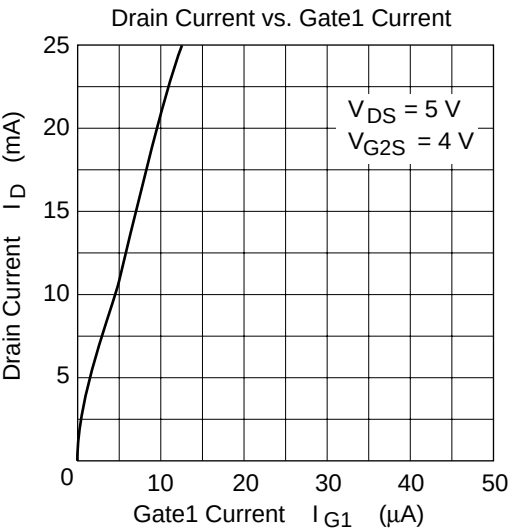
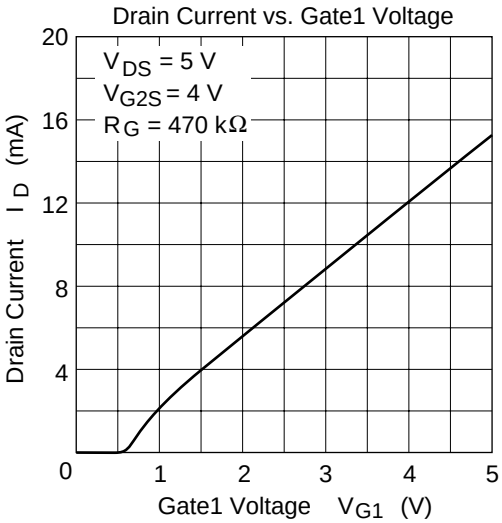
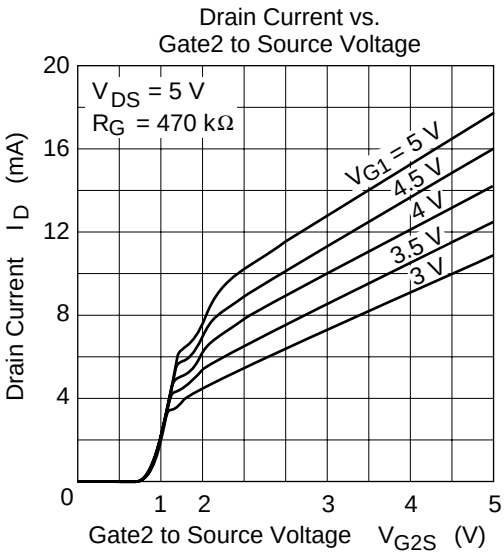


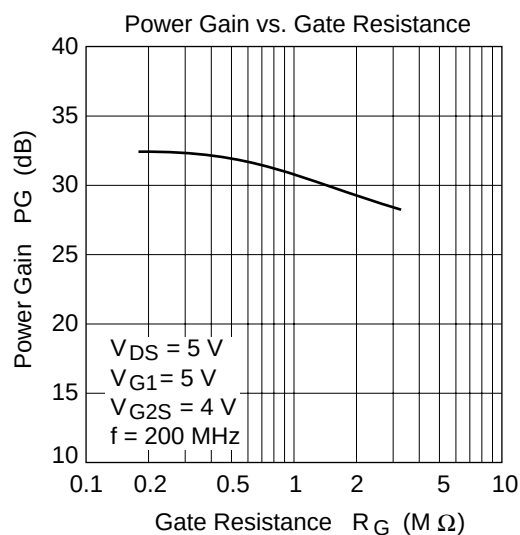
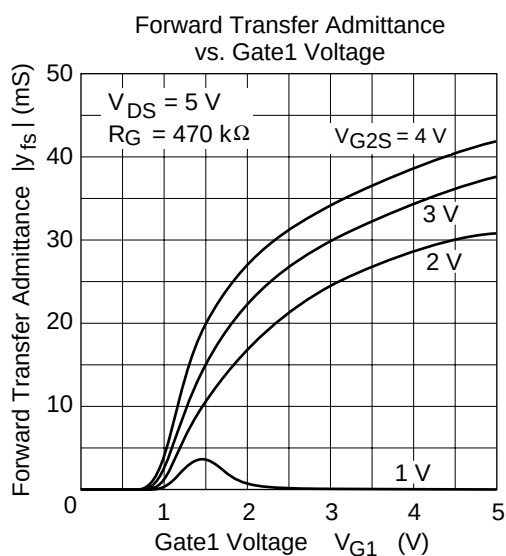
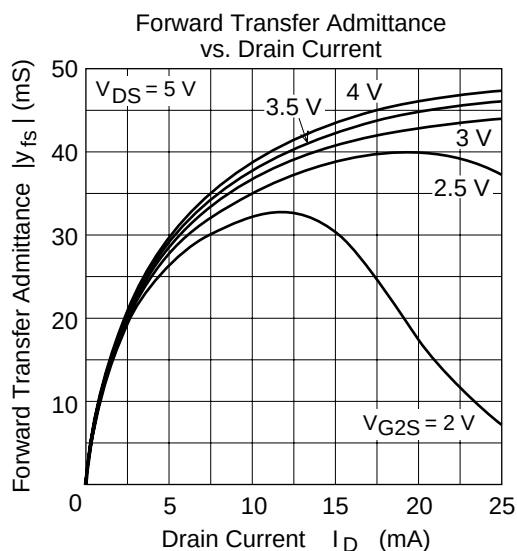
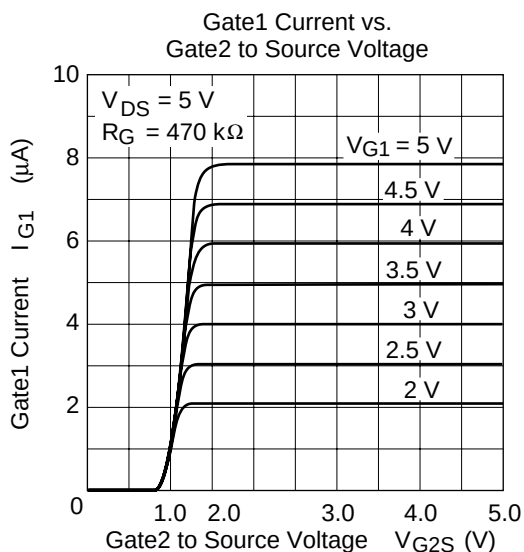
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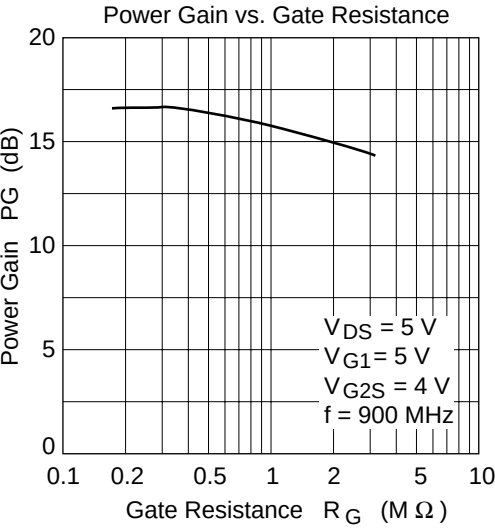
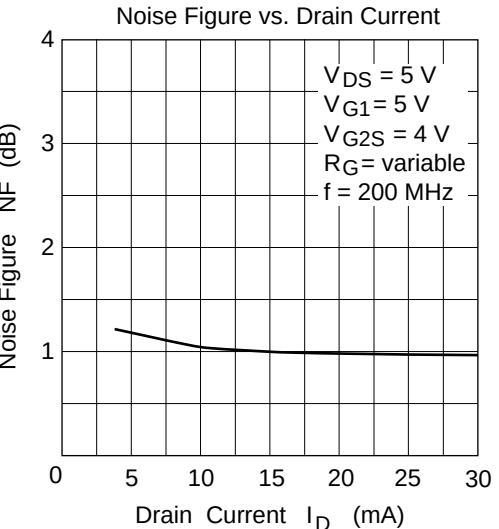
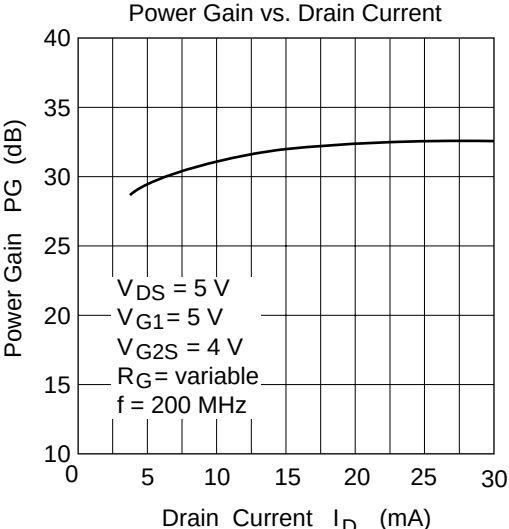
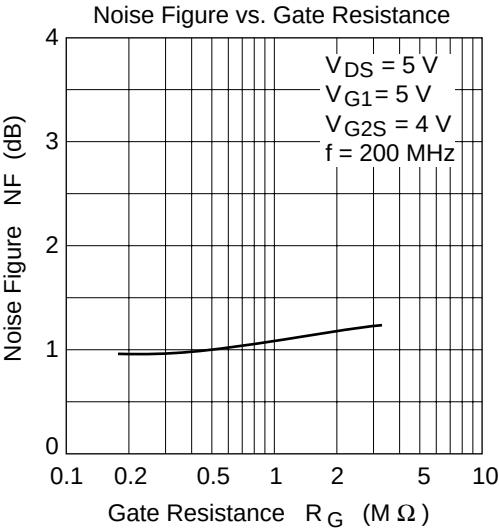


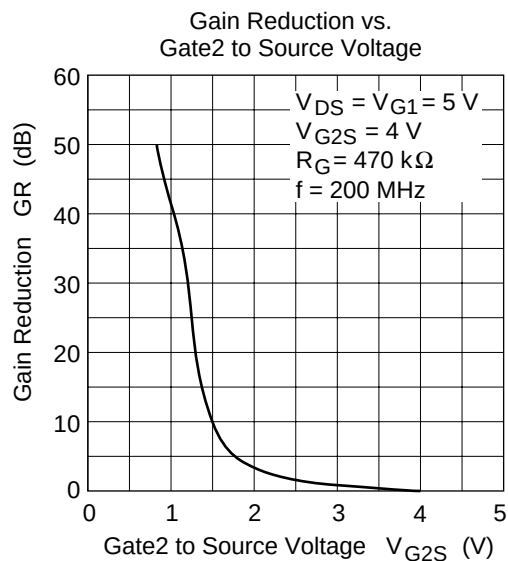
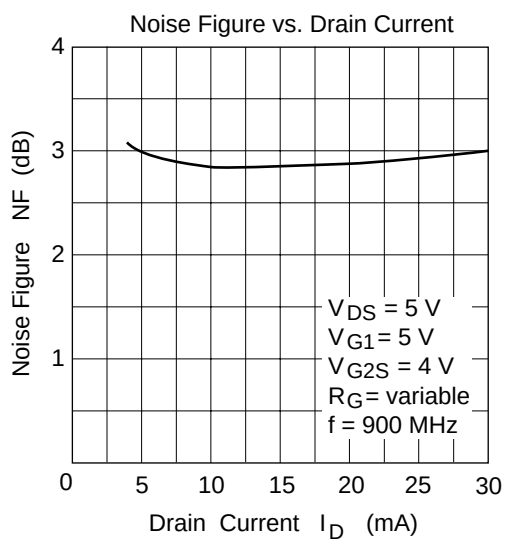
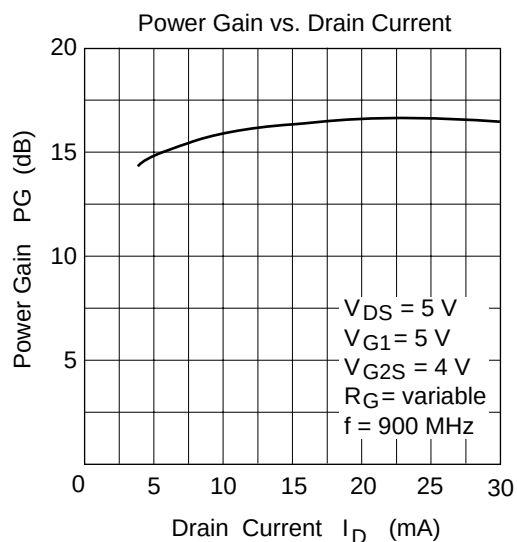
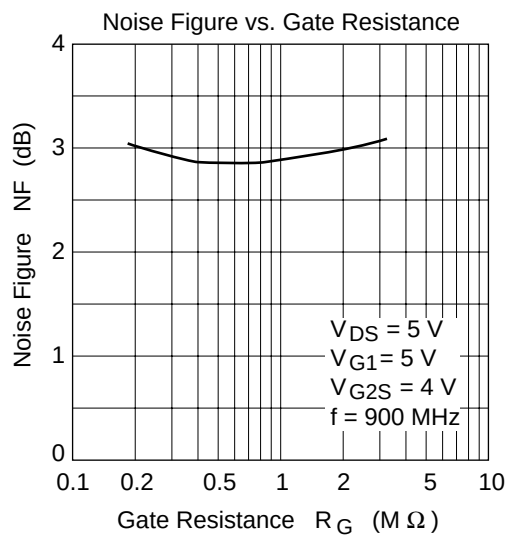
RFC : ϕ 1mm Copper wire with enamel 4turns inside dia 6mm



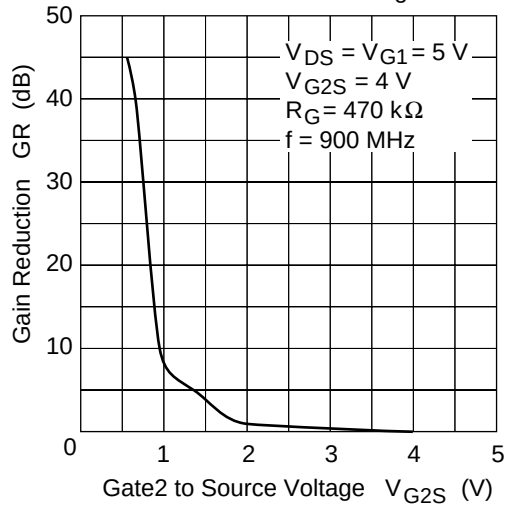




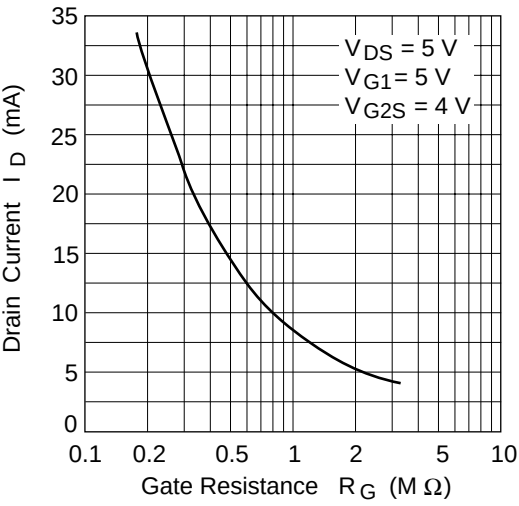




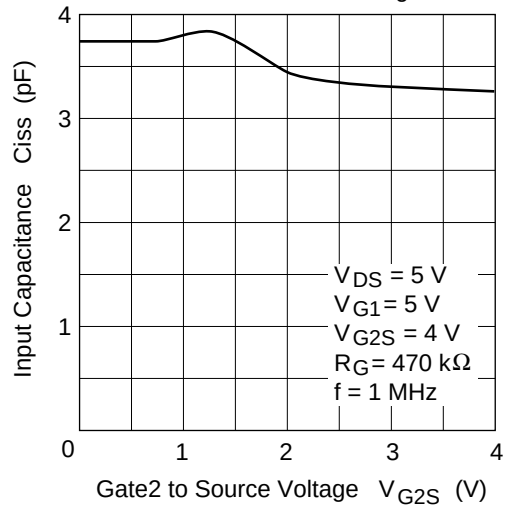
Gain Reduction vs.
Gate2 to Source Voltage



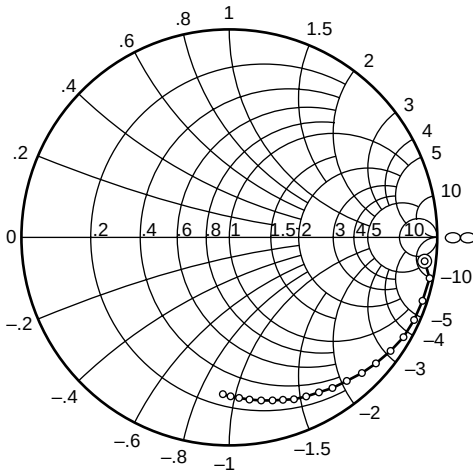
Drain Current vs. Gate Resistance



Input Capacitance vs.
Gate2 to Source Voltage



S11 Parameter vs. Frequency

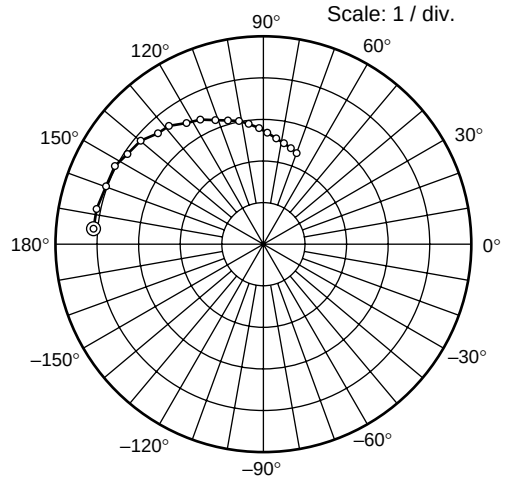


Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 470\text{ k}\Omega$
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S21 Parameter vs. Frequency

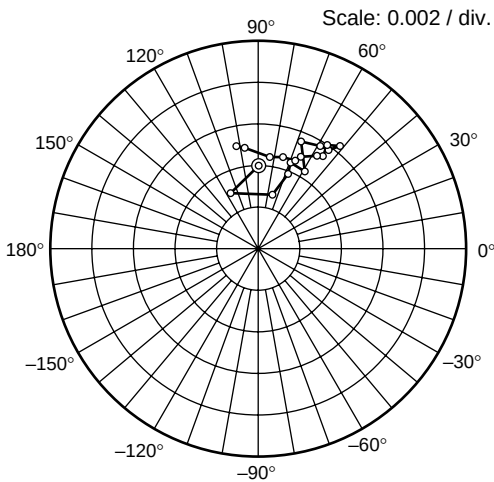


Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 470\text{ k}\Omega$
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S12 Parameter vs. Frequency

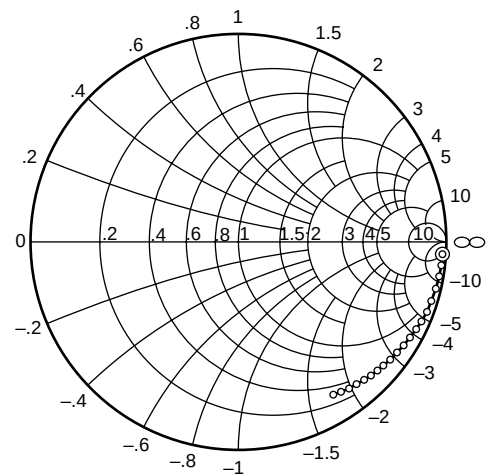


Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 470\text{ k}\Omega$
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S22 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 470\text{ k}\Omega$
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



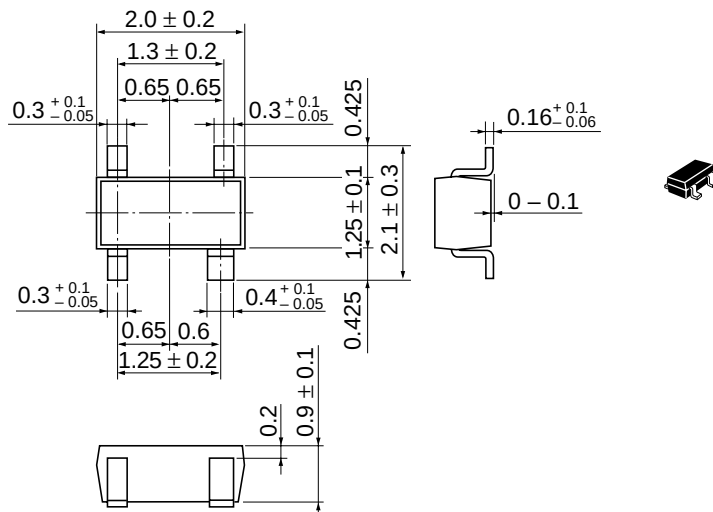
Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 470k\Omega$, $Z_o = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.947	−7.0	4.11	174.4	0.00400	89.0	0.985	−3.1
100	0.978	−11.9	4.13	167.1	0.00305	116.5	0.985	−6.8
150	0.973	−18.7	4.04	159.8	0.00266	75.5	0.982	−10.1
200	0.960	−23.8	4.01	152.7	0.00384	66.8	0.978	−13.5
250	0.956	−29.6	3.90	146.4	0.00453	70.1	0.970	−16.8
300	0.939	−35.5	3.85	139.9	0.00440	59.6	0.965	−20.0
350	0.930	−40.3	3.68	133.6	0.00550	67.2	0.957	−23.1
400	0.905	−45.7	3.63	128.3	0.00571	59.0	0.949	−26.2
450	0.889	−50.3	3.45	122.7	0.00583	54.2	0.940	−29.2
500	0.870	−55.6	3.35	116.6	0.00634	51.6	0.932	−32.1
550	0.855	−59.6	3.22	111.5	0.00596	56.2	0.924	−35.0
600	0.841	−63.9	3.10	106.3	0.00591	55.7	0.917	−37.7
650	0.826	−67.9	3.02	101.4	0.00544	54.9	0.908	−40.5
700	0.812	−71.8	2.89	96.1	0.00533	57.2	0.900	−43.1
750	0.799	−75.6	2.78	91.8	0.00495	64.6	0.893	−45.7
800	0.788	−78.9	2.70	87.5	0.00470	66.5	0.887	−48.1
850	0.778	−82.6	2.60	82.2	0.00460	75.1	0.880	−50.6
900	0.765	−85.8	2.48	78.1	0.00445	83.8	0.874	−52.9
950	0.763	−88.8	2.41	74.2	0.00486	97.0	0.869	−55.3
1000	0.748	−92.2	2.34	69.7	0.00502	102.6	0.864	−57.5

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

Cautions

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
	Asia	:	http://sicapac.hitachi-asia.com
	Japan	:	http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax: <65>-538-6933/538-3877
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
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