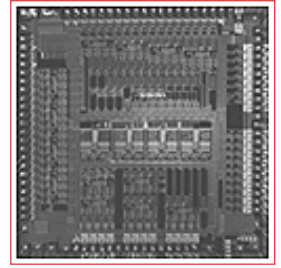




BCM3440 PRODUCT Brief



BCM3440 DIRECT CONVERSION SATELLITE TUNER

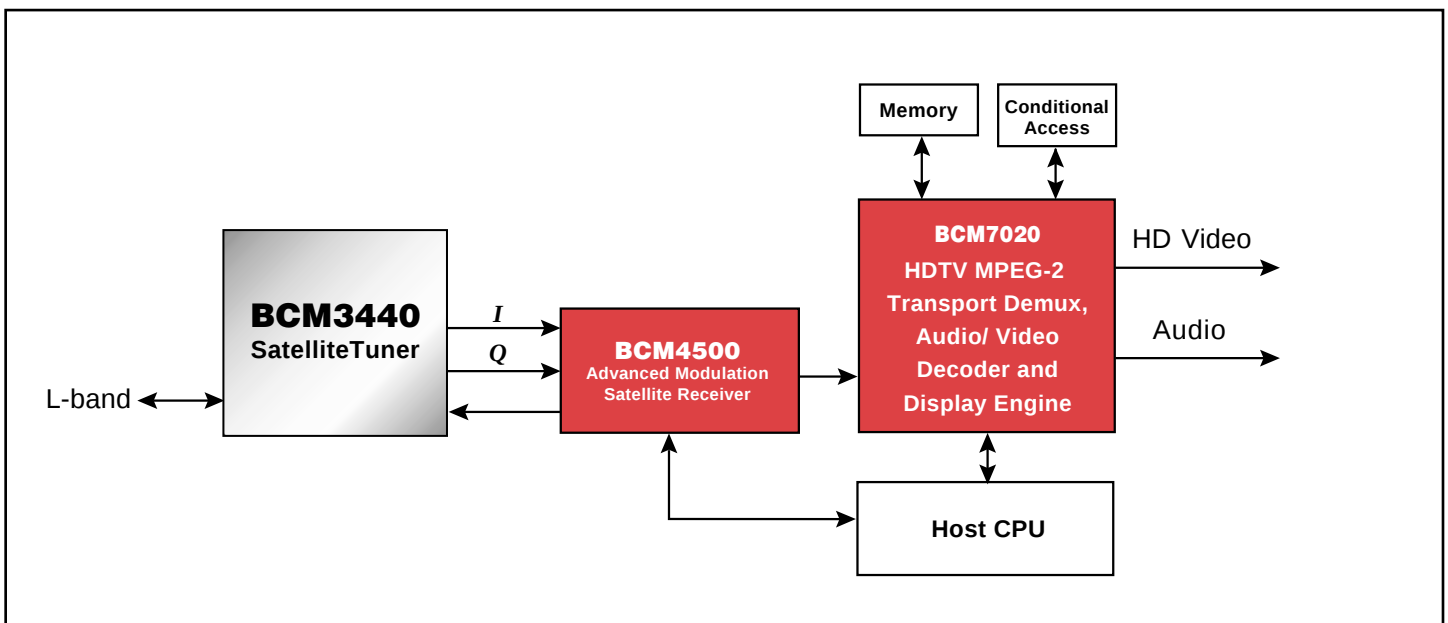
BCM3440 FEATURES

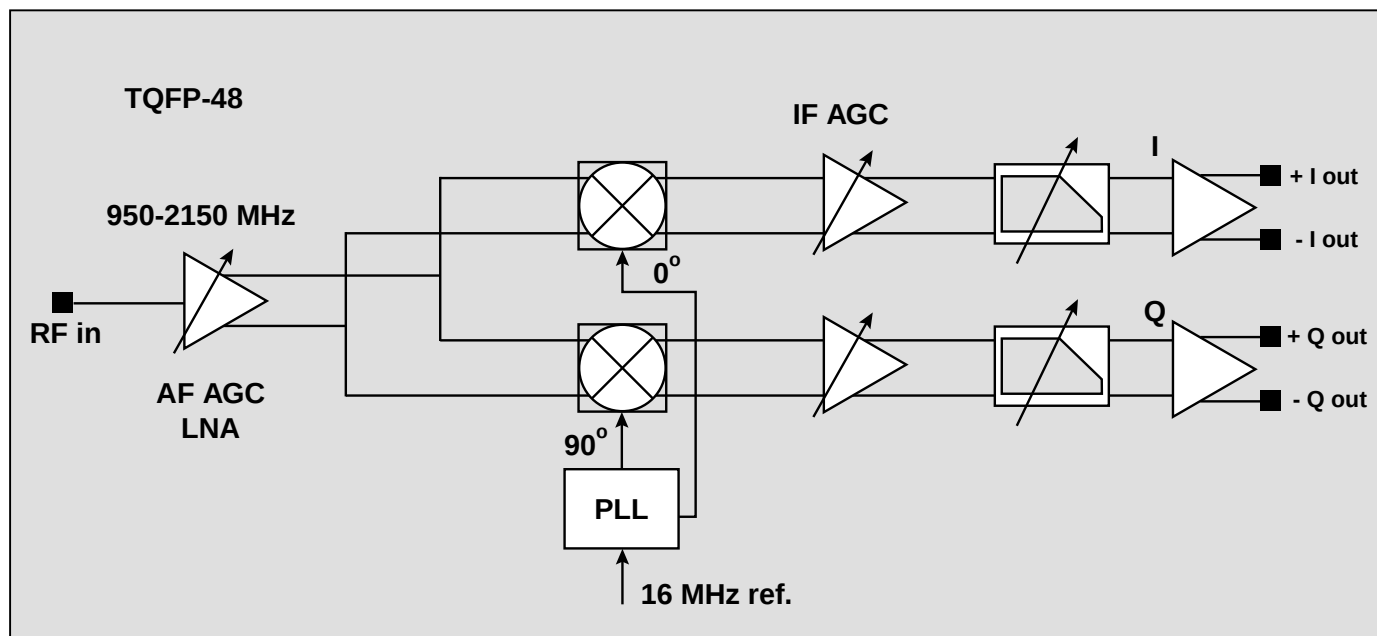
- Direct conversion architecture in standard CMOS process
- Supports QPSK and 8PSK demodulation
- Input frequency range: 950 to 2150 MHz
- Supports 1 to 45 Mbaud data rates
- Input signal: -25 to -70 dBm
- Baseband in-phase and quadrature outputs
- Programmable bandwidth I/Q baseband filters
- Integrated LO with on-chip VCO and PLL
- Integrated LNA with RF AGC
- On-chip IF AGC
- Two wire I²C host interface
- Differential signals for high noise immunity
- Uses a low-cost crystal
- 3.3V operation
- 48-pin TQFP

SUMMARY OF BENEFITS

- Designed to work with the BCM4500 and BCM4201 satellite receivers
- Operates across entire satellite L-band frequency range
- Extremely low phase noise for operation with 8PSK modulation systems
- Highly integrated solution minimizes design time and system cost
- Operates using single 3.3V supply to eliminate the need for 5V
- Complete reference design available to minimize customer RF expertise requirement

BCM3440 Tuner Application Example (Satellite Set-Top Box)





The **BCM3440** is a highly integrated CMOS tuner for the direct broadcast satellite (DBS) market. It is designed to operate with Broadcom's Advanced Modulation Receiver, the BCM4500, which supports 8PSK modulation with turbo code FEC. The **BCM3440** also operates with the BCM4201 QPSK satellite receiver. It is designed to support the full 1–45 Mbaud DVB operating range with support for 950 to 2150 MHz input frequencies.

The **BCM3440** is based on a direct conversion architecture to reduce external component count and increase performance. The chip has integrated LNA, VCO and PLL and has both RF and IF AGCs. The **BCM3440** uses a single 16-MHz crystal that it shares with the BCM4500 for reduced system cost.

The **BCM3440** is a single-chip satellite tuner implemented in low-cost CMOS technology. The tuner takes in a differential L-band signal from standard consumer-grade LNB devices. An on-chip LNA is controlled by an internal AGC to provide wide tuner dynamic range. A direct conversion architecture is used to convert the L-band signal to in-phase and quadrature baseband signals. The signals required for direct

conversion are all generated within the chip by a fully integrated PLL and a quadrature LO generator. These signals are mixed with the L-band input and then filtered by low-pass filters to remove the upper image produced by the mixer. A variable gain amplifier is then used to adjust the baseband signal levels before processing by the channel selection filters to optimize noise performance and prevent distortion within the filters. The channel select filters are digitally programmable 5th order low-pass Butterworth filters. The filters are controlled with **BCM3440** register writes through the I²C interface in 1 MHz steps from 2-MHz to 36-MHz. The device output is a buffered signal capable of driving a 1k ohm differential load 1 V_{pp}. An on-chip DC servo loop is included to correct DC offsets inherent in direct conversion mixers and to minimize the offsets through the channel select filters and output buffers.

The BCM93440 reference design is available to simplify testing and design using the **BCM3440**. Schematics, Gerber files and test and evaluation software are available.

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