Network access

October 26, 1998

product bulletin

Bt8471

Referenced Literature: N8474DSB
Product Affected: Bt8471

Please see the attached pages for brief technical overview of the Bt8471
Multichannel Synchronous Communications Controller (MUSYCC™) device.

PROVIDING

HIGH

SPEED

MULTIMEDIA

CONNECTIONS

CONNECT *with*
Rockwell
Because
Communication
Matters™

N8471BL1

Rockwell *Semiconductor Systems*

Bt8471

Multichannel Synchronous Communications Controller (MUSYCC™)

Product Description

The Bt8471 is the newest member of the family of advanced Multichannel Synchronous Communications Controllers (MUSYCC™) which include the Bt8474/2 (64/128 channel HDLC controller). Bt8471 formats and deformats up to 32 HDLC channels in a single CMOS integrated circuit. MUSYCC operates at Layer 2 of the Open Systems Interconnection (OSI) protocol reference model and provides a comprehensive, high-density solution for processing of HDLC channels for inter-networking applications such as Frame Relay, ISDN D-channel signaling, X.25, Signaling System 7 (SS7), DXI, ISLP and LAN/WAN data transport. Under minimal host supervision, MUSYCC manages a linked list of channel data buffers in host memory by performing Direct Memory Access (DMA) of up to 32 channels (Bt8471), 64 channels (Bt8472), and 128 channels (Bt8474).

Bt8471 interfaces to a serial data stream, such as T1/E1 signals, and then transfers data across the popular 32-bit Peripheral Component Interface (PCI) bus to system memory at a rate of up to 33 MHz. Bt8471's serial interface can be operated up to 8.192 MHz. Logical channels can be mapped as any combination of DS0 timeslots to support ISDN hyperchannels (Nx64 Kb/s) or as any number of bits in a DS0 for subchanneling applications (Nx8 Kb/s). Bt8471 also includes a 32-bit expansion port for bridging the PCI bus to local microprocessors or peripherals. A JTAG port enables boundary-scan testing to replace bed-of-nails board testing.

All specifications for the Bt8471 are identical to the Bt8472 unless otherwise stated in this document.

Functional Block Diagram
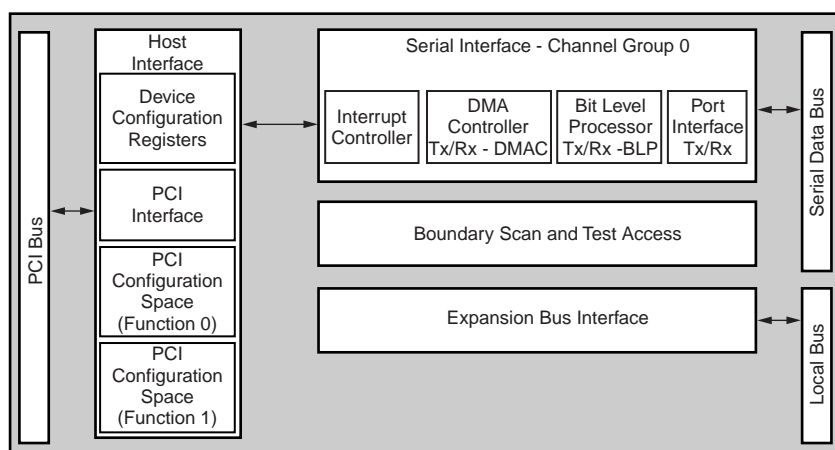
Distinguishing Features

- 32-channel HDLC controller
- OSI Layer 2 protocol support
- General purpose HDLC (ISO 3309)
  - X.25 (LAPB)
  - Frame relay (LAPF/ANSI T1.618)
  - ISDN D-channel (LAPD/Q.921)
  - SS7 support
- 1 serial interface that supports:
  - T1/E1 data streams
  - DC to 8.192 Mb/s TDM bus
- Configurable logical channels
  - Standard DS0 (56, 64 Kbps)
  - Hyperchannel (Nx64)
  - Subchannel (Nx8)
- Per-channel protocol mode selection
  - 16-bit FCS mode
  - 32-bit FCS mode
  - SS7 mode (16-bit FCS)
  - Transparent mode (unformatted data)
- Per-channel DMA buffer management
  - Linked list data structures
  - Variable size transmit/receive FIFO
- Per-channel message length check
  - Select no length checking
  - Select from two 14-bit registers to compare message length
  - Maximum length: 16,384 bytes
- Direct PCI bus interface
  - 32-bit, 33 MHz operation
  - Bus master and slave operation
  - PCI Version 2.1
- Local expansion bus interface (EBUS)
  - 32-bit multiplexed address/data bus
- Low power, 5 volt CMOS operation
- JTAG boundary scan access port
- 160-pin PQFP surface-mount package

Applications

- ISDN basic-rate or primary-rate interfaces
- ISDN D-channel controller
- Routers
- Cellular base station switch controller
- CSU/DSU
- Protocol converter
- Packet data switch
- Frame relay switches/Frame Relay Access Devices (FRAD)
- DXI network interface
- Distributed packet-based communications systems
- Access multiplexer/concentrator

Ordering Information

Model Number	Version	Package	Temperature Range
28471-16	32-Channel	160-Pin Plastic Quad Flat Pack (PQFP)	0 °C to +70 °C
28471-17	32-Channel	160-Pin Plastic Quad Flat Pack (PQFP)	–40 °C to +85 °C

Product Definition

The Bt8471 is identical to the Bt8472, except the Bt8471 has these features:

- 32-channel HDLC controller
- 1 serial interface
- Pins 12, 13, 15, 16 and 99-101 labeled NC

Figure 1 displays the pinout diagram of the Bt8471. Figure 2 displays the logic diagram. Table 1 details Register 0, Address 00h, with the Device ID and Vendor ID bits.

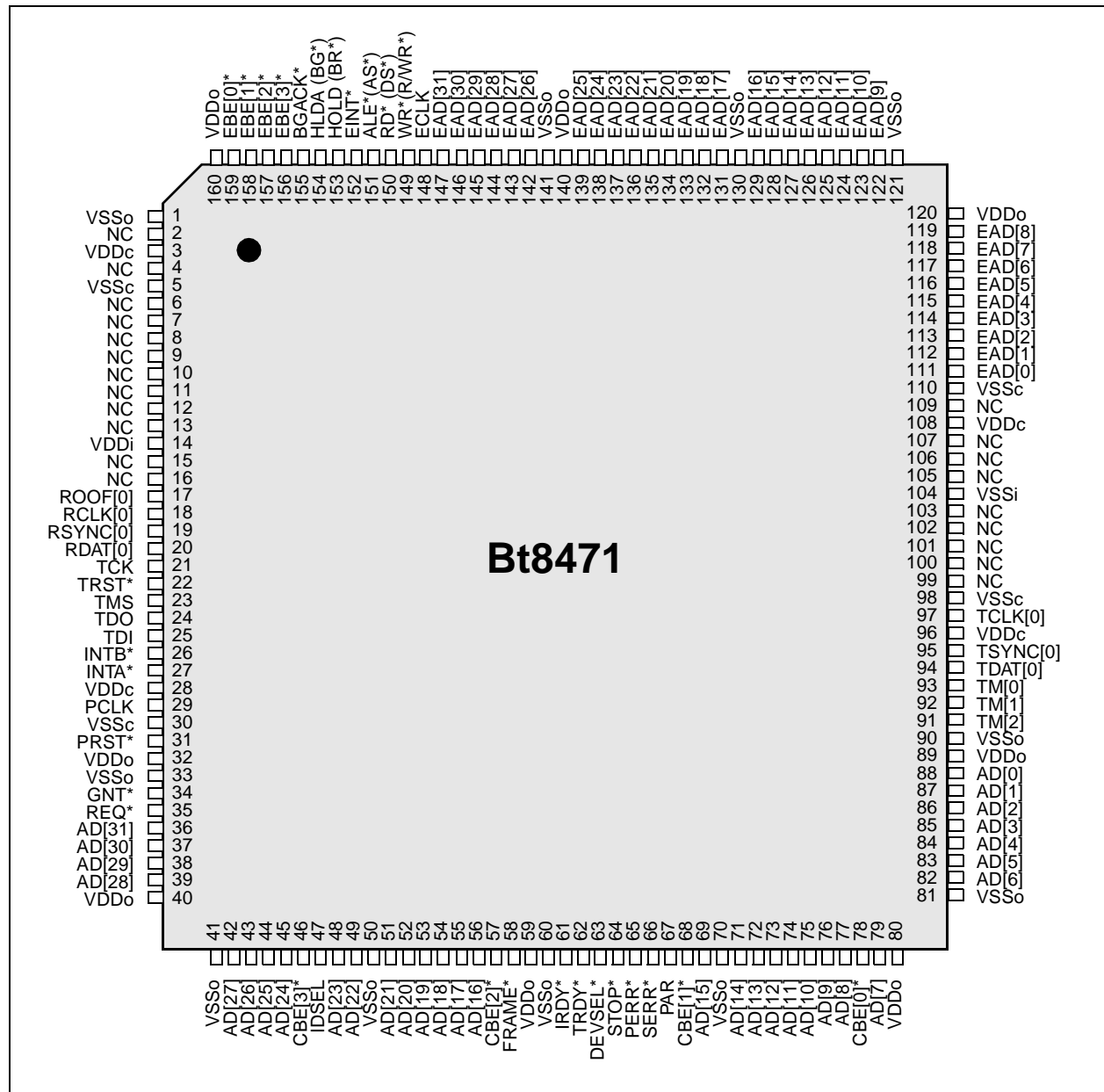Figure 1. Bt8471 Pinout Configuration
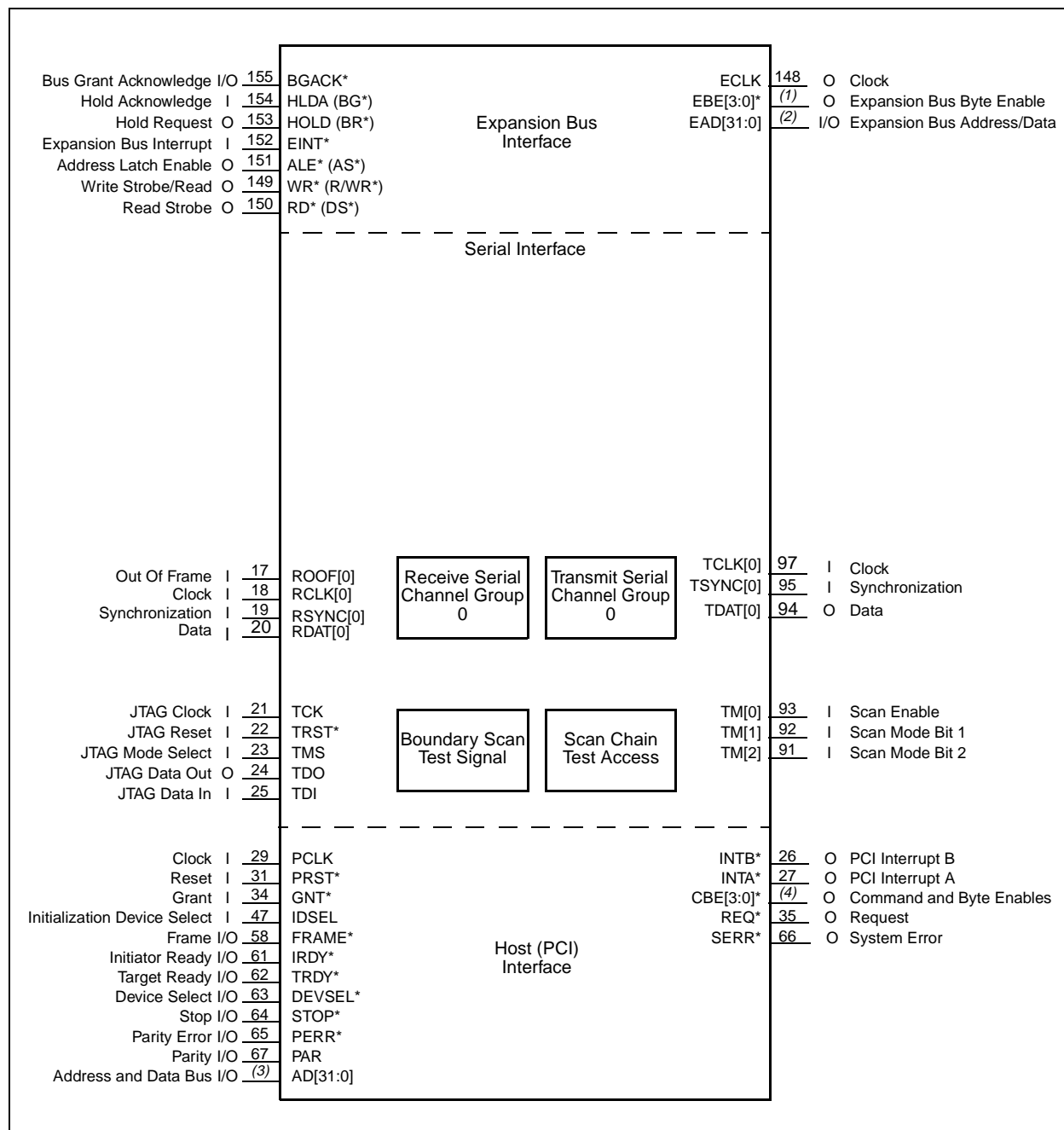
Figure 2. Bt8471 Logic Diagram

Bus Grant Acknowledge I/O 155 BGACK*
Hold Acknowledge I 154 HLDA (BG*)
Hold Request O 153 HOLD (BR*)
Expansion Bus Interrupt I 152 EINT*
Address Latch Enable O 151 ALE* (AS*)
Write Strobe/Read O 149 WR* (R/WR*)
Read Strobe O 150 RD* (DS*)

ECLK 148 O Clock
EBE[3:0]* (1) O Expansion Bus Byte Enable
EAD[31:0] (2) I/O Expansion Bus Address/Data

Expansion Bus Interface

Serial Interface

Out Of Frame I 17 ROOF[0]
Clock I 18 RCLK[0]
Synchronization I 19 RSYNC[0]
Data I 20 RDAT[0]

Receive Serial Channel Group 0

Transmit Serial Channel Group 0

TCLK[0] 97 I Clock
TSYNC[0] 95 I Synchronization
TDAT[0] 94 O Data

JTAG Clock I 21 TCK
JTAG Reset I 22 TRST*
JTAG Mode Select I 23 TMS
JTAG Data Out O 24 TDO
JTAG Data In I 25 TDI

Boundary Scan Test Signal

Scan Chain Test Access

TM[0] 93 I Scan Enable
TM[1] 92 I Scan Mode Bit 1
TM[2] 91 I Scan Mode Bit 2

Clock I 29 PCLK
Reset I 31 PRST*
Grant I 34 GNT*
Initialization Device Select I 47 IDSEL
Frame I/O 58 FRAME*
Initiator Ready I/O 61 IRDY*
Target Ready I/O 62 TRDY*
Device Select I/O 63 DEVSEL*
Stop I/O 64 STOP*
Parity Error I/O 65 PERR*
Parity I/O 67 PAR
Address and Data Bus I/O (3) AD[31:0]

Host (PCI) Interface

INTB* 26 O PCI Interrupt B
INTA* 27 O PCI Interrupt A
CBE[3:0]* (4) O Command and Byte Enables
REQ* 35 O Request
SERR* 66 O System Error

Table 1. Register 0, Address 00h

Bit Field	Name	Reset Value	Type	Description
31:16	Device ID[1]	8472h	RO	This unique device identification is assigned by the manufacturer. This field always returns the value 8472h for the Bt8471.
15:0	Vendor ID[1]	109Eh	RO	The unique vendor identification assigned to the manufacturer. This field always returns the value 109Eh.
(1) Registers shared between Function 0 and 1.				