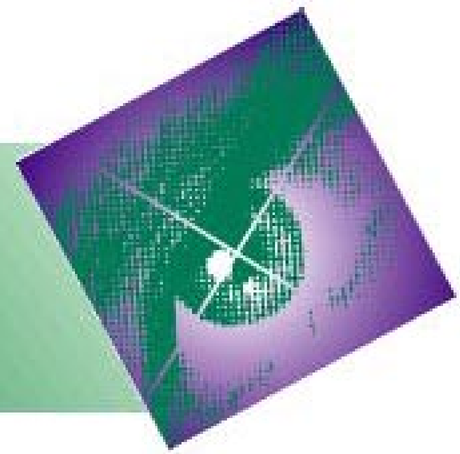
Advance Information

This document contains information on a product under development.
The parametric information contains target parameters that are subject to change.



Bt864/865

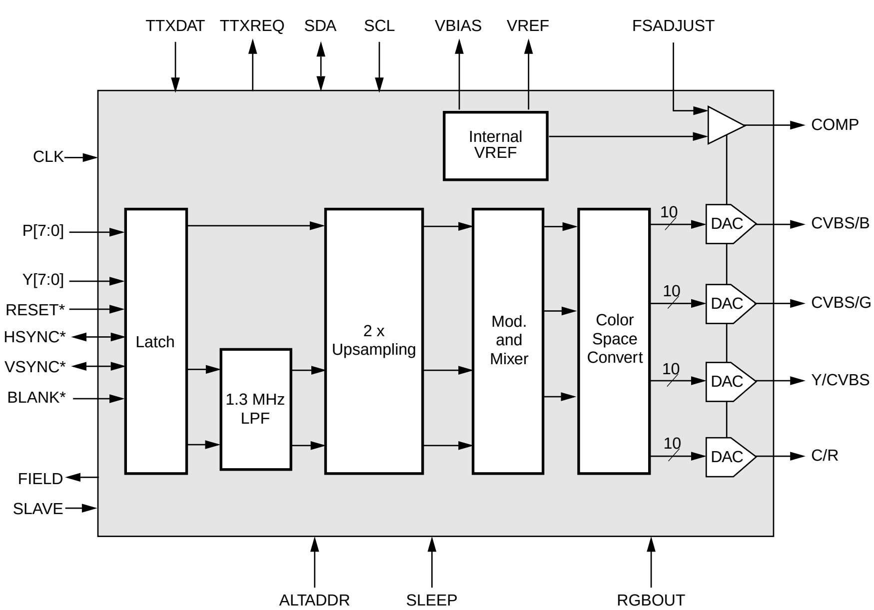
YCrCb to NTSC/PAL Digital/Video Encoder

The Bt864/865 is specifically designed for video systems requiring the generation of composite, Y/C (S-video) or RGB (SCART) video signals from an 8- or 16-bit YCrCb digital video stream. Worldwide video standards are supported including NTSC-M (N. America, Taiwan, Japan), PAL-B,D,G,H,I (Europe, Asia), PAL–M (Brazil), PAL-N (Uruguay, Paraguay) and PAL–Nc (Argentina). The Bt864 and Bt865 are functionally identical, with the exception that Bt865 can output the Macrovision level 6.1 anticopy algorithm.

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) may be configured as inputs (slave mode) or outputs (master mode). BLANK* is an input and may be externally controlled. Horizontal and vertical blanking are automatically generated. The rise and fall times of sync, the burst envelope, and closed caption data are internally controlled.

Analog luminance (Y) and chrominance (C) information is available on the Y and C outputs for interfacing to S-video equipment. The composite analog video signal is output simultaneously onto two outputs. This allows one output to provide baseband composite video while the other drives an RF modulator. Analog RGB is also available to allow for support of the European SCART/PeriTV interface.

Functional Block Diagram



Distinguishing Features

- 8- or 16-bit 4:2:2 YCrCb inputs
- NTSC-M/PAL/PAL–M/PAL–Nc composite video outputs
- S-Video/RGB (SCART) outputs
- CCIR 601 or square pixel operation
- 2x oversampling
- 10-bit DACs
- Master or slave video timing
- Interlaced/noninterlaced operation
- Macrovision support (Bt865 only)
- Closed caption encoding
- Teletext encoding (WST system B)
- I^2C Interface
- On-board voltage reference
- Power-down mode
- 52-pin PQFP package
- Programmable luma delay (CVBS/B)
- 5 V or 3.3 V supply voltage

Related Products

- Bt856/7
- Bt856A
- Bt866/7
- Bt852
- Bt864A/5A

Applications

- Digital cable systems
- Direct broadcast satellite (DBS)
- DVD players
- Digital VCR (DVC, DVHS)
- VideoCD players
- Portable VideoCD players

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Ordering Information

Model Number	Package	Ambient Temperature Range
Bt864KPF	52-Pin Plastic Quad Flatpack	0˚ to +70˚C
Bt865KPF	52-Pin Plastic Quad Flatpack	0˚ to +70˚C

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CIRCUIT DESCRIPTION

Pin Descriptions

Pin names, input/output assignments, numbers, and descriptions are listed in Table 1. Figure 1 illustrates the Bt864/865 pinout diagram, and Figure 2 details the block diagram.

Table 1. Pin Assignments *(1 of 3)*

Pin Name	I/O	Pin #	Description
CLK	I	43	2x pixel clock input (TTL compatible).
RESET*	I	47	Reset control input (TTL compatible). A logical zero resets and disables video timing (horizontal, vertical, subcarrier counters to the start of VSYNC of first field) and resets the I^2C interface (but does not reset I^2C registers). RESET* must be a logical one for normal operation.
BLANK*	I	48	Composite blanking control input (TTL compatible). BLANK* is registered on the rising edge of CLK. The P[7:0] and Y[7:0] inputs are ignored while BLANK* is a logical zero.
VSYNC*	I/O	49	Vertical sync input/output (TTL compatible). As an output (master mode operation), VSYNC* is output following the rising edge of CLK. As an input (slave mode operation), VSYNC* is registered on the rising edge of CLK.
HSYNC*	I/O	50	Horizontal sync input/output (TTL compatible). As an output (master mode operation), HSYNC* is output following the rising edge of CLK. As an input (slave mode operation), HSYNC* is registered on the rising edge of CLK.
P[7:0]	I	35–28	YCrCb pixel inputs (TTL compatible) in 8-bit YCrCb mode. CrCb pixel inputs (TTL compatible) in 16-bit YCrCb mode. A higher index corresponds to a greater significance.
Y[7:0]	I	25, 24, 21–16	Y pixel inputs (TTL compatible) in 16-bit YCrCb mode. Y[7] enables internal color bars when operating in 8-bit YCrCb mode. A higher index corresponds to a greater significance.[1]
TTXDAT	I	27	Teletext bit stream input (TTL compatible).[1]
TTXREQ	O	38	Teletext request output (TTL compatible).

Table 1. Pin Assignments *(2 of 3)*

Pin Name	I/O	Pin #	Description
ALTADDR	I	26	Alternate slave address input (TTL compatible). A logical one configures the device to respond to an I^2C address of 0x88; a logical zero configures the device to respond to an I^2C address of 0x8A.(1)
SLAVE	I	42	Slave/master mode select input (TTL compatible). A logical one configures the device for slave video timing operation. A logical zero configures the device for master video timing operation. This pin may be connected directly to VDD or GND.
RGBOUT	I	14	Analog RGB control input (TTL compatible). A logical one configures the device to output analog RGB (RGBOUT mode). A logical zero configures the device to generate S-video along with a second composite video output. This pin may be connected directly to VDD or GND.
FIELD	O	15	Field control output (TTL compatible). FIELD transitions after the rising edge of CLK, two clock cycles following falling HSYNC*. It is a logical zero during FIELD 1 and is a logical one during FIELD 2.
SLEEP	I	39	Power-down control input (TTL compatible). A logical one configures the device for power-down mode. A logical zero configures the device for normal operation. This pin may be connected directly to VDD or GND.
SDA	I/O	40	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this serial bus.
SCL	I	41	Serial interface clock input (TTL compatible). The maximum clock rate is 100 KHz.
VDD3V	I	44	Input threshold adjustment. When low, indicates supply voltage of nominally 5 volts. When high, indicates supply voltage of nominally 3.3 volts.
CVBS/B	O	8	Composite video or Blue (with blanking and sync, and optionally, Macrovision pulse).
CVBS/B AGND		6	Analog ground for pin CVBS/B.
CVBS/G	O	10	Composite video or Green (with blanking and sync, and optionally, Macrovision pulse).
CVBS/G AGND		7	Analog ground for pin CVBS/G.
C/R	O	12	Modulated chrominance, or Red.
C/R AGND		9	Analog ground for pin C/R.
Y/CVBS	O	13	Luminance or composite video (with blanking, sync, and optionally, Macrovision pulses, and/or closed-captioning encoding).
Y/CVBS AGND		11	Analog ground for pin Y/CVBS.
FSADJUST	I	1	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the analog outputs. For standard operation, use the nominal RSET values shown under Recommended Operating Conditions.
VBIAS	O	2	DAC bias voltage. A 0.1 µF ceramic capacitor must be used to bypass this pin to GND. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Table 1. Pin Assignments *(3 of 3)*

Pin Name	I/O	Pin #	Description
VREF	O	3	Voltage reference pin. A 0.1 μF ceramic capacitor must be used to decouple this pin to GND, as shown in Figure 21 in the PC Board Layout section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
COMP	O	5	Compensation pin. A 0.1 μF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	–	4	Analog power. All VAA and VDD pins must be connected together on the same PCB plane to prevent latchup. Current <200 mA.
VDD	–	37, 23, 46	Digital power. All VAA and VDD pins must be connected together on the same PCB plane to prevent latchup.
AGND	–	51, 52	Analog ground. All AGND and GND pins must be connected together on the same PCB plane to prevent latchup.
GND	–	22, 36, 45	Digital ground. All AGND and GND pins must be connected together on the same PCB plane to prevent latchup.
Notes: (1). Any unused inputs should not be left floating.			

Figure 1. Bt864/865 Pinout Diagram

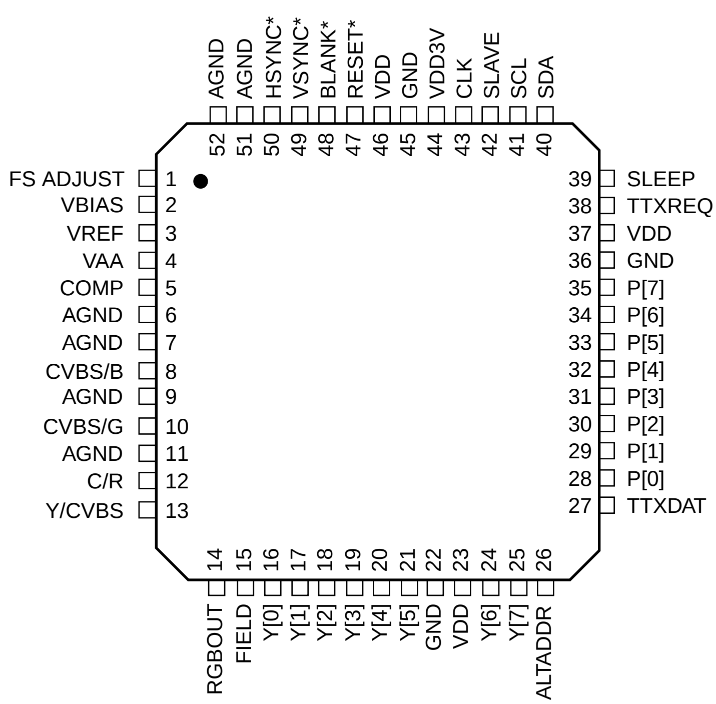
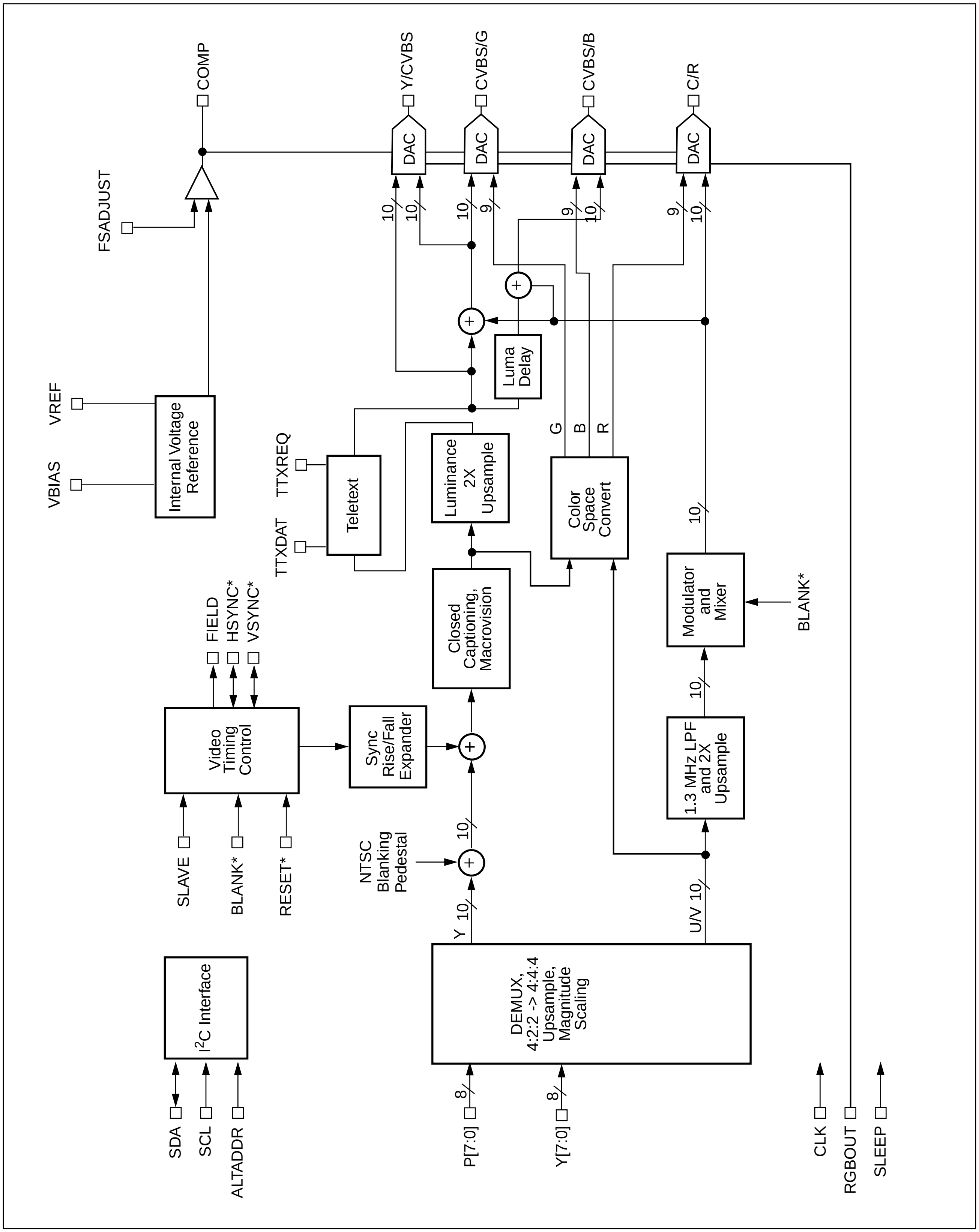


Figure 2. Detailed Block Diagram



Clock Timing

A clock signal with a frequency twice the pixel sampling rate must be present at the CLK pin. The device generates an internal pixel CLOCK that in slave mode is synchronized to the HSYNC* pin. This signal is used to increment the horizontal pixel and vertical line counters and to register the pixel (P[7:0], RESET*, BLANK*, SLAVE*, and VSYNC*) inputs. All setup and hold timing specifications are measured with respect to the rising edge of CLK.

Pixel Input Timing

8-bit YCrCb Input Mode

The 8-bit YCrCb multiplexed input mode is selected by default. Multiplexed Y, Cb, and Cr data is input through the P[7:0] inputs. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc. in accordance with CCIR656.

16-bit YCrCb Input Mode

The 16-bit mode is selected by setting the YC16 register bit. Y data is input through the Y[7:0] inputs. Multiplexed Cb and Cr data is input through the P[7:0] inputs.

Pixel Synchronization

The default input pixel sequence is such that the next clock after HSYNC* goes low will be the start of the 4-byte CB/Y/CR/Y sequence in 8-bit mode, or Y/CB sample pair in 16-bit mode. This is true for slave mode, and for master mode with the default HSYNC* timing. This sequence can be changed by the SYNCDLY and CBSWAP bits in both master and slave modes, or by using the variable HSYNC* timing in master mode.

The SYNCDLY bit will decrease the delay between the HSYNC* pin and the analog output by one clock cycle. The pixel-to-analog out timing is unaffected. This makes the next pixel after the falling edge of HSYNC* the last Y of the CB/Y/CR/Y sequence in 8-bit mode.

The CBSWAP bit will shift the sequence at the input such that the next sample after the falling edge of HSYNC* will be the CR sample of the CB/Y/CR/Y sequence in 8-bit mode, or the Y/CR sample pair in 16-bit mode. The relationship between the HSYNC* pin and the analog output is unaffected, as is the pixel-to-analog out timing.

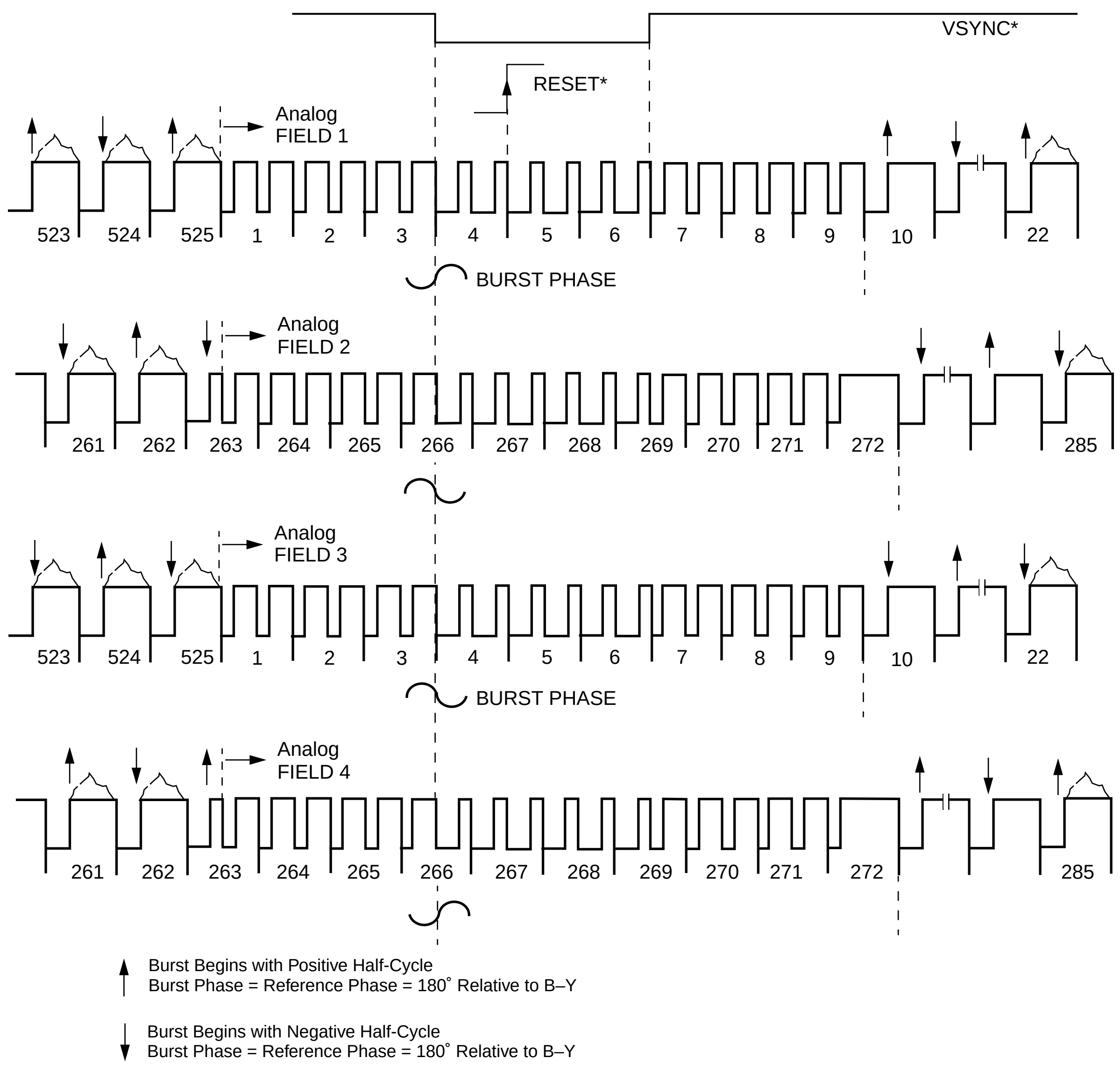
In slave mode, the pipeline delay from HSYNC* to analog sync out is 48 clocks if SYNCDLY = 0, and 47 clocks if SYNCDLY = 1. In master mode, the pipeline delay from HSYNC* to analog sync out for the default HSYNC* timing is 42 clocks if SYNCDLY = 0, 41 clocks if SYNCDLY = 1. If the variable HSYNC* timing is selected, the pipeline delay from HSYNC* to analog sync out is 41–2 * HSYNCF if SYNCDLY = 0, 42–2 * HSYNCF clocks if SYNCDLY = 1. The pipeline delay from pixel input to analog sync output is 52 clocks.

In slave mode, the pipeline delay from HSYNC* input to horizontal pixel counter reset is 6 clocks. In master mode, the pipeline delay from horizontal pixel counter reset to HSYNC* is 2 clocks.

Video Timing

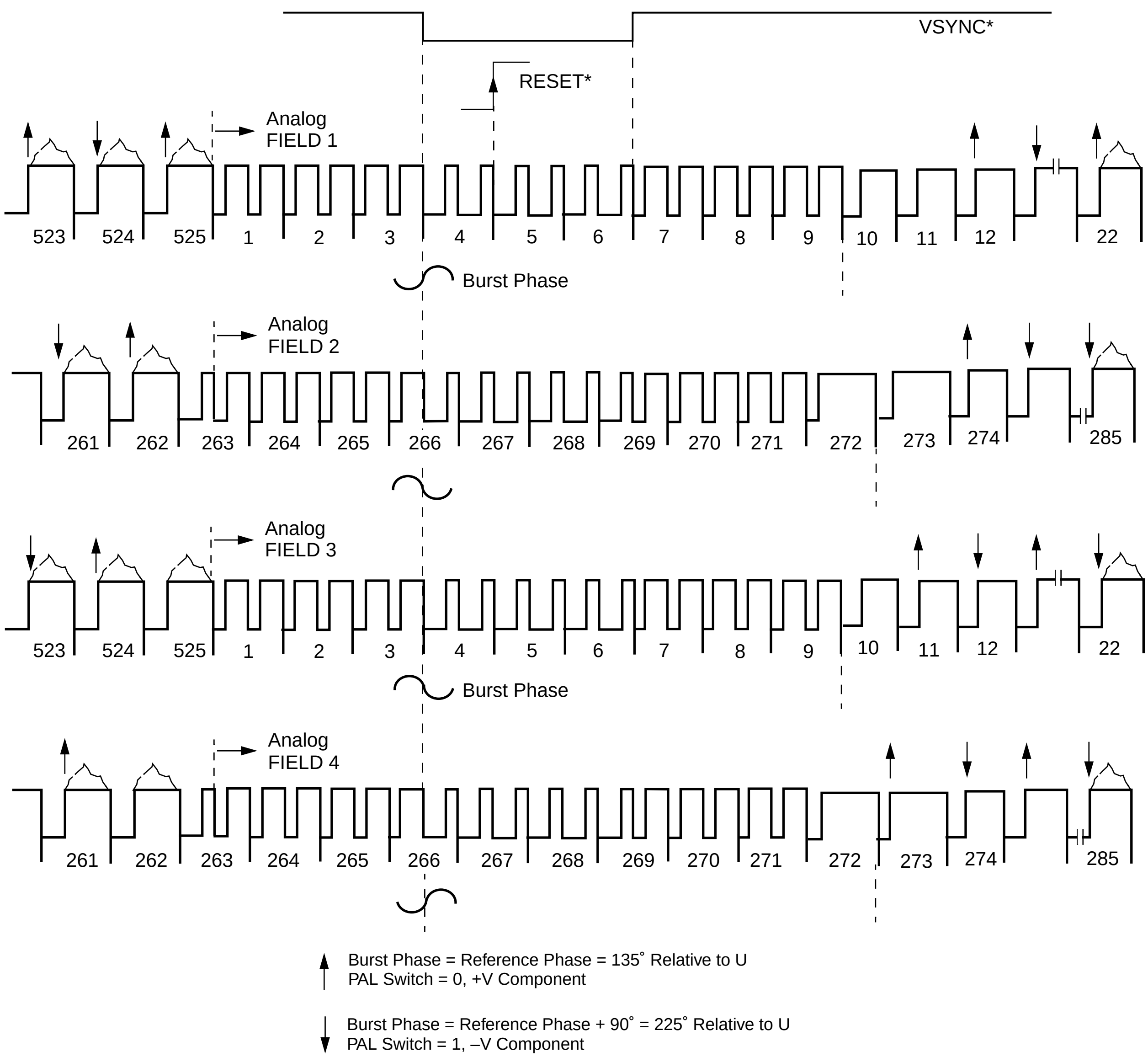
The width of the analog horizontal sync pulses and the start and end of color burst are automatically calculated and inserted for each mode according to ITU-RBT.470-3. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, closed-caption data transitions, and the burst envelope are internally controlled. Figures 3–8 show the timing characteristics for various Bt864/865 modes of operation.

Figure 3. Interlaced 525-Line (NTSC) Video Timing



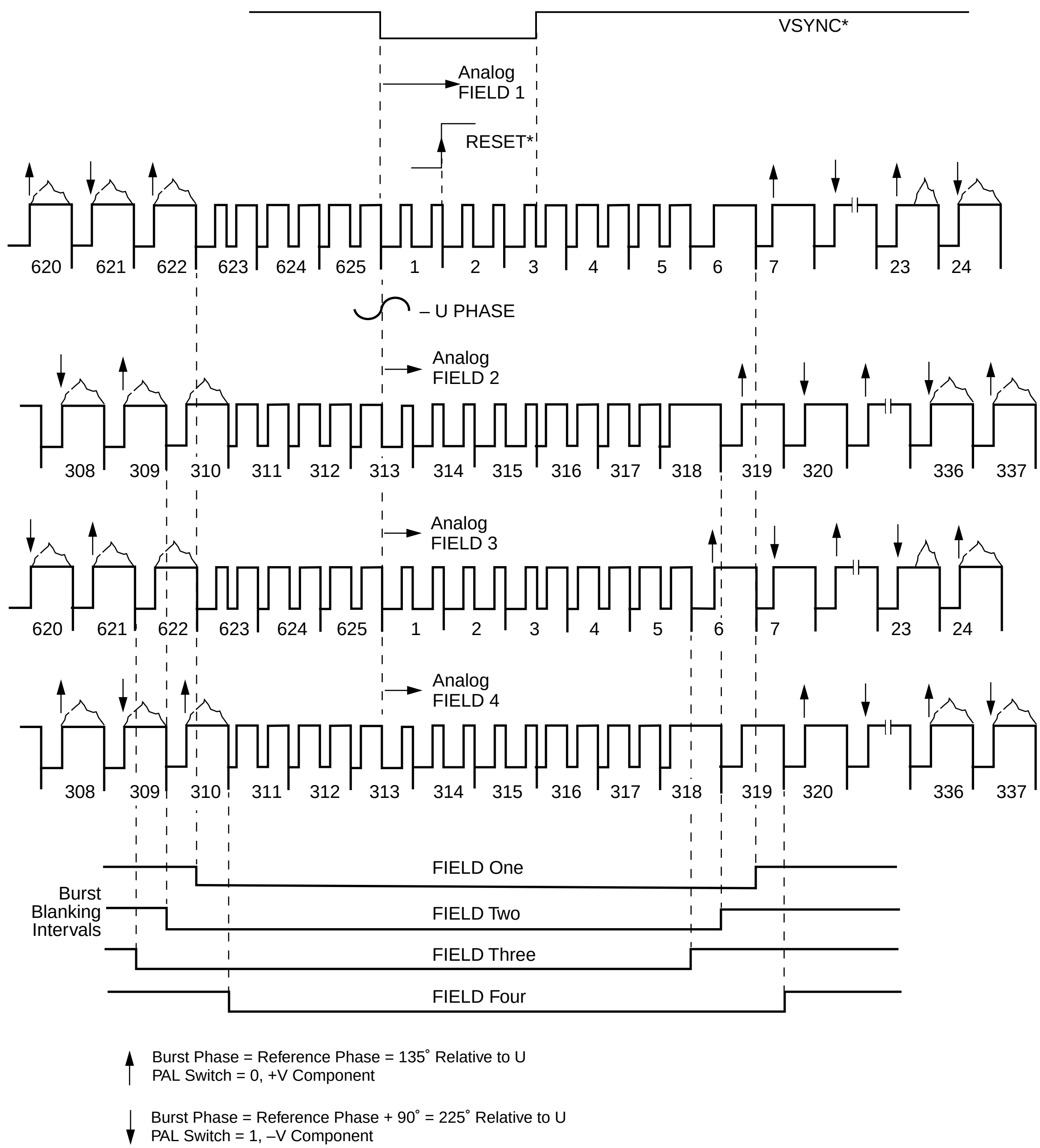
Note: SMPTE line numbering convention rather than ITU-R BT.470-3 is used. EVBI = 0

Figure 4. Interlaced 525-Line (PAL-M) Video Timing



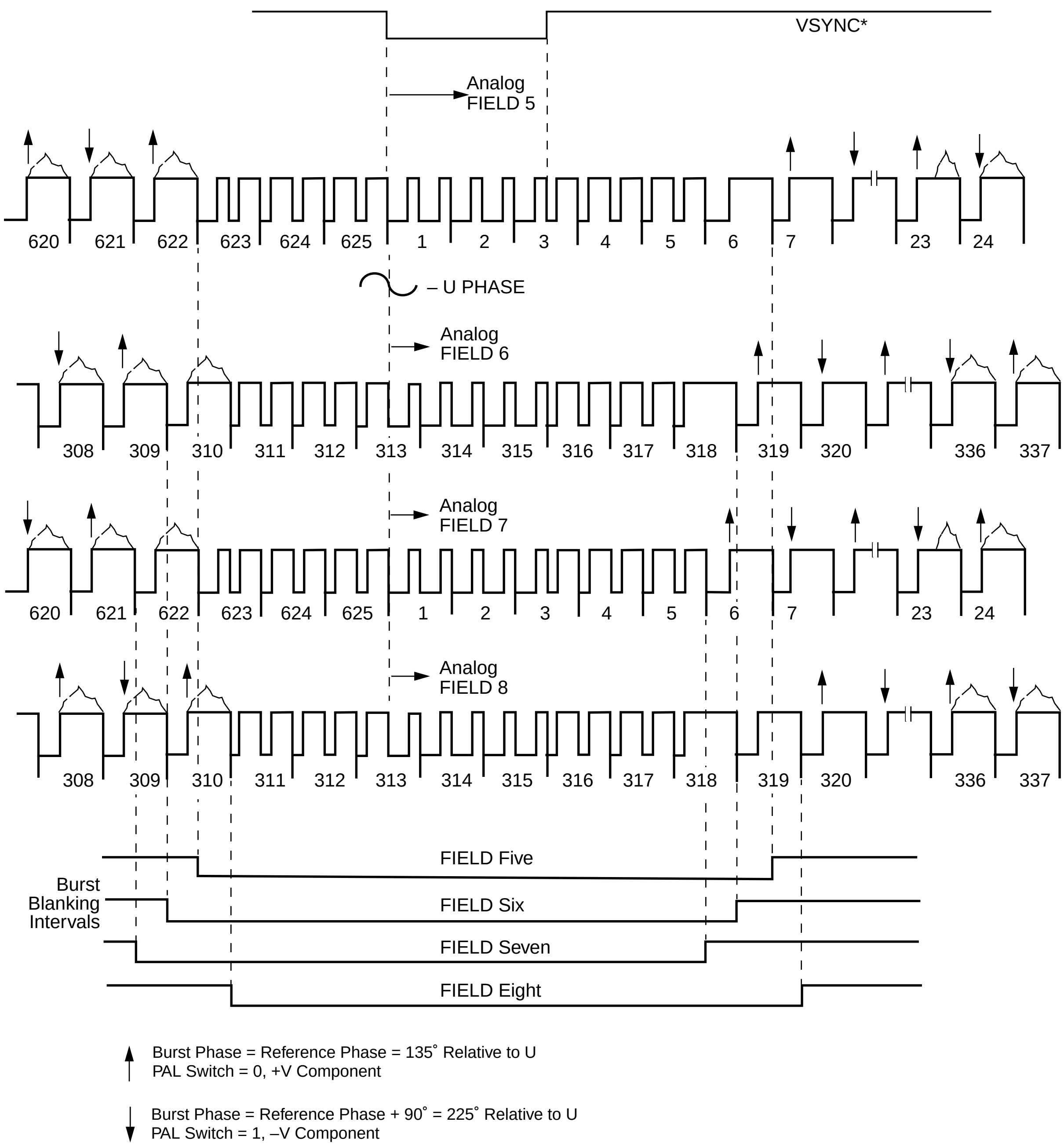
Note: SMPTE line numbering convention rather than ITU-R BT.470-3 is used. EVBI = 0.

Figure 5a. Interlaced 625-Line (PAL–B, D, G, H, I, Nc) Video Timing



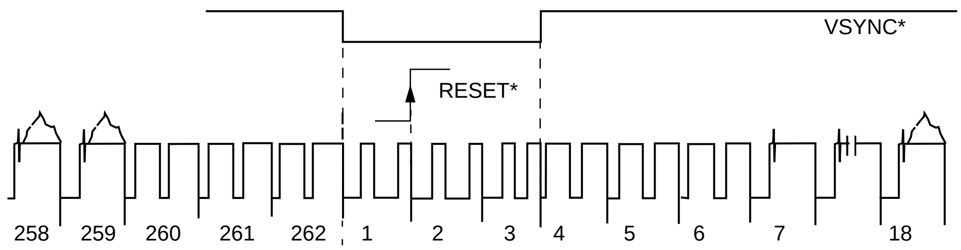
Note: EVBI = 0.

Figure 5b. Interlaced 625-Line (PAL–B, D, G, H, I, Nc) Video Timing



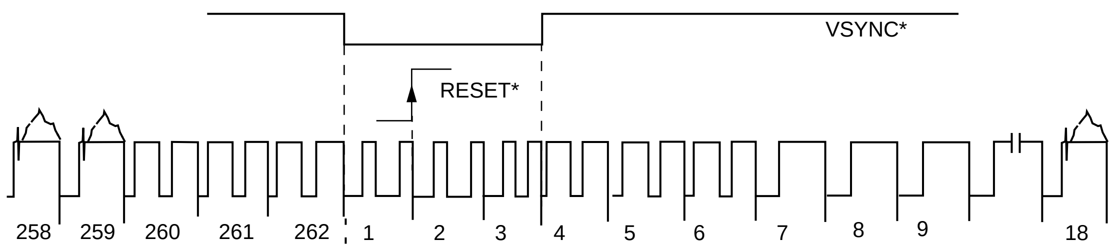
Note: EVBI = 0.

Figure 6. Noninterlaced 262-Line (NTSC) Video Timing



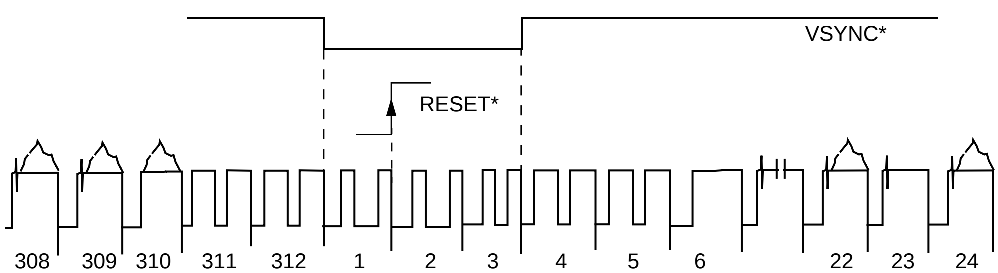
Note: CCIR 624 line numbering convention. EVBI = 0.

Figure 7. Noninterlaced 262-Line (PAL-M) Video Timing



Note: CCIR 624 line numbering convention. EVBI = 0.

Figure 8. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, N_C) Video Timing



Note: EVBI = 0.

Reset

If the RESET* pin is held low during a single rising edge of CLK, the subcarrier phase is set to zero, and the horizontal and vertical counters are held to the first pixel and second line of FIELD1. Counting resumes on the first rising edge of CLK after rising RESET*. A software reset will occur immediately after writing a 1 to register SRESET. This will reset all software-programmable register bits to zero.

On power-up, the Bt864/865 will automatically perform a timing and software reset. The power-up state has the following configuration: interlaced, NTSC CCIR601 black burst (no active video), and zero chroma scaling. Setting register EACTIVE will enable active video. On power-up, the DACs are disabled for 8 fields or until register 0x6F (0xD5 as 8-bit address) is written.

Sync and Burst Timing

Table 2 lists the resolutions and clock rates for the various modes of operation.

Table 3 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked.

The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync.

The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, Nc above the blanking level).

The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, Nc above the blanking level).

Table 2. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active Luminance Resolution (pixels)			Total Resolution (pixels)			Luminance Pixel Frequency (MHz)
	Horizontal	Vertical		Horizontal	Vertical		
	Porch = 0	Non Interlaced Field	Interlaced Frame		Non Interlaced	Interlaced	
NTSC/PAL–M CCIR601	711	241	482	858 ± 1	262 ± 1/4	262.5 ± 1/4	13.5000
PAL–B, D, G, H, I, N, Nc CCIR601	702	287	575	864 ± 1	312 ± 1/4	312.5 ± 1/4	13.5000
NTSC/PAL–M Square Pixel	647	241	482	780 ± 1	262 ± 1/4	262.5 ± 1/4	12.2727
PAL–B, D, G, H, I, N, Nc Square Pixel	767	287	575	944 ± 1	312 ± 1/4	312.5 ± 1/4	14.7500

Notes: 1. Tolerances apply to slave mode. Cumulative errors over color frame interval may result in subcarrier glitches.
2. Due to upsampling filter response, pixels near the boundary of the active definition will be reduced in amplitude due to averaging with the blank level.

Table 3. Horizontal Counter Values for Various Video Timings

Operating Mode	Horizontal Counter Value											
	Equalization Pulse Width		Horizontal/Serration Pulse Width		Start of Burst		Duration of Burst		Back Porch		Front Porch(1)	
	HCNT	μs	HCNT	μs	HCNT	μs	HCNT	μs	HCNT	μs	HCNT	μs
NTSC CCIR601	32	2.37	63	4.67	72	5.33	34	2.52	127	9.41	20	1.48
PAL–M CCIR601	32	2.37	63	4.67	78	5.78	34	2.52	127	9.41	20	1.48
NTSC Square	29	2.36	58	4.73	65	5.30	31	2.53	115	9.37	18	1.47
PAL–M Square	29	2.36	58	4.73	71	5.79	31	2.53	115	9.37	18	1.47
PAL-B CCIR601	32	2.37	63	4.67	76	5.63	30	2.22	142	10.52	20	1.48
PAL–N_c CCIR601	32	2.37	63	4.67	76	5.63	34	2.52	142	10.52	20	1.48
PAL–B Square	35	2.37	69	4.68	83	5.63	33	2.24	155	10.51	22	1.49
PAL-N_c Square(2)	35	2.37	69	4.68	83	5.63	37	2.51	155	10.51	22	1.49

Notes: (1). In slave mode, since Front Porch timing is triggered by the previous HSYNC pulse, any deviation from nominal line length can affect the front porch duration.
(2). PAL-N_c refers to the PAL format used in Argentina (Combination N).
3. HCNT refers to the number of luminance pixel periods; with respect to the CLK pin, there are twice as many CLK periods as HCNT periods.
4. Odd counts at front porch transitions indicate invalid chroma framing

Master Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and from optional software bits. HSYNC* and VSYNC* are output following the rising edge of CLK.

The HSYNC* output may be configured to have standard video timing (4.7 μs wide, asserted at start of a line default after RESET cycle) or it may be programmed to specify the start of HSYNC* (10-bit value) and the end of HSYNC* (10-bit value). VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively. When HSYNC* is configured for standard video timing, coincident falling edges of HSYNC* and VSYNC* indicate the beginning of the first field (CCIR convention).

Slave Mode

The horizontal counter is incremented on every other rising edge of CLK. A falling edge of HSYNC* resets it to one, indicating the start of a new line.

The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

A falling edge of VSYNC* that occurs within ±1/4 of a scan line from the falling edge of HSYNC* indicates the beginning of FIELD 1. A falling edge of VSYNC* that occurs within ±1/4 scan line from the center of the line indicates the beginning of FIELD 2. Referring to Figures 3–8, start of VSYNC* occurs on the falling HSYNC* at the beginning of the next expected FIELD 1 and halfway between expected falling HSYNC* edges at the beginning of the next expected FIELD 2.

HSYNC* and VSYNC* must remain low for at least 2 CLK cycles. The operating mode (NTSC/PAL, interlaced/noninterlaced, square pixel/CCIR601, and setup) is automatically determined when configured as a slave when the SETMODE bit is zero. 525-line operation is assumed, unless 625-line operation is detected by the number of lines in a field. Interlaced operation is detected by observing the sequence of FIELD 1 or FIELD 2; if the field timing (odd follows odd, even follows even) is repeated, then noninterlaced mode is assumed. The frequency of operation (square pixels or CCIR) is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz unless the exact horizontal count for square pixels, ±1 count, is detected in between two successive falling edges of HSYNC*.

NOTE: Square pixel 625-line operation with this sequence requires one frame to stabilize.

By setting SETMODE = 1, the video format control register bits (VIDFORM [3:0], SETUPDIS, NONINL, and SQUARE) will determine the operating mode.

FIELD Output

The FIELD output indicates whether FIELD 1 (logical zero) or FIELD 2 (logical one) is being generated. This corresponds directly to the "bottom/top" convention of some MPEG decoders. Field changes occur one CLK cycle after the falling edge of VSYNC*. FIELD is output following the rising edge of CLK. Unless special HSYNC* timing is programmed, FIELD output transitions low four CLK periods following the falling edge of HSYNC* at the beginning of FIELD 1.

To invert the sense of the FIELD output, set the FIELD 1 bit to a logical one.

Pixel Blanking

BLANK* is registered on the rising edge of CLK. For video outputs, BLANK* is pipelined to match the luminance and chrominance paths and is applied to the digital video before analog conversion. The automatic horizontal blanking sequence described in Table 3 takes precedence over the BLANK* input.

Burst Blanking

For interlaced NTSC, color burst information is automatically disabled on scan lines 1–9 and 264–272, inclusive. (SMPTE line numbering convention.)

For interlaced PAL-M color burst information is automatically disabled on scan lines 1–11 and 263–273 and 525 of FIELD 1 and FIELD 2 and scan lines 1–10 and 262–272 of FIELDs 3 and 4.

For interlaced PAL–B, D, G, H, I, N, Nc, color burst information is automatically disabled on scan lines 1–6, 310–318, and 623–625, inclusive, for FIELDs 1, 2, 5, and 6. During FIELDs 3, 4, 7, and 8, color burst information is disabled on scan lines 1–5, 311–319, and 622–625, inclusive.

For noninterlaced NTSC, color burst information is automatically disabled on scan lines 1–6 and 261–262, inclusive.

For noninterlaced PAL-M, color burst information is automatically disabled on scan lines 1–10 and 262–272.

For noninterlaced PAL–B, D, G, H, I, N, Nc, color burst information is automatically disabled on scan lines 1–6 and 310–312, inclusive. See Figures 3–8.

Digital Processing

The input is scaled to YUV format. For the CVBS, Y, and C outputs, the UV components are low-pass filtered with a filter response shown in Figures 9a and 9b (linearly scalable by clock frequency). The Y and filtered UV components are upsampled to CLK frequency by a digital filter whose response is shown in Figures 10a and 10b. For the RGB outputs, the scaled YUV is color space converted and output.

Chrominance Disable

The chrominance subcarrier may be turned off by setting the DCHROMA bit to a logical one. This kills burst as well, providing luminance only signals on the CVBS outputs and a static blank level on the C/R output (RGBOUT = 0).

Figure 9a. Three-Stage Chrominance Filter

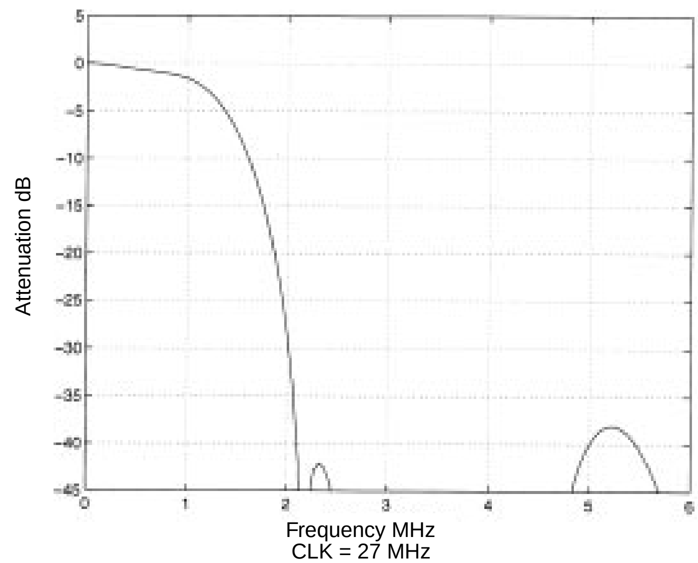


Figure 9b. Three-Stage Chrominance Filter (Passband)

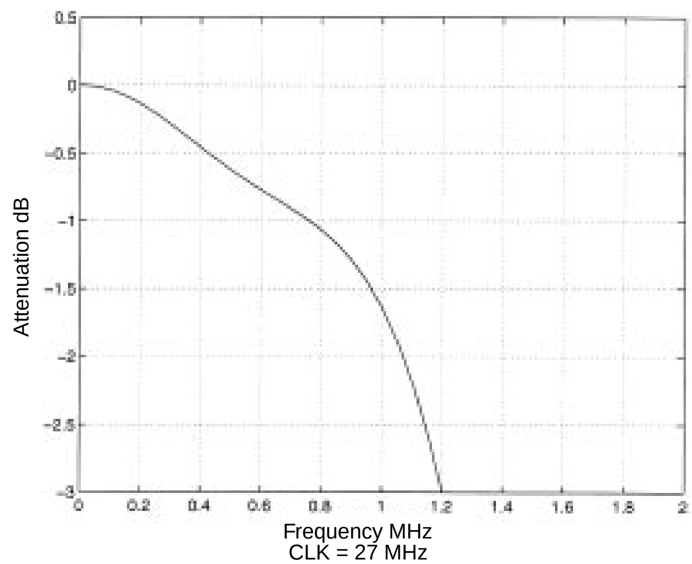


Figure 10a. Luminance 2X Upsampling Filter Response

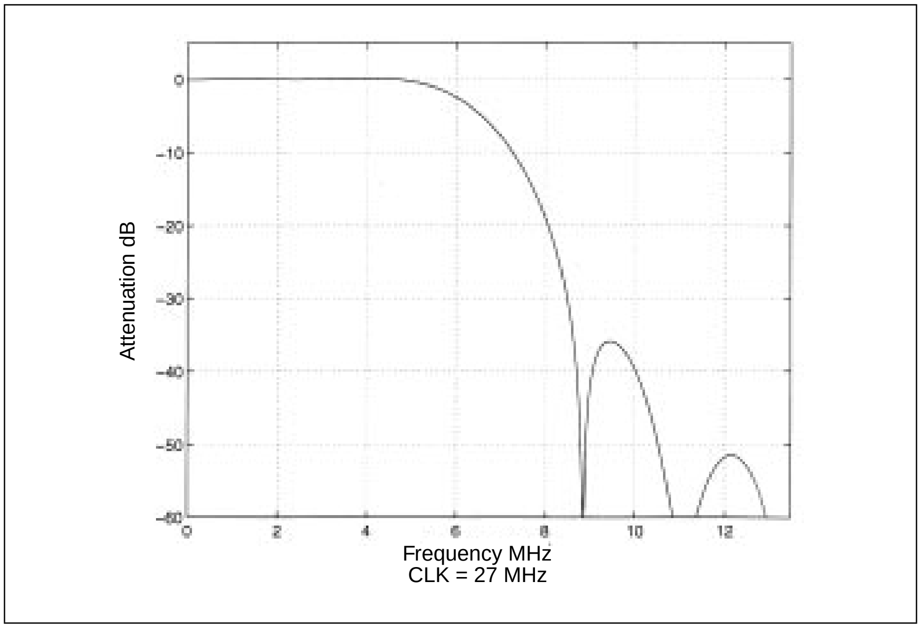
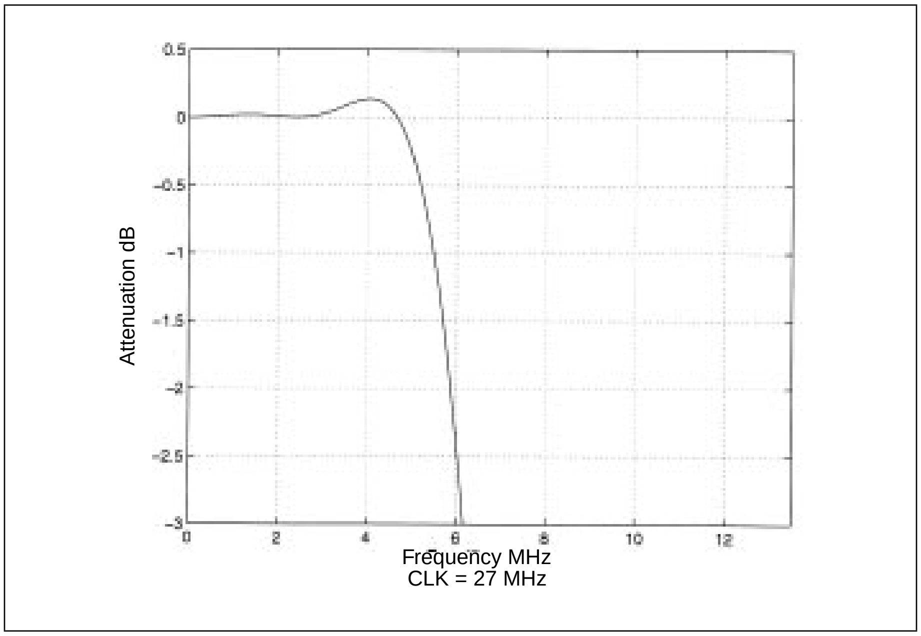


Figure 10b. Luminance 2X Upsampling Filter Response (Passband)



Subcarrier Phasing

In order to maintain correct SC-H phasing, subcarrier phase is set to zero on the falling edge of HSYNC* associated with VSYNC* every four (NTSC) or eight (PAL) fields, unless the SCRESET bit is set to a logical one.

In slave mode, falling HSYNC* may lag falling VSYNC* by 1/4 scan line but cannot precede falling VSYNC* by more than seven CLK periods for correct SC-H reset.

Setting SCRESET to one may be useful in situations where the ratio of CLK/2 to HSYNC* edges in a color frame is noninteger, which could produce a significant phase impulse by resetting to zero.

Vertical Blanking Intervals

For interlaced NTSC/PAL–M, if EVBI = 0, scan lines 1–21 and 263–284, inclusive, are always blanked regardless of the BLANK* input (SMPTE line numbering convention).

For interlaced PAL–B, D, G, H, I, N, Nc, if EVBI = 0, scan lines 1–23, 311–335, and 624–625, inclusive, are always blanked regardless of the BLANK* input.

For noninterlaced NTSC/PAL–M, if EVBI = 0, scan lines 1–17 and 261–262, inclusive, are always blanked regardless of the BLANK* input. For noninterlaced PAL–B, D, G, H, I, N, Nc, if EVBI = 0, scan lines 1–22 and 311–312, inclusive, are always blanked regardless of the BLANK* input.

Alternately, all displayed lines in the vertical blanking interval (10–21 and 273–284 for interlaced NTSC/PAL–M; 6–23 and 320–335 for interlaced PAL–B, D, G, H, I, N, Nc; 10–21 for noninterlaced NTSC/PAL–M, 7–23 for noninterlaced PAL–B, D, G, H, I, N, Nc) may be enabled by setting the EVBI bit to a logical one (except for caption lines controlled by bits ECCF1 or ECCF2, or the Macrovision process).

BLANK* Pin

The BLANK* pin can be used to BLANK any portion of the active display lines (including those enabled by EVBI) by driving the pin to a logical zero.

Noninterlaced Operation

When the Bt864/865 is programmed for noninterlaced master mode, the Bt864/865 always displays FIELD 1, meaning that the falling edges of HSYNC* and VSYNC* will be output coincidentally. FIELD will be held low if FIELDI = 0. Additionally, a 30 Hz offset will be subtracted from the color subcarrier frequency while in NTSC mode so that the color subcarrier phase will be inverted from field to field.

Transition from interlaced to noninterlaced in master mode, occurs during FIELD 1 to prevent synchronization disturbance. In slave mode, transition occurs after a subsequent falling edge of VSYNC*.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan > 2x) may not function properly.

Power Saving Modes

In power-down mode (SLEEP pin set to 1), register states are preserved, but other chip functionality (including I^2C communication) is disabled. This mode should be set when the Bt864/865 may be subjected to clock and data frequencies outside its functional range.

When DACs are disabled by either SLEEP or DACOFF, VREF will go to approximately 0.5 V below VAA.

Pixel Input Ranges and Colorspace Conversion

YC Inputs (4:2:2 YCrCb)

Y has a nominal range of 16–235; Cb and Cr have a nominal range of 16–240, with 128 equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

The SETUPDIS bit will alter pixel scaling and disable or enable the 7.5 IRE setup. When this bit is enabled, PAL–B, D, G, H, I, N, Nc video can be generated using NTSC/PAL–M blanking levels and 7.5 IRE setup, and NTSC/PAL–M pixel scaling is performed (Y range of 16–235 represents 7.5–100 IRE); or, NTSC/PAL–M video can be generated using PAL–B, D, G, H, I, N, Nc scaling (Y range of 16–235 represents 0–100 IRE) without the 7.5 IRE setup. NTSC/PAL–M mode with setup disabled has 2% less black-to-white range than NTSC/PAL–M mode with setup enabled.

For RGBOUT mode, 4:2:2 YCrCb digital component video will be upsampled to 4:4:4 and used to generate composite video and will be converted to the RGB colorspace to drive the RGB DACs. The Y input range of 16–235 will produce a range of 0.7 V at the output. Since YC values outside of the nominal range are allowed, the black level is raised above zero volts to allow for Y values less than 16, and the output range of the DACs can exceed 0.7 V to allow for Y values above 235. The conversion is linearly scaled in the overshoot and undershoot regions. The following matrix, based on CCIR601, is used to convert YCrCb to RGB:

$R = Y + 1.371*Cr$

$G = Y - 0.699*Cr - 0.337*Cb$

$B = Y + 1.733*Cb$

Values are rounded to 9 bits at the DAC.

DAC Coding

For all video formats, the input luma and chroma values are scaled internally such that, after sync and setup (if enabled) are added, the output from sync to 100% white (for CVBS/Y outputs) is approximately 1.00 V.

In addition, the chroma is boosted to compensate for the sinx/x rolloff due to the DAC (see Figures 11a and 11b). The amount of boost is determined by SETUPDIS. Table 4 summarizes the blank, black, and 100% white DAC codes and chroma gain values as a function of SETUPDIS.

Table 4. DAC Coding

SETUPDIS	Blank	Black	100% White	Chroma Gain
0	228	272	801	1.02944
1	224	224	800	1.0458

Figure 11a. DAC Sinx/x Response

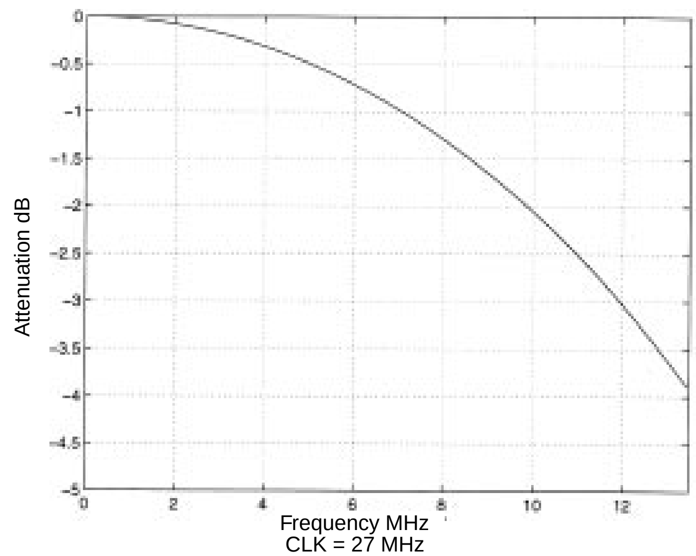
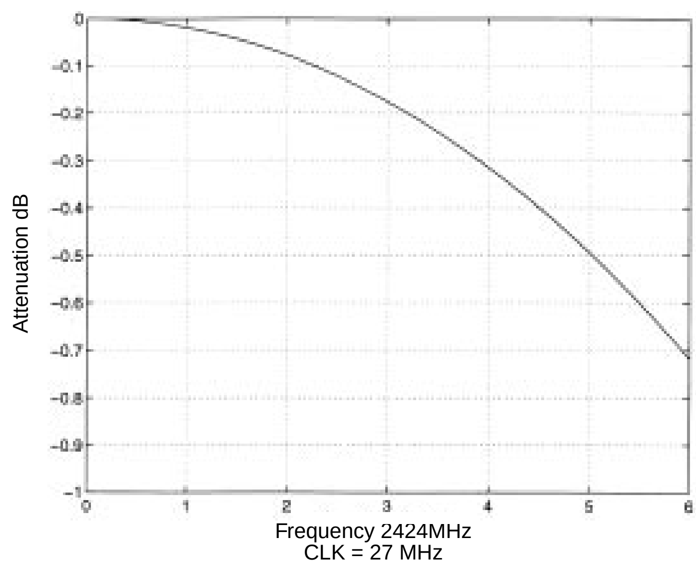


Figure 11b. DAC Sinx/x Response (Passband)



Closed Captioning

The Bt864/865 encodes NTSC/PAL–M closed captioning on scan line 21 and NTSC/PAL–M extended data services on scan line 284. Four 8-bit registers (CCF1B1, CCF1B2, CCF2B1, and CCF2B2) provide the data while bits ECCF1and ECCF2 enable display of the data. A logical zero corresponds to the blanking level of 0 IRE, while a logical one corresponds to 50 IRE above the blanking level.

Closed captioning for PAL–B, D, G, H, I, N, Nc is similar to that for NTSC. Closed caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC system, except that encoding is provided on lines 22 and 335.

The Bt864/865 generates the clock run-in and appropriate timing automatically. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47 Section 15.119 (10/91 edition or later) for programming information. EIA608 describes ancillary data applications for FIELD 2 Line 21 (line 284).

When CCF1B2 is written, CCSTAT1 is set; when CCF2B2 is written CCSTAT2 is set. After the closed-caption bytes for FIELD 1 are encoded, CCSTAT1 is cleared; after the closed-caption bytes for FIELD 2 are encoded, CCSTAT2 is cleared. If the ECCGATE bit is set, no further encoding will be performed until the appropriate registers are again written; a NULL with odd parity will be transmitted on the appropriate closed caption line in that case. User must set the odd parity bit. If the ECCGATE bit is not set, the user must rewrite the closed-caption registers prior to reaching the closed-caption line, otherwise the last bytes will be re-encoded.

Closed-caption will override EVBI inserted data on lines 21 and 284 for 525-line formats, and lines 22 and 335 for 625-line formats. Closed-caption will be overridden by teletext if teletext is enabled on these lines.

Teletext

Teletext encoding is accomplished via a two-wire interface, TTXDAT and TTXREQ, and internal registers that are programmed through the I^2C interface. Teletext encoding in the Bt864/865 conforms to Teletext B for 625/50 television systems. See “Recommendation 653-1 Teletext Systems” for further information about the standard. Teletext should be disabled for 525-line television systems.

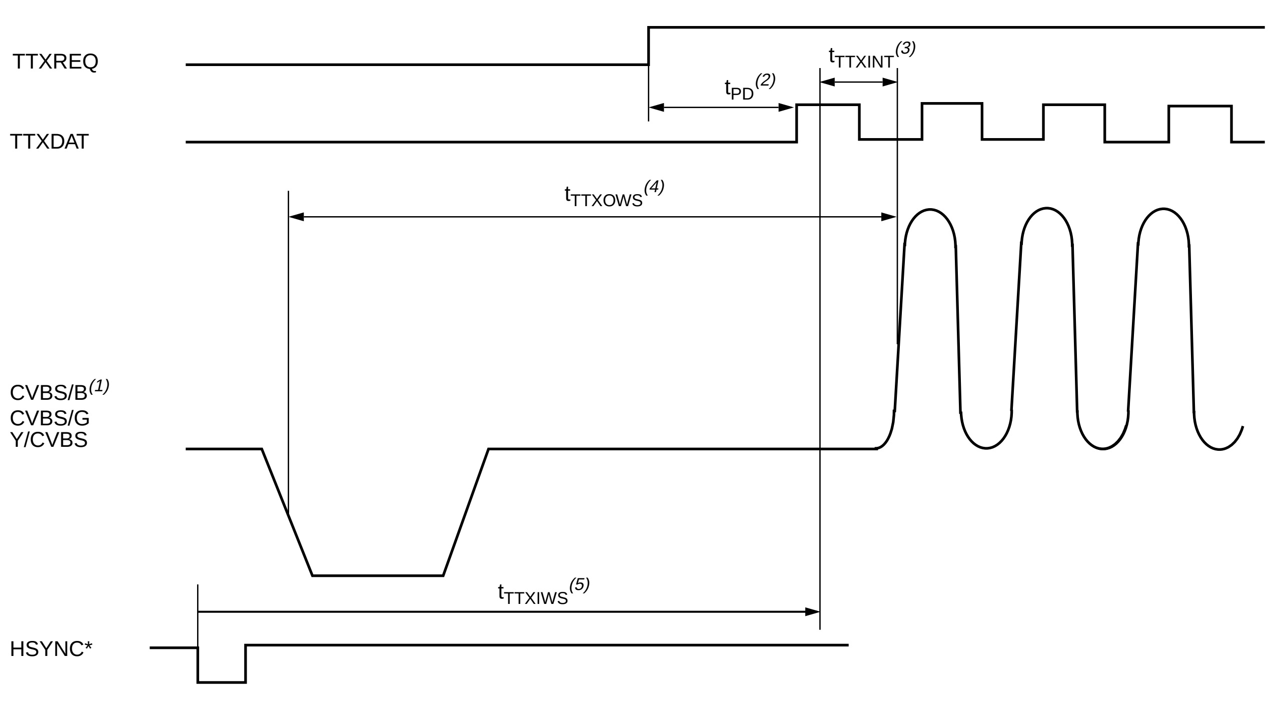
The internal registers allow for the enable/disable of teletext and the programming of the start and stop of the TTXREQ signal, the active teletext lines in an FIELD 1, and the active teletext lines in FIELD 2. Active teletext lines override closed caption, Macrovision, the BLANK* input, and active video. See the “Internal Registers” section for more details.

The following information will use the device clock, CLK, which is twice the input pixel rate, as a reference. The TTXREQ is generated by the encoder to indicate the start of teletext data to the TTXDAT pin on each active teletext line (see Figure 12). The TTXREQ signal's rising and falling edges are programmable to the resolution of CLK and are adjusted to account for the propagation delay of the teletext source so that the teletext data is provided to the TTXDAT pin at the proper time. If the falling edge is programmed to be longer than the video line length, the start of a new video line will clear TTXREQ.

The data to TTXDAT is sampled on every rising input clock edge and must meet the following protocol for proper teletext data insertion. The protocol demands that the teletext data bit duration is the required number of CLKs.

Internal to the chip is a sequencer and a data shaper to minimize the jitter. Using the midpoint of the falling edge of the horizontal sync pulse as it appears at the output Y/CVBS or CVBS/G, the teletext data protocol must begin 262 to 264 CLKs later for CCIR601(13.5 MHz pixel rate) or 286 to 288 CLKs later for Square Pixel Operation (14.75 MHz pixel rate). Relative to the internally generated teletext window, the protocol must start 5 to 7 clocks earlier. The teletext window begins at 10.2 µsec from the horizontal sync pulse's falling edge and the data rate is the specified 6.9375 Mbits/sec.

Figure 12. Teletext Timing for Bt864/865 Encoder



Notes: (1). Luma Delay is set to zero.
(2). TTXREQ is generated by encoder using programmable registers TXHS and TXHE. This allows the user to adjust for the propagation delay (t_{PD}) in CLK cycles of the teletext data source.
(3). TTXDAT is supplied to the encoder at the proper time to be interpolated by the encoder (t_{TTXINT}) and inserted into the video output signals. The Teletext data must follow the correct protocol. See “Teletext” on page 23.
(4). t_{TTXOWS} is the start of the teletext output window and is fixed internally by the encoder at 10.2 μsec.
(5). t_{TTXIWS} is the start of the teletext input window and is fixed internally.
6. TXE is enabled and video line is a valid teletext line. See “Teletext” on page 23.

CCIR601 Operation (13.5 MHz pixel rate)

The bit duration follows this pattern which repeats every 37 teletext bits. Each teletext data bit is carried by four CLKs except bits 10, 19, 28, and 37 which are three CLKs in duration. This pattern continues until all 360 bits (1402 CLKs) have been transferred.

Square Pixel Operation (14.75 MHz pixel rate)

This bit pattern repeats after every 111 teletext bits: After every teletext bit that is carried by five CLKs the next three teletext bits are carried by four CLKs except for the first bit of the pattern which is five CLKs in duration and only the next two bits are carried by four CLKs. This pattern continues until all 360 bits (1531 CLKs) have been transferred. The repeating bit duration pattern starting at bit 1 would be:

Bit number:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15...
Duration in CLKs:	5	4	4	5	4	4	4	5	4	4	4	5	4	4	4...

Teletext Clock Generation

Figure 13 shows how to generate a teletext clock using a P:Q ratio counter for shifting out the teletext data serially to the Bt864/865. The diagram is for illustrative purposes only. The actual implementation is left to the user.

Figure 13. PQ Ratio Counter

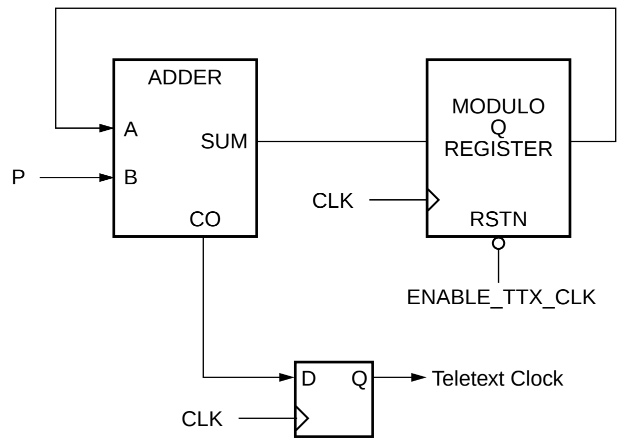


Table 5. Teletext Clock P and Q Values

CLK	Pixel Rate	P	Q
27 MHz	13.5 MHz	37	144
29.5 MHz	14.75 MHz	111	472

Anticopy Process (Bt865 Only)

The anticopy process contained within the Bt865 is implemented according to the Macrovision revision 6.1 specification developed by Macrovision Corporation in Sunnyvale, California. All luminance, chrominance, and composite video waveforms include the Macrovision Anticopy Process. Macrovision is not supported in RGB mode. The Bt865 incorporates an anticopy process technology that is protected by U.S. patents and other intellectual property rights. The anticopy process is licensed for noncommercial, home use only. Reverse engineering or disassembly is prohibited.

Brooktree cannot ship Bt865 units to any customer until that customer has been approved by Macrovision. To obtain approval for shipment of Bt865 samples, a "Macrovision Proprietary Material License Agreement" is required. Contact Macrovision Corporation to facilitate this agreement.

Internal Color Bars

The Bt864/865 can be configured to internally generate colorbar test patterns (100/7.5/75/7.5 with SETUPDIS = 0 for NTSC/PAL-M; 100/0/75/0 with SETUPDIS = 1 for PAL).

Internal color bars can be enabled by setting the ECBAR bit to a logical one. In 8-bit YCrCb mode, setting the Y[7] pin to a logical one also enables color bars, thereby simplifying testing of various modes. Internal color bars can be enabled in all video formats.

SCART/PeriTV Support

RGBOUT mode can be enabled by setting the RGBOUT pin to a logical one, or by setting register bit RGBO. Bt864/865 can generate analog RGB video signals to interface to a SCART/PeriTV connector (see Table 6). Composite video will be present on the Y/CVBS DAC. RGB outputs are nominally 700 mVpp (black to white without setup).

I²C Interface

A simplified I²C (7-bit subaddress, 100 Kbps) interface is provided for programming the registers. CLK must be applied and stable for I²C communication. Activating SLEEP or RESET* will disable I²C communication.

Analog Outputs

All digital-to-analog converters are designed to drive standard video levels into a combined RLOAD of 37.5 Ω. Unused outputs should be connected directly to ground to minimize supply switching currents. In standard mode, one S-Video (YC), and two composite video outputs are available. In RGBOUT mode, one composite video output along with analog RGB are available (see Table 6). If the SLEEP pin is high, the DACs are essentially turned off and only the leakage current is present. The D/A converter values for 100% saturation, 100% amplitude color bars are shown in Figures 14–19. Both composite video and analog RGB video (to provide support for SCART/PeriTV) may be generated simultaneously.

Table 6. DAC Output Cross-Reference

DAC Name	Pin Number		Pin Function	
	Signal	AGND	Std Mode	RGB Out Mode
CVBS/B	8	6	CVBS	B
CVBS/G	10	7	CVBS	G
C/R	12	9	C	R
Y/CVBS	13	11	Y	CVBS

Luminance or CVBS (Y/CVBS) Output

Digital luminance information drives the 10-bit D/A converter that generates the analog Y video output (Figures 14 and 15 and Tables 7 and 8). This DAC can also provide CVBS for SCART/PeriTV synchronization when RGBOUT is enabled.

Chrominance or Red (C/R) Output

Digital chrominance information drives the 10-bit D/A converter that generates the analog C video output (Figures 16 and 17 and Tables 9 and 10). This DAC can also provide Red for SCART/PeriTV when RGBOUT is enabled.

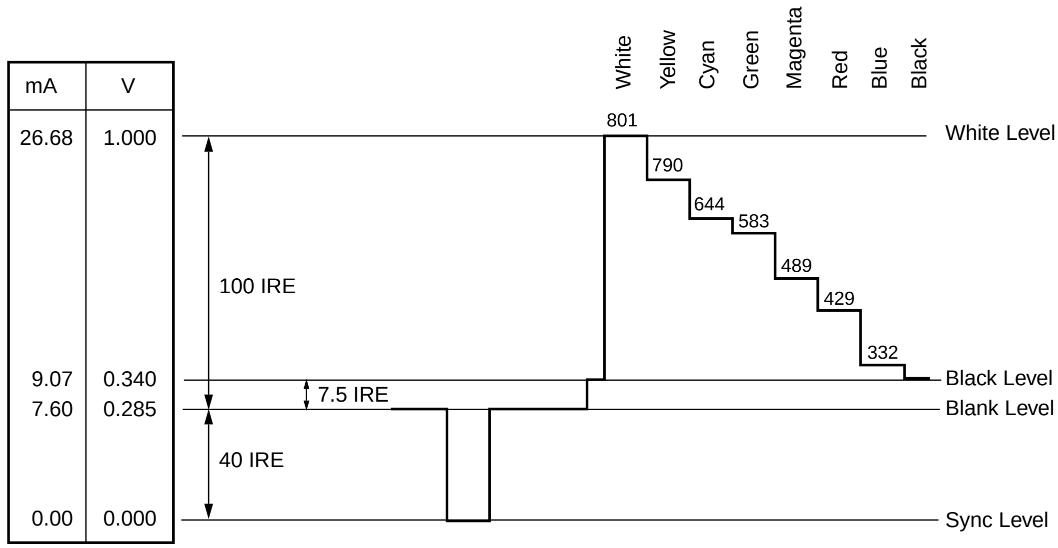
Composite Video or Blue (CVBS/B) Output

Digital composite video information drives the 10-bit D/A converter that generates the analog NTSC or PAL video output (Figures 18 and 19 and Tables 11 and 12). This DAC can also provide Blue for SCART/PeriTV when RGBOUT is enabled. An optional luminance delay can be enabled on this pin (in standard mode only) by setting the LUMADLY bits. The luma can be delayed 0 to 3 pixels (up to 200–245 ns) to compensate for group delays introduced in the chroma path by external filters or vestigial sideband processing.

Composite Video (CVBS/G) Output

Digital composite video information drives the 10-bit D/A converter that generates the analog video output (Table 13). This DAC can also provide Green for SCART/PeriTV when RGBOUT mode is enabled.

Figure 14. SETUPDIS = 0, Y (Luminance) Video Output Waveform



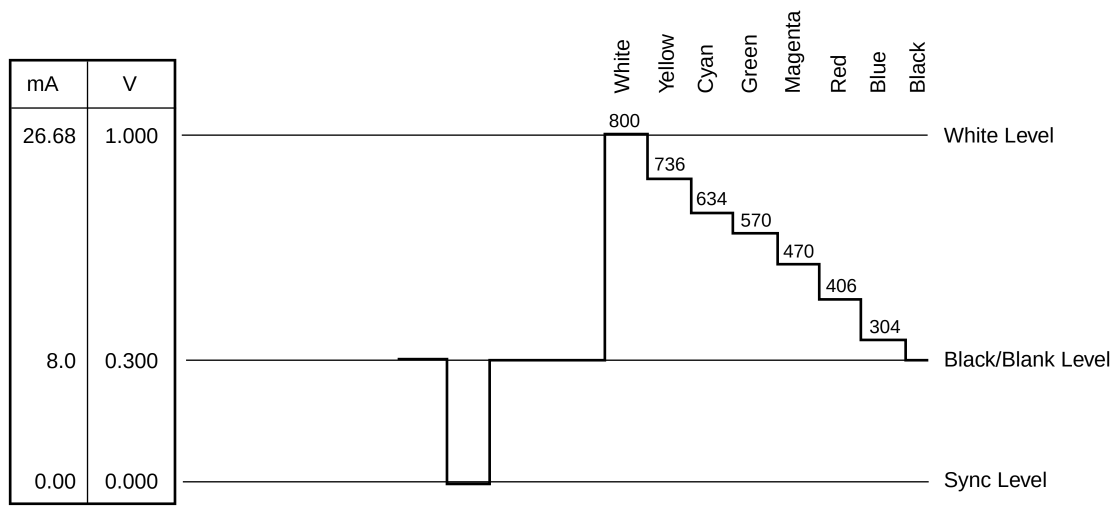
Note: Typical with 37.5 Ω load, nominal RSET. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 7. SETUPDIS = 0, Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
White	26.68	801	0	1
Black	9.07	272	0	1
Blank	7.60	228	0	0
Sync	0	0	1	0

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load, nominal RSET, and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 15. SETUPDIS = 1, Y (Luminance) Video Output Waveform



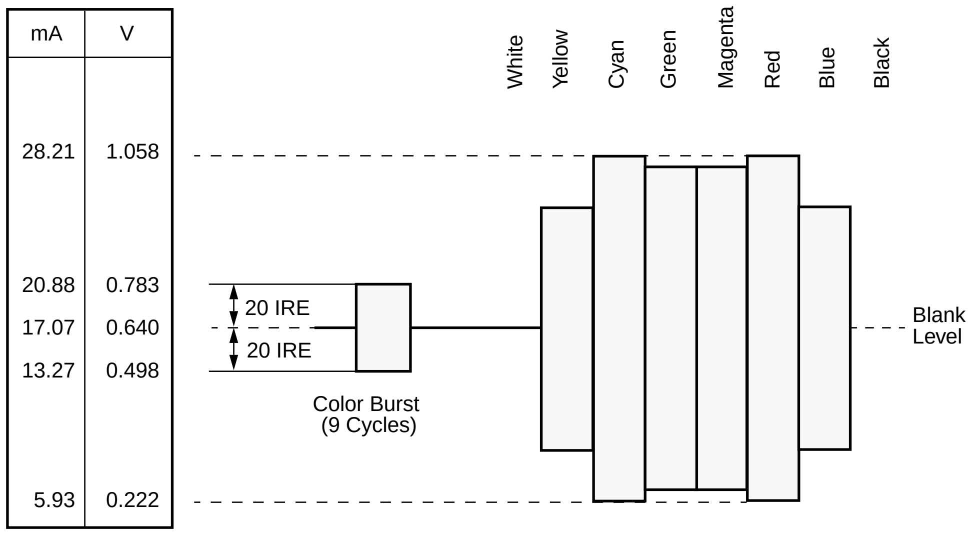
Note: Typical with 37.5 Ω load and nominal RSET. ITU-RBT.470-3 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 8. SETUPDIS = 1, Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
White	28.68	800	0	1
Black	8.00	240	0	1
Blank	8.00	240	0	0
Sync	0	0	1	0

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load and nominal RSET. ITU-RBT.470-3 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 16. SETUPDIS = 0, C (Chrominance) Video Output Waveform



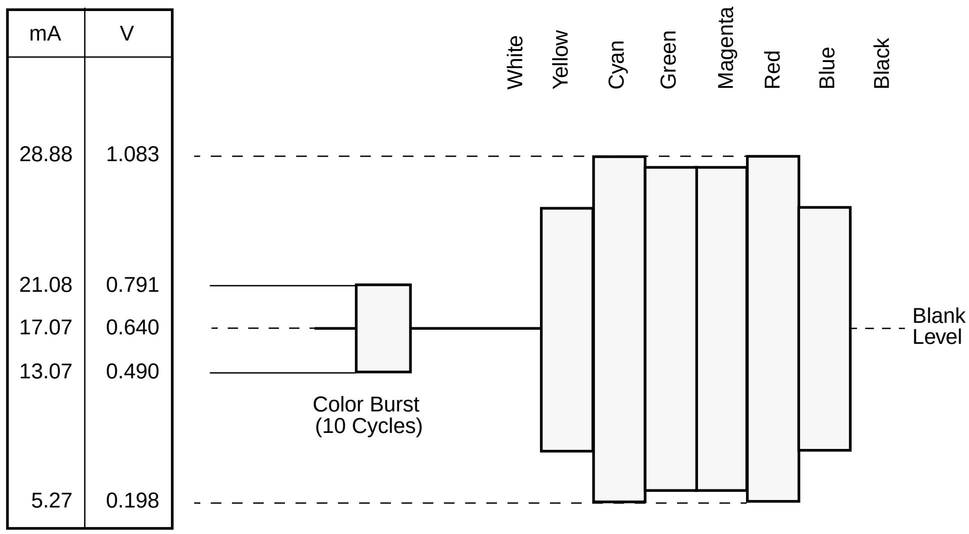
Note: Typical with 37.5 Ω load, nominal RSET, and chroma on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 9. SETUPDIS = 0, C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
Peak Chroma (High)	28.21 [25.56]	856 [770]	x	1
Burst (High)	20.88 [20.88]	629 [629]	x	x
Blank	17.07 [17.07]	512 [512]	x	0
Burst (Low)	13.27 [13.27]	395 [395]	x	x
Peak Chroma (Low)	5.93 [8.53]	168 [254]	x	1

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load, nominal RSET, and chroma on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.
3. Bracketed values indicate expected values when using the internal color bars (100/7.5/75/7.5).

Figure 17. SETUPDIS = 1, C (Chrominance) Video Output Waveform



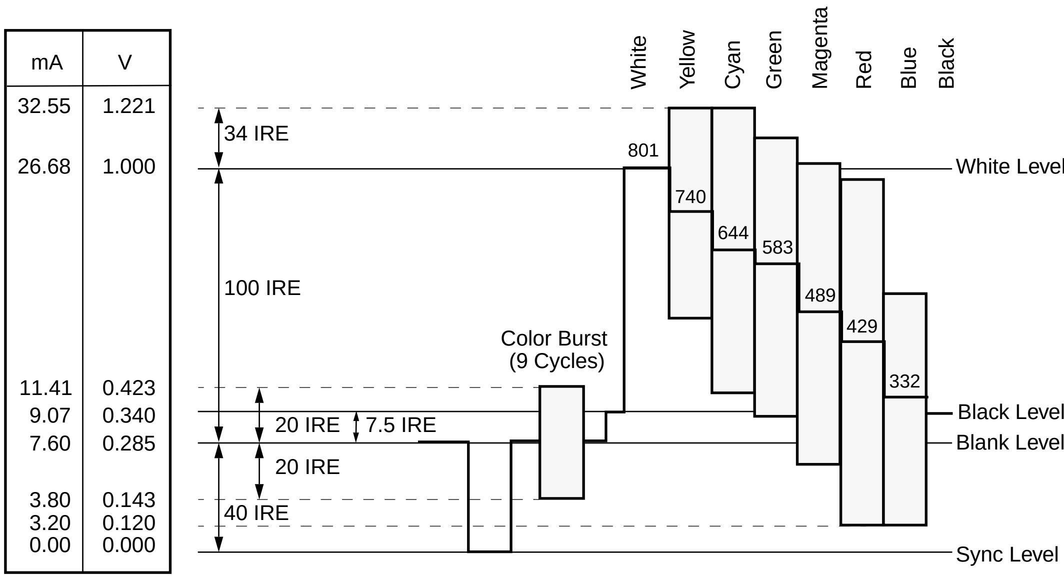
Note: Typical with 37.5 Ω load, nominal RSET, and chroma on. ITU-RBT.470-3 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 10. SETUPDIS = 1, C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
Peak Chroma (High)	28.88 [26.06]	877 [785]	x	1
Burst (High)	21.08 [21.08]	635 [635]	x	x
Blank	17.07 [17.07]	512 [512]	x	0
Burst (Low)	13.07 [13.07]	389 [389]	x	x
Peak Chroma (Low)	5.27 [7.97]	147 [239]	x	1

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load, nominal RSET, and chroma on. ITU-RBT.470-3 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.
3. Bracketed values indicate expected values when using the internal color bars (100/0/75/0).

Figure 18. SETUPDIS = 0, Video Output Waveform



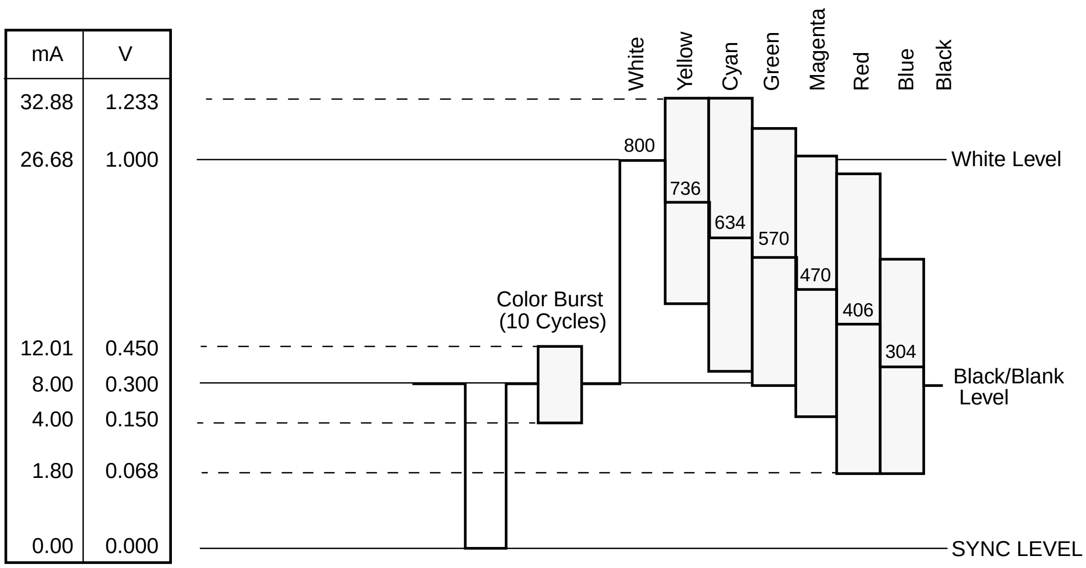
Note: Typical with 37.5 Ω load, nominal RSET, clipping off, and chroma on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 11. SETUPDIS = 0, Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
Peak Chroma (High)	32.55 [30.38]	988 [922]	0	1
White	26.68 [26.68]	801 [801]	0	1
Burst (High)	11.41 [11.41]	345 [345]	0	x
Black	9.07 [9.07]	272 [272]	0	1
Blank	7.60 [7.60]	228 [228]	0	0
Burst (Low)	3.80 [3.80]	111 [111]	0	x
Peak Chroma (Low)	3.20 [5.32]	85 [149]	0	1
Sync	0 [0]	0 [0]	1	0

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load, nominal RSET, clipping off, and chroma on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.
3. Bracketed values indicate expected values when using the internal color bars (100/7.5/75/7.5).

Figure 19. SETUPDIS = 1, Video Output Waveform



Note: Typical with 37.5 Ω load, nominal RSET, and clipping off. ITU-RBT.470-3 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.

Table 12. SETUPDIS = 1, Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*(1)
Peak Chroma (High)	32.88 [30.61]	998 [929]	0	1
White	26.68 [26.68]	800 [800]	0	1
Burst (High)	12.01 [12.01]	363 [363]	0	x
Black	8.00 [8.00]	240 [240]	0	1
Blank	8.00 [8.00]	240 [240]	0	0
Burst (Low)	4.00 [4.00]	117 [117]	0	x
Peak Chroma (Low)	1.80 [3.76]	41 [110]	0	1
Sync	0 [0]	0 [0]	1	0

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Typical with 37.5 Ω load, nominal RSET, and clipping off. ITU-RBT.470-3 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.
3. Bracketed values indicate expected values when using the internal color bars (100/0/75/0).

Table 13. RGB Output Table (RGBOUT = 1)

Description	SETUPDIS = 1		SETUPDIS = 0		BLANK*(1)
	Iout (mA)	DAC Data	Iout (mA)	DAC Data	
White	18.68	560	18.68	560	1
Black	0	0	1.47	44	1
Blank	0	0	0	0	0

Notes: (1). BLANK occurs by external BLANK* pin or internally generated BLANK.
2. Iout typical with 37.5 Ω load, nominal RSET.

INTERNAL REGISTERS

A read-back bit map is given in Table 14, and a register bit map is given in Table 15. Bit descriptions and detailed programming information follow the bit map. All registers are write-only and are set to zero following a software reset. A software reset is always performed at power-up; after power-up, a reset can be triggered by writing the SRESET register bit. Figure 22 illustrates timing required for I^2C communications.

Table 14. Read-back Bit Map

ESTATUS	7	6	5	4	3	2	1	0
0	ID[2:0]			VERSION[4:0]				
1	ID[2:0]			CCSTAT[2]	CCSTAT[1]	FIELD[2:0]		

Note: The ID[2:0] bits indicate the part number: 4 is returned from the Bt864; 5 is returned from the Bt865. The version number is indicated by bits VERSION[4:0]. For this revision, VERSION[4:0] = 0x01. The CCSTAT[2] bit is high if closed-caption data has been written for the even field; it is low immediately after the clock run-in on line 284 or 335. The CCSTAT[1] bit is high if closed-caption data has been written for the odd field; it is low immediately after the clock run-in on line 21 or 22. The FIELD[2:0] bits represent the field number, where 000 indicates the first field.

Essential Registers

The power-up state is defined to be blank burst CCIR601 NTSC video. To enable active video, the EACTIVE register bit must be set.

Important Registers

The default video format is interlaced 8-bit CCIR601 NTSC. Other video formats can be enabled only by programming the four following registers: 0x53, 00x65, 0x66, and 0x67. Other registers may need to be programmed to get the desired timing of the synchronization pins; these include HSYNCF[9:0] and HSYNCR[9:0].

Writing Addresses

Following a start condition, writing to slave address 0x8A initiates access to subaddresses. Alternative slave address 0x88 must be written if the ALTADDR pin is high.

Reading Information

Following a start condition, writing 0x8B initiates the read-back sequence, during which 8 bits of information can be read from the SDA pin, MSB first. Alternative address 0x89 is required if the ALTADDR pin is high. The first three bits indicate the part type (Bt864 or Bt865). The lower five bits indicate either the version number or the status bits.

Table 15. Register Bit Map

7-Bit Subaddr	8-Bit Subaddr	D7	D6	D5	D4	D3	D2	D1	D0
0x53	0xA6	SRESET	Reserved(1)						
0x54	0xA8	Reserved(1)							
0x55	0xAA	Reserved(1)							
0x56	0xAC	TXHS[7:0]							
0x57	0xAE	TXHE[7:0]							
0x58	0xB0	LUMADLY[1:0]		TXHE[10:8]			TXHS[10:8]		
0x59	0xB2	Reserved(1)			TXE	TXEF2[8]	TXBF2[8]	TXEF1[8]	TXBF1[8]
0x5A	0xB4	TXBF1[7:0]							
0x5B	0xB6	TXEF1[7:0]							
0x5C	0xB8	TXBF2[7:0]							
0x5D	0xBA	TXEF2[7:0]							
0x5E	0xBC	ECCF2	ECCF1	ECCGATE	Reserved(2)	DACOFF	YC16	CBSWAP	PORCH
0x5F	0xBE	CCF2B1[7:0]							
0x60	0xC0	CCF2B2[7:0]							
0x61	0xC2	CCF1B1[7:0]							
0x62	0xC4	CCF1B2[7:0]							
0x63	0xC6	HSYNCF[7:0]							
0x64	0xC8	HSYNCR[7:0]							
0x65	0xCA	SYNCDLY	FIELDI	SYNCDIS	ADJHSYNC	HSYNCF[9,8]		HSYNCR[9,8]	
0x66	0xCC	SETMODE	SETUPDIS	VIDFORM[3:0]				NONINTL	SQUARE
0x67	0xCE	ESTATUS	RGBO	DCHROMA	ECBAR	SCRESET	EVBI	EACTIVE	ECLIP
0x68	0xD0	Reserved(1)							
•••	•••	Reserved(1)							
0x7F	0xFE	Reserved(1)							

Notes: (1). Must be zero for normal operation. This is the default software reset state.
(2). Must be one for normal operation.
3. All subaddresses are hexadecimal. The 8-bit subaddress reflects a left-shift 8-bit subaddress with zero added as the LSB.

Programming Detail

SRESET — When set to logical one, this will reset all registers, including itself, to logical zero.

TXHS[10:0] — Relative position of rising edge on the TTXREQ pin.

TXHE[10:0] — Relative position of falling edge on the TTXREQ pin.

NOTE: Legal values to TXHS and TXHE are shown in the following table..

	Pixel rate	TXHS	TXHE
Min. Value	13.5 MHz	2	TXHS + 2
Max. Value	13.5 MHz	0X6BE	0X7FF
Min. Value	14.75 MHz	2	TXHS + 2
Max. Value	14.75 MHz	0X75E	0X7FF

LUMADLY[1,0] — This 2-bit value can be used to program the luminance delay on the CVBS/B output.

D7	D6	Function
0	0	No delay
0	1	1 pixel clock delay
1	0	2 pixel clock delay
1	1	3 pixel clock delay

TXE — 0 = Disable teletext.
1 = Enable teletext.

TXBF1[8:0] — First line of teletext, field one; TXBF1 + 1 = Std. PAL line number.

TXEF1[8:0] — Last line of teletext, field one; TXEF1= Std. PAL line number.

TXBF2[8:0] — First line of teletext, field two; TXBF2 + 313 = Std. PAL line number.

TXEF2[8:0] — Last line of teletext, field two; TXEF2 + 312 = Std. PAL line number.

ECCF2 — 0 = Disable closed-caption encoding on field 2.
1 = Enable closed-caption encoding on field 2.

ECCF1 — 0 = Disable closed-caption encoding on field 1.
1 = Enable closed-caption encoding on field 1.

ECCGATE — 0 = Normal closed-caption encoding.
1 = Enable closed-caption encoding constraints. After encoding, future encoding is disabled until a complete pair of new data bytes is received. This prevents encoding of redundant or incomplete data.

DACOFF — 0 = Normal operation.
1 = Disable DAC output current and internal voltage reference. This will limit power consumption to just the digital circuits.

NOTE: The DACOFF bit is forced high after power-up until either 8 fields have been output or register 0x67 (0xCE in 8-bit subaddress) has been written.

YC16 — 0 = 8-bit mode: YCrCb data is input on P[7:0] as 8-bit multiplexed video.
1 = 16-bit mode: YCrCb data is input on P[7:0] and Y[7:0], where multiplexed CrCb is input on P[7:0].

CBSWAP	0 = Normal pixel sequence. 1 = The Cb and Cr pixels can be swapped at the input of the pixel port. Refer to the pixel sequence section for more information.
PORCH	0 = Front and back porch timing conforms to ITU-RBT.470-3. Front porch is 1.5 µs and back porch is 9.4 for M-systems or 10.5 for PAL-systems. The active video region is therefore smaller than the 720 pixels specified in CCIR601. 1 = Redefine porch timing per CCIR601. This setting allows the full picture with 720 pixels to be encoded by using a portion of both the front and back porch for active video.
CCF2B1[7:0]	This is the first byte of closed-caption information for the FIELD 2, line 284 for NTSC or line 335 for PAL. Data is encoded LSB first.
CCF2B2[7:0]	This is the second byte of closed-caption information for the FIELD 2, line 284 for NTSC or line 335 for PAL. Data is encoded LSB first.
CCF1B1[7:0]	This is the first byte of closed-caption information for the FIELD 1, line 21 for NTSC or line 22 for PAL. Data is encoded LSB first.
CCF1B2[7:0]	This is the second byte of closed-caption information for the FIELD 1, line 21 for NTSC or line 22 for PAL. Data is encoded LSB first.
HSYNCF[9:0] HSYNCR[9:0]	These 10-bit values can be used to program the horizontal count for the falling and rising edges (HSYNCF and HSYNCR respectively) of HSYNC*. These values are only useful if variable HSYNC* output timing is enabled with bit ADJHSYNC. HSYNCF and HSYNCR cannot be zero and they cannot be equal. Values represent pixel counts and should be less than or equal to the total horizontal resolution shown in Table 2.
SYNCDLY	0 = Normal sync timing. 1 = Delayed sync timing.
FIELDI	0 = A “1” on FIELD indicates an FIELD 2. 1 = A “1” on FIELD indicates an FIELD 1.
SYNCDIS	0 = Normal HSYNC* operation. 1 = Disable HSYNC* edges during VBI (master mode only).
ADJHSYNC	0 = Output hsync pulse on HSYNC*. The standard hsync pulse falls at the start of a new line and remains low for 4.7 µs. 1 = Output a programmable hsync pulse on HSYNC*. By programming HSYNCR and HSYNCF, HSYNC* can rise and fall at any desired time during each line.
SETMODE	This bit is ignored in master mode. 0 = By default, in slave mode, the video mode is automatically detected. This is further explained in the SLAVE mode section. 1 = Override automatic mode-detection in slave mode. The mode will be set according to the VIDFORM[3:0], NONINTL, and SQUARE register bits.
SETUPDIS	0 = Setup on. The 7.5 IRE setup is enabled for active video lines. 1 = Setup off. The 7.5 IRE setup is disabled.

VIDFORM[3:0] Configures the device for various worldwide video formats

SETUPDIS	D5	D4	D3	D2	Format	Typical Market
0	0	0	0	0	NTSC normal	USA
1	0	0	0	0	NTSC no setup	Japan
0	0	0	1	0	NTSC-60 Hz(1)	USA–HDTV
0	1	1	0	0	PAL-M normal	Brazil
0	1	1	1	0	PAL-M–60 HZ	Brazil - HDTV
1	1	0	0	1	PAL-BDGHI	W. Europe
0	1	0	0	1	PAL-N	Uruguay, Paraguay
1	1	1	0	1	PAL-Nc	Argentina

Notes: (1). SCRESET must be “1”.

NONINTL
0 = Interlaced operation.
1 = Noninterlaced operation.

SQUARE
0 = CCIR601 operation.
1 = Square pixel operation.

ESTATUS
0 = The I^2C read-back information contains the version number.
1 = The I^2C read-back information contains closed-captioning status and field number.

RGBO
0 = Normal operation.
1 = Enable RGB outputs.

DCHROMA
0 = Normal operation.
1 = Blank chroma.

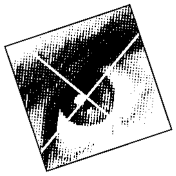
ECBAR
0 = Normal operation.
1 = Enable color bars.

SCRESET
0 = Normal operation. The subcarrier phase is reset to zero at the beginning of each color field sequence.
1 = Disable subcarrier reset event at beginning of field sequence.

EVBI
0 = Video is blanked during the vertical blanking interval.
1 = Enable active video during vertical blanking interval. Setup is added during VBI, if SETUPDIS = 0, and scaling of YCrCb pixels is always based on 100% blank to white, i.e., normal PAL input scaling.

EACTIVE
0 = Only sync information is output (only if ECBAR = 0).
1 = Enable normal video.

ECLIP
0 = Normal operation.
1 = Enable clipping; DAC values less than 31 are made 31. This limit corresponds to roughly one-fourth of the sync height.



PC BOARD CONSIDERATIONS

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

Component Placement

Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt864/865 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to the VAA power pin, protection diodes, RF modulator, VREF, VBIAS, and COMP decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog area should be separated as shown in Figure 20. This layout eliminates noise on the analog signals caused by cross-currents from digital switching.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 21. This bead should be located within 3 inches of the Bt864/865. The bead provides impedance to switching currents, which provides increased impedance at high frequencies. A low-resistance (<0.5 Ω) bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.

Figure 20. Example Power Plane Layout

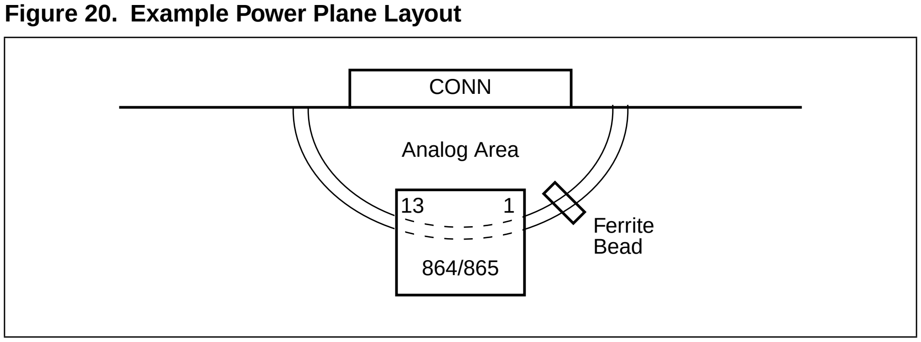
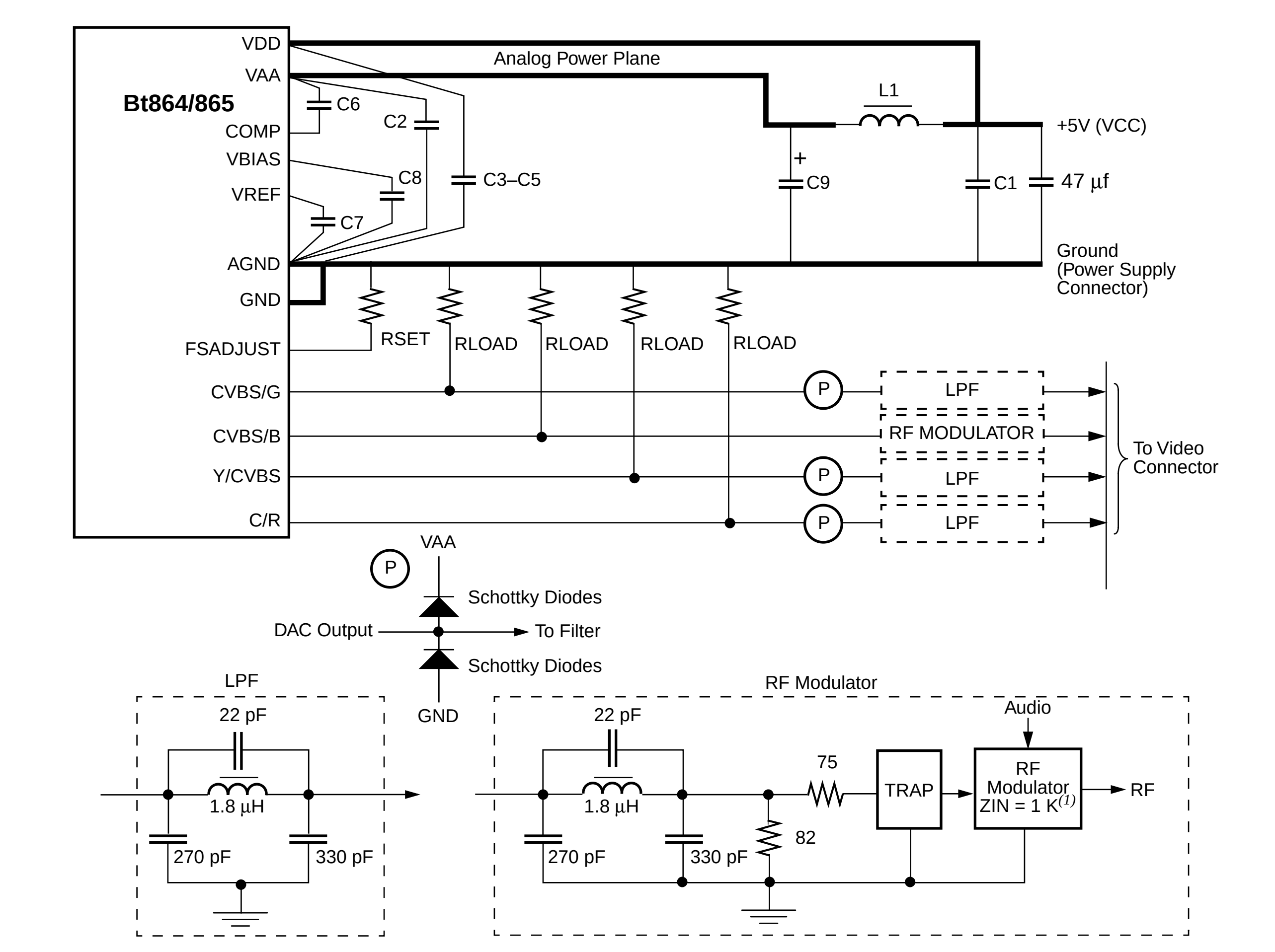


Figure 21. Typical Connection Diagram and Parts List



Notes: (1). Some modulators may require AC coupling capacitors (10 µF).

Location	Description	Vendor Part Number
C1–C8	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C9	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
RSET	1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)
RLOAD	1% Metal Film Resistor (1)	Dale CMF-55C

Notes: (1). Conductance combined with the load equals that of a 37.5 Ω resistor.
2. The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt864/865.

Decoupling

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply performance is obtained with a 0.1 μF ceramic capacitor decoupling each group of VDD pins to GND, and the VAA pin to AGND. The capacitors should be placed as close as possible to the device VAA, VDD, AGND, and GND pins and connected with short, wide traces.

The 47 μF capacitor shown in Figure 21 is for low-frequency power supply ripple; the 0.1 μF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 5% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to the VAA pin, typically with a 0.1 μF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and the VAA pin. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF Decoupling

A 0.1 μF ceramic capacitor should be used to decouple this pin to AGND.

VBIAS Decoupling

A 0.1 μF ceramic capacitor should be used to decouple this pin to AGND.

Signal Interconnect

Digital Signal Interconnect

The digital inputs to the Bt864/865 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time. Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt864/865 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and AGND should be as close as possible to the Bt864/865 to minimize reflections. Unused DAC outputs should be connected to AGND unless the power-down feature is being utilized..

Applications Information

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage. Device damage can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided; they could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA and VDD pins are at the same potential, all GND and AGND pins are at the same potential, and that the VAA and VDD supply voltages are applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

Clock and Subcarrier Stability

The color subcarrier is derived directly from the CLK input, hence any jitter or frequency deviation of CLK will be transferred directly to the color subcarrier. Jitter within the valid CLK cycle interval will result in hue noise on the color subcarrier on the order of 0.9–1.6 degrees per nanosecond. Random hue noise can result in degradation in AM/PM noise ratio (typically around 40 dB for consumer media such as Videodiscs and VCRs). Periodic or coherent hue noise can result in differential phase error (which is limited to 10 degrees by FCC cable TV standards). Any frequency deviation of the CLK from nominal will challenge the subcarrier tracking capability of the destination receiver. This may range from a few parts-per-million (ppm) for broadcast equipment to 50 ppm for industrial equipment to a few hundred ppm for consumer equipment. Greater subcarrier tracking range generally results in poorer subcarrier decoding dynamic range, so that receivers that tolerate jitter and wide subcarrier frequency deviation will introduce more noise in the decoded image. Crystal clock sources provide best stability and lowest jitter, with 50–100 ppm accuracy required by most industrial or consumer receivors. Note that a 30 ppm tolerance constraint applies for Teletext and MPEG2.

Some applications call for maintaining correct Subcarrier-Horizontal (SC-H) phasing for correct color framing, which requires subcarrier coherence within specified tolerances over a 4-field interval for 525-line systems or 8 fields for 625-line systems. Any CLK interruption (even during vertical blanking interval) which results in nonstandard pixel counts per line can result in SC-H excursions outside the NTSC limit of ±40 degrees (reference EIA RS170A) or the PAL limit of ±20 degrees (reference EBU D23-1984).

Any deviation of the number CLK cycles between HSYNC* falling edges when in SLAVE mode may result in automatic mode switching unless the internal control registers VIDFORM, NONINTL and SQUARE are set for the desired mode of operation.

Filtering RF Modulator Connection

The Bt864/865 internal upsampling filter alleviates external filtering requirements by moving significant sampling alias components above 19 MHz and reducing the sinx/x aperture loss up to the filter's passband cutoff of 5.75 MHz. While typical chrominance subcarrier decoders can handle the Bt864/865 output signals without analog filtering, the higher frequency alias products pose some EMI concerns and may create troublesome images when introduced to an RF modulator. When the video is presented to an RF modulator, it should be free of energy in the region of the aural subcarrier (4.5 MHz for NTSC, 5.5–6.5 MHz for PAL), hence some additional frequency traps may be necessary when the video signal contains fundamental or harmonic energy (as from unfiltered character generators) in that region. For example, a pixel rate of 13.5 msps is three times the NTSC-M aural carrier of 4.5 MHz, hence significant harmonic energy can fall on the FM aural carrier for character cell sizes which are multiples of three. Where better frequency response flatness is required, some peaking in the analog filter is appropriate to compensate for residual digital filter losses with sufficient margin to tolerate 10% reactive components.

A three-pole elliptic filter (1 inductor, 3 capacitors) with a 6.75 MHz passband can provide at least 45 dB attenuation (including sinx/x loss) of frequency components above 20 MHz and provide some flexibility for mild peaking or special traps. An inductor value with a self-resonant frequency above 80 MHz is chosen so that its intrinsic capacitance contributes less than 10% of the total effective circuit value. The inductor itself may induce 1% (0.1 dB) loss, and worst case subcarrier attenuation (including sinx/x loss) may be 7% with 10% tolerance reactive components. Any additional ferrites introduced for EMI control after termination should have less than 5 Ω impedance below 5 MHz to minimize additional losses. The capacitor to ground at the Bt864/865 output pin is compensated for the parasitic capacitance of the chip plus any protection diodes and lumped circuit traces (about 22 pF+5 pF/diode). Some filter peaking can be accomplished by splitting the source impedance across the reactive PI filter network. However, this will also introduce some chrominance-luminance delay distortion in the range of 10–20 ns for a maximum of 0.5 dB boost at the subcarrier frequency.

The filter network feeding an RF modulator may include the aforementioned trap, which could take two forms depending on the depth of attenuation and type of resonator device employed. The RF modulator typically has a high input impedance (about 1 KΩ ± 30%) and loose tolerance. Consequently, the amplitude variation at the modulator input will be greater, especially when the trap is properly terminated at the modulator input for maximum effect. Some modulators video or aural fidelity will degrade dramatically when overdriven, so the value of the effective termination (nominally 37.5 Ω) may need to be adjusted downward to maintain sufficient linearity (or depth of modulation margin) in the RF signal. Where required to maintain better than 40 dB audio dynamic range in the presence of video energy in the region of the aural carrier, a two section trap with more than 20 dB attenuation may be warranted. Best gain flatness versus frequency and luma-chroma delay match can be obtained by active buffering and use of the variable luma delay on CVBS/B channel. See Figure 21.

Luminance Delay on CVBS/B

Postfiltering of the video signal can introduce a variable delay between the lower frequency Luminance components and the higher frequency chrominance subcarrier components. The Group Delay distorion is often specified in system as Chroma-Luma delay inequality or as Sinx-x pulse Group Delay. Group delay distortion is commonly induced by postfilters which peak the Chrominance level, by trap circuits intended to reduce video energy in the aural subcarrier frequency range, and by Vestigial Sideband (VSB) filtering in RF tuners. Since oversampling encoders greatly reduce the need for peaking filters, delay compensation of the Luminance signal largely benefits the channel through the RF modulation and tuner path where Group delay distortion can amount to several hundred nanoseconds or several pixels of misregistration.

While flat Group Delay correction as observed from a Sinx pulse spectrum can require several LC stages with active buffers, a simplified approach where only Luma-Chroma delay must be equalized is to shift the Luminance signal through pipeline delays to match any additional Group Delay induced on the Chrominance components by postfiltering. This alignment of the lower frequency Luminance components with the Chrominance components does not strictly satisfy Broadcast quality requirements but provides perceptible improvements in display registration.

While VSB delays are prescribed in ITU-R BT.470-3 as about 170 nS, the Luminance delay compensation for postfilter aural traps depends on the attenuation required at the aural carrier frequency. In the case of NTSC signals sampled at CCIR601 resolution, the coincidence of the aural carrier (4.5 MHz) at one third of the sample rate means that any video component which transitions at intervals of everyh third pixel clock can generate significant energy at the aural carrier frequency. In the case of hard-edged, unblended characters having a font cell size which is a multiple of three pixels, harmonic energy at the aural carrier frequency may be only 15 DB below the maximum video level, or roughly equal to the power of the sound subcarrier in the RF spectrum.

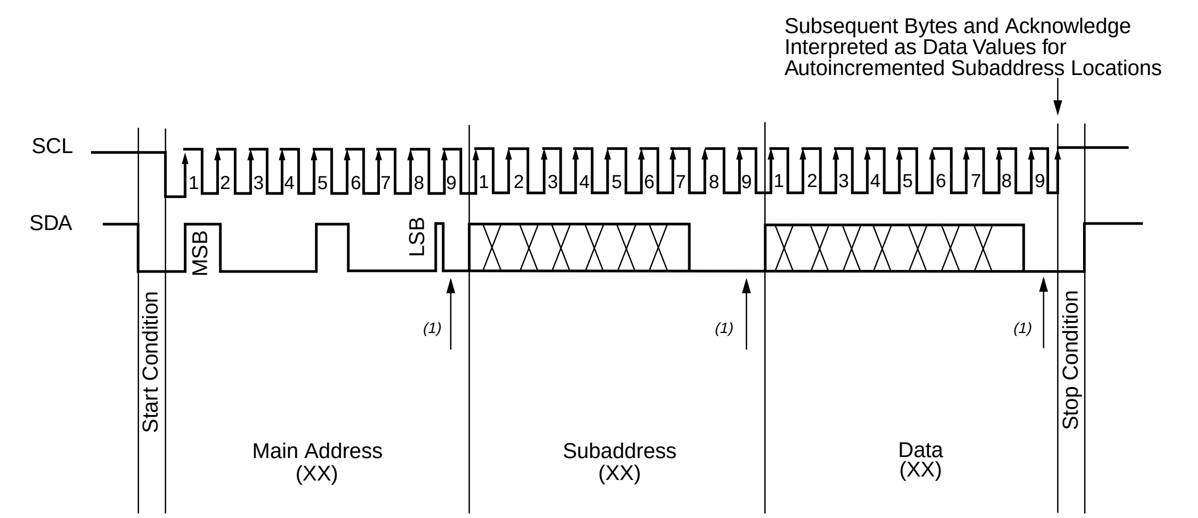
Trap attenuation of about 20 dB can assure that the resultant interference with the FM Aural signal will degrade the noise level at the monaural decoded receivor about 1 dB (–44 dB range) with less than 50 nS additional Chroma delay. [Multichannel stereo (BTSC) or Second Audio Program (SAP) encoder may require greater attenuation due to lower level subcarriers]. Therefore, Luminance delay compensation of about 225 nS on just the RF feed (e.g. CVBS/B) can correct for the Chroma delay artifacts of additional processing in the RF channel without compromising the inherently low Group Delay distortion of the baseband channels (e.g. CVBS/Y/C).

I²C Programming

Data Transfer on the I²C Bus

Figure 22 shows the relationship between SDA and SCL to be used when programming the I²C bus. If the bus is not being used, both SDA and SCL lines must be left high.

Figure 22. I²C Diagram



Notes: (1). Acknowledge generated by Bt864/865.

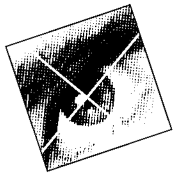
Every byte put onto the SDA line should be 8 bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes (autoincrementing the subaddress) until another stop condition is detected.

Bit 8 of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the Bt864/865, the address is only considered valid if the R/W bit is low.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the SDA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the Bt864/865 will remain in the state defined by the last complete data byte transmitted. Any master acknowledge subsequent to reading the chip ID is ignored.



PARAMETRIC INFORMATION

DC Electrical Parameters

Preliminary 3.3 V data will be supplied upon completion of characterization

Table 16. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		70	°C
DAC Output Load	RL	37.5		TBD	Ω
Nominal RSET	RSET		75		Ω

Table 17. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA and VDD (measured to GND)				7.0	V
Voltage on Any Signal Pin (1)		GND –0.5		VAA or VDD + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		Indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+125	°C
Vapor Phase Soldering (1 Minute)	TVSOL			220	°C

Notes: (1). This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.

2. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		10	10	10	Bits
Output Current-DAC Code 1023(Iout FS)			34.13		mA
Output Voltage-DAC Code 1023			1.28		V
Video Level Error (Nominal Resistors)				5	%
Output Capacitance			22		pF
Digital Inputs (Except those specified below)					
Input High Voltage	VIH	2.0		VDD + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
SCL, SDA					
Input High Voltage	VIH	0.7 x VDD		VAA + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.3 x VDD	V
CLK Input					
Input High Voltage	VIH	2.4		VDD + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			50	µA
Output Capacitance	CDOUT		10		pF

Note: "Recommended Operating Conditions," NTSC CCIR 601 operation, and CLK frequency = 27 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Electrical Parameters

Table 19. AC Characteristics *(1 of 2)*

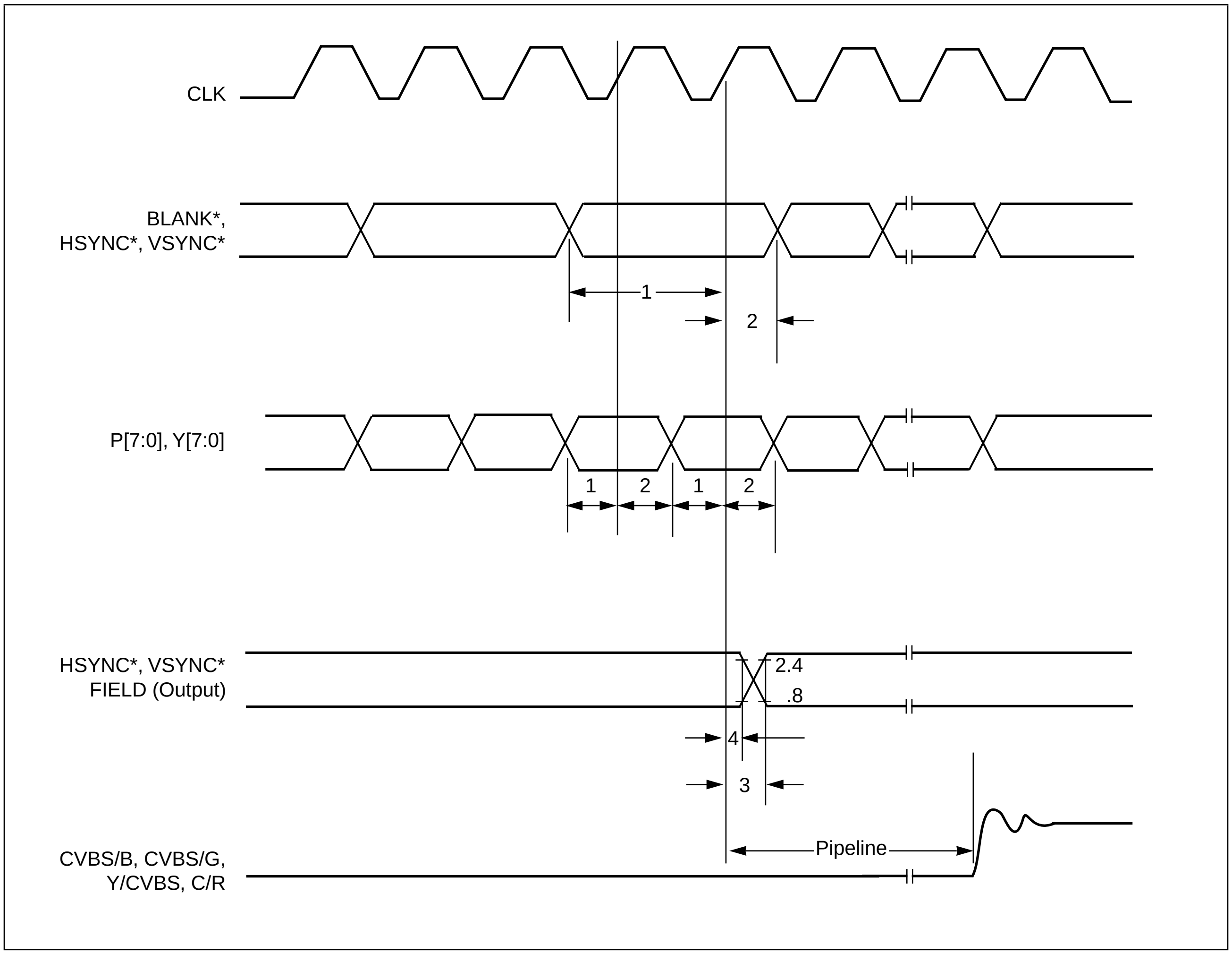
Parameter	EIA/TIA 250C Ref	CCIR 567	Symbol	Min	Typ	Max	Units
Hue Accuracy(1, 2)							± °
Color Saturation Accuracy(1, 2)							± %
Chroma AM/PM Noise(3)	1 MHz Red Field						dB rms
Differential Gain(2)	6.2.2.1	C3.4.1.3					% p–p
Differential Phase(2)	6.2.2.2	C3.4.1.4					° p–p
SNR (unweighted 100 IRE Y Ramp Tilt Correct)(2)							
RMS	6.3.1						dB rms
Peak Periodic	6.3.2						dB p–p
100 IRE Multiburst(3)	6.1.1						± IRE
Gain/frequency		C3.5.4.1					
Chroma/Luma Gain Ineq(3)	6.1.2.2	C3.5.3.1					± IRE
Chroma/Luma Delay Ineq(3)	6.1.2	C3.5.3.2					ns
Short Time Distortion 100IRE/PIXEL(3)	6.1.6	C3.5.1.4					%
Luminance Nonlinearity(2)	6.2.1						%
Chroma/Luma Intermod(2)	6.2.3						± IRE
Chroma Nonlinear Gain(2)	6.2.4.1						± IRE
Chroma Nonlinear Phase(2)	6.2.4.2						± °
Pixel/Control Setup Time(4)			1	7			ns
Pixel/Control Hold Time(4)			2	3			ns
Control Output Delay Time(4)			3			17	ns
Control Output Hold Time(4)			4	4			ns
CLK Frequency				24.54	27	29.5	MHz
CLK Pulse Width Low Time				8			ns
CLK Pulse Width High Time				8			ns
Pipeline Delay							
Input Pixels to Composite Video					52		CLK periods
Input Pixels to RGB Output					52		CLK periods

Table 19. AC Characteristics *(2 of 2)*

Parameter	EIA/TIA 250C Ref	CCIR 567	Symbol	Min	Typ	Max	Units
VAA Supply Current					180		mA
VDD Supply Current					50		mA
Total Supply Current					230		mA
Power-Down Mode Currents							
VAA Supply Current (SLEEP = 1)*(5)*					1		mA
VDD Supply Current (SLEEP = 1)*(5)*					10		mA
VAA Supply Current (DAC off =1)					1		mA
VDD Supply Current (DAC off =1)					50		mA

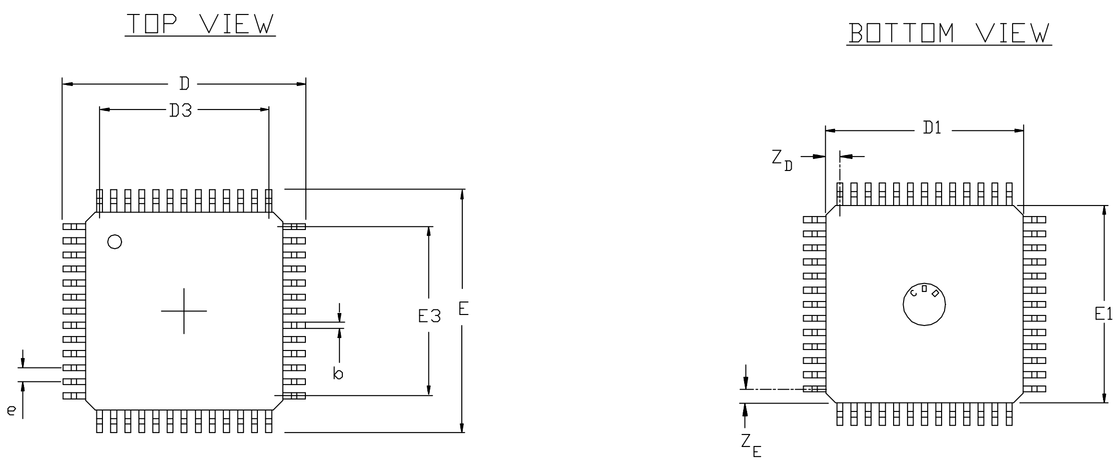
Notes: (1). 75/7.5/75/7.5 Color bars normalized to burst.
(2). Guaranteed by characterization.
(3). Without post filter. Guaranteed by design.
(4). Control pins are defined as: P[7:0], Y[7:0],BLANK*, HSYNC*, VSYNC*, FIELD, TTXREQ, TTXDAT.
(5). All digital inputs at GND or VDD.
6. "Recommended Operating Conditions," NTSC CCIR 601 operation, and CLK frequency = 27 MHz. Analog output load ≤ 75 pF. HSYNC*, VSYNC*, BLANK*, and FIELD output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. Video input and output timing is shown in Figure 23.

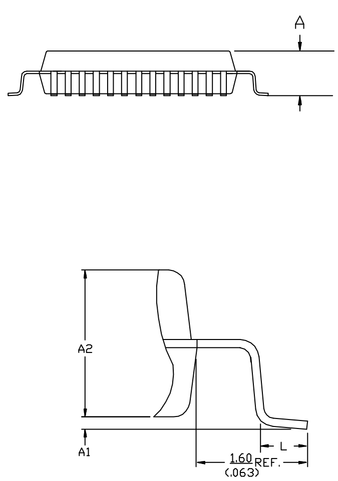
Figure 23. 8-bit YCrCb Video Input and Output Timing



Package Drawing

Figure 24. 52-Pin MQFP





SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	3.40
A_1	0.10	---	---
A_2	2.55	2.67	3.05
D	16.95	17.20	17.45
D_1	13.90	14.00	14.10
D_3	12.00 REF.		
Z_D	1.00 REF.		
E	16.95	17.20	17.45
E_1	13.90	14.00	14.10
E_3	12.00 REF.		
Z_E	1.00 REF.		
L	0.65	0.70	0.95
e	1.00 BSC.		
b	0.35	---	0.50

Revision History

Revision	Change from Previous Revision
A	New Datasheet.
B	To the Circuit Description section: added Three-Stage Chromiinance filters, Luminance 2X Upsampling Filters, and DAC Sinx/x Response, modified Video Timing Diagrams, Teletext Timing for Bt864/5 Encoder, and Video Output Waveforms.

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