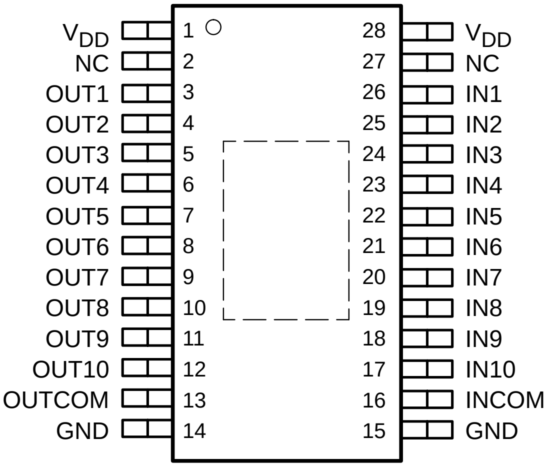
BUF11702
10+1-CHANNEL HIGH CURRENT BUFFER

SLOS359 – MARCH 2001

- **10 Channels With >10 mA Output Current**
- **1 V_{COM} Channel With >30 mA Output Current**
- **Low Power Buffer . . . I_{DD} < 5 mA**
- **Unity Gain Buffers Capable of Driving Large Capacitive Loads**
- **Input Ranges Matched to LCD Reference Requirements**
- **Specified for 0°C to 85°C . . . 4.5 V to 15 V**
- **1 pA Input Bias Current**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The BUF11702 is a 10+1-channel buffer targeted toward the needs of modern high-resolution LCD panels. These high resolution LCD panels are driven by external LCD source drivers which require a varying number of references. Due to nonideal characteristics of the LCD panels, the LCD source drivers must produce nonlinear voltages to the LCD panel. This is called gamma-correction.

Buffers 1 through 10 have output voltage drive characteristics matched to the gamma correction voltage/current requirements of these panels and are used to drive the reference inputs of the LCD source drivers. The V_{COM} channel has increased output drive capability to meet the drive requirements of the common-node of these panels.

The BUF11702 is available in the 28-pin PowerPAD™ package that enables it to meet the power handling requirements of driving these load currents at the required voltage levels.

A flow through pin out has been adopted to allow simple PCB routing and maintain the cost effectiveness of this solution.

Each buffer is capable of driving heavy capacitive loads and offers fast load current switching, often necessary when used to drive large LCDs.

PowerPAD is a trademark of Texas Instruments.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	16.5 V
Input voltage range, V_I	$\pm V_{DD}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 85°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
PWP (28)	0.72	27.9	4.3 W

[‡] See the Texas Instruments document, PowerPAD Thermally Enhanced Package Application Report (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled Texas Instruments Recommended Board for PowerPAD on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	15	V
Common-mode input voltage range, V_{ICR}[§]	Buffers 1, 2, 3, 4 & 5	1	V_{DD}	V
	Buffers 6, 7, 8, 9 & 10	0	V_{DD}–1	
	V_{COM} buffer	1	V_{DD}	
Operating free air temperature T_A		0	85	°C

[§] The common-mode input range was chosen to match the expected input/output range required for LCD reference buffers. These devices are unity-gain buffers, and as such the effective input range will ultimately be limited by the voltage swing of the outputs and what load currents are being driven.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_O = 5 V, V_I = 5 V R_S = 50 Ω		25°C		1.5	12	mV
					Full Range			15	
I_{IB}	Input bias current		V_O = 5 V, V_I = 5 V		25°C		1		pA
					Full Range		200		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V		25°C	62	80		dB
					Full Range	60			
	Load regulation	Combuffer Sinking	I_O = 1 mA to 30 mA		25°C		1		mV/mA
					Full Range				
		Combuffer Sourcing	I_O = –1 mA to –30 mA		25°C		1	1.2	
					Full Range				
		Buffers 1–10 Sinking	I_O = 1 mA to 10 mA		25°C		0.85	1	
					Full Range				
		Buffers 1–10 Sourcing	I_O = –1 mA to –10 mA		25°C		0.85	1	
					Full Range				
I_{DD}	Supply current		$V_O = V_{DD}/2$ $V_I = V_{DD}/2$	V_{DD} = 5 V	25°C		2.3	3.3	mA
					Full Range			5.5	
				V_{DD} = 10 V	25°C		2.5	3.7	
					Full Range			5.5	
	Buffer gain		V_I = 5 V		25°C		0.9995		V/V

† Full range is 0°C to 85°C.

output characteristics

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH1}	High level output voltage	Buffer1	V_I = 9.8 V,	I_O = –10 mA	25°C	9.75	9.8		V
					Full range	9.7			
$V_{OH2/3/4/5}$		Buffer2/3/4/5	V_I = 9.5 V,	I_O = –10 mA	25°C	9.45	9.5		V
					Full range	9.4			
$V_{OH6/7/8/9}$		Buffer6/7/8/9	V_I = 8 V,	I_O = –10 mA	25°C	7.95	8		V
					Full range	7.9			
V_{OH10}		Buffer10	V_I = 8 V,	I_O = –10 mA	25°C	7.95	8		V
					Full range	7.9			
V_{OHCOM}		ComBuffer	V_I = 8 V,	I_O = –30 mA	25°C	7.95	8		V
					Full range	7.9			
V_{OL1}	Low level output voltage	Buffer1	V_I = 2 V,	I_O = 10 mA	25°C		2	2.05	V
					Full range			2.1	
$V_{OL2/3/4/5}$		Buffer2/3/4/5	V_I = 2 V,	I_O = 10 mA	25°C		2	2.05	V
					Full range			2.1	
$V_{OL6/7/8/9}$		Buffer6/7/8/9	V_I = 0.5 V,	I_O = 10 mA	25°C		0.5	0.55	V
					Full range			0.6	
V_{OL10}		Buffer10	V_I = 0.2 V,	I_O = 10 mA	25°C		0.2	0.25	V
					Full range			0.3	
V_{OLCOM}		ComBuffer	V_I = 2 V,	I_O = 30 mA	25°C		2	2.05	V
					Full range			2.1	

† Full range is 0°C to 85°C.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted) (continued)

ac characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB Bandwidth	Buffers 1–10	C_L = 100 pF,	R_L= 2 kΩ		1.2		MHz
		Com buffer				0.6		
SR	Slew rate	Buffers 1–10	C_L = 100 pF, V_{IN} = 2 V to 8 V	R_L= 2 kΩ,		1		V/µs
		Com buffer				0.7		
	Transient load regulation disturbance		I_O = 0 to ±5 mA, C_L = 100 pF	V_O = 5 V,		900		mV
$t_{sl\text{-}sink}$	Settling time – current		I_O = 0 to –5 mA, C_L = 100 pF	V_O = 5 V, 0.1%		1		µs
$t_{sl\text{-}source}$	Settling time – current		I_O = 0 to 5 mA, C_L = 100 pF	V_O = 5 V, 0.1%		2		µs
t_s	Settling time – voltage	Buffers 1–10	V_I = 4.5 V to 5.5 V	0.1%		6		µs
			V_I = 5.5 V to 4.5 V	0.1%		4.6		
		Com buffer	V_I = 4.5 V to 5.5 V	0.1%		5.8		
			V_I = 5.5 V to 4.5 V	0.1%		5.6		
V_n	Noise voltage	Buffers 1–10	V_I = 5 V, f = 1 kHz			45		nV/√Hz
		Com buffer				40		
	Crosstalk					85		dB

APPLICATION INFORMATION

The BUF11702 was designed to buffer the gamma correction reference voltages supplied to the digital-to-analog converters (DACs) within the LCD source drivers and provide the voltage/current requirements for LCD panel common node (Vcom). See Figure 1.

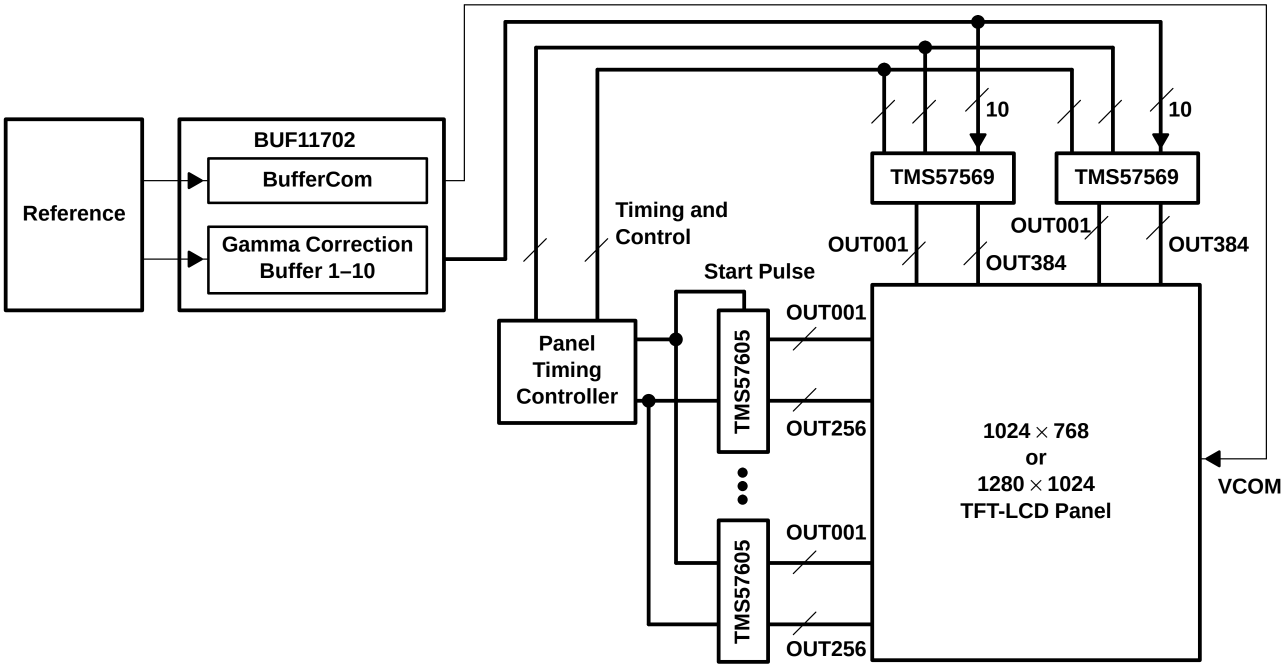


Figure 1. LCD Panel Drive Block Diagram

Depending on the size of the display, the BUF11702 will have to drive the gamma correction voltage inputs of a different number of LCD source drivers. A typical LCD source driver available from TI is the TMS57569.

A 64 gray scale LCD source driver employs internal DACs to convert a 6 bit digital word into a corresponding analog voltage. A 64 gray scale LCD source driver typically has 10 reference nodes to allow for external gamma voltage correction. Gamma voltage correction is used to match the characteristic of the LCD source driver chip as close as possible to the characteristic of the actual LCD panel to improve the overall picture quality. External gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 2. The BUF11702 acts as a buffer for the various nodes on the gamma correction resistor ladder. Due to the low output impedance of the BUF11702 it forces the external gamma correction voltage on the respective reference node of the LCD source driver providing an accurate match between the source driver and the LCD panel.

APPLICATION INFORMATION

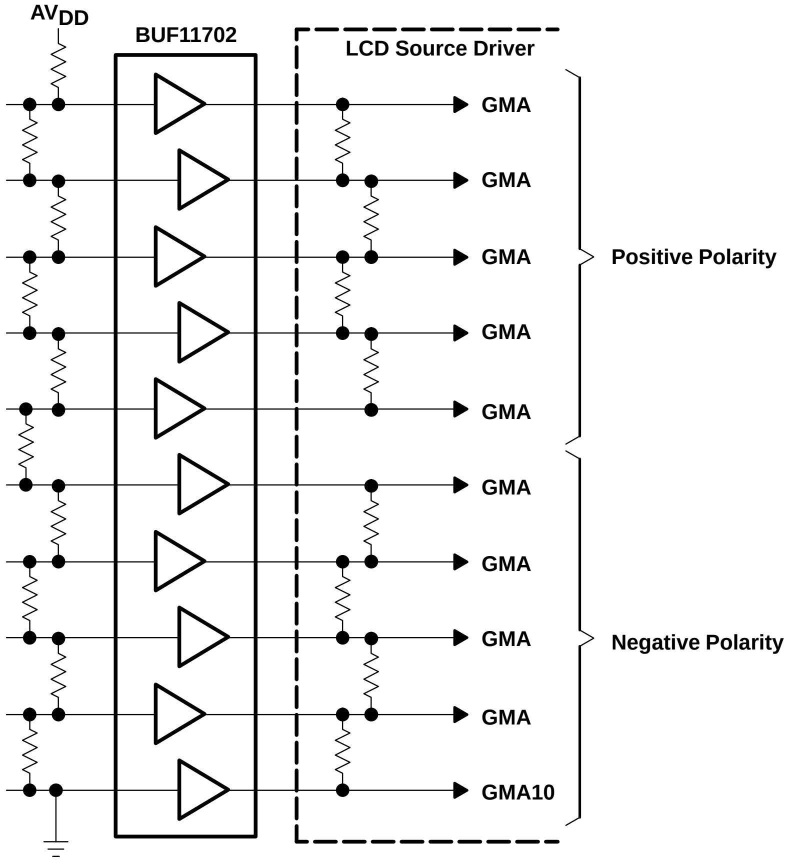


Figure 2. Reference Buffer for LCD Source Driver

APPLICATION INFORMATION

gamma correction

Figure 3 shows a typical 10-reference voltage gamma correction curve. As can be seen from this curve the various voltages that each buffer encounters vary greatly.

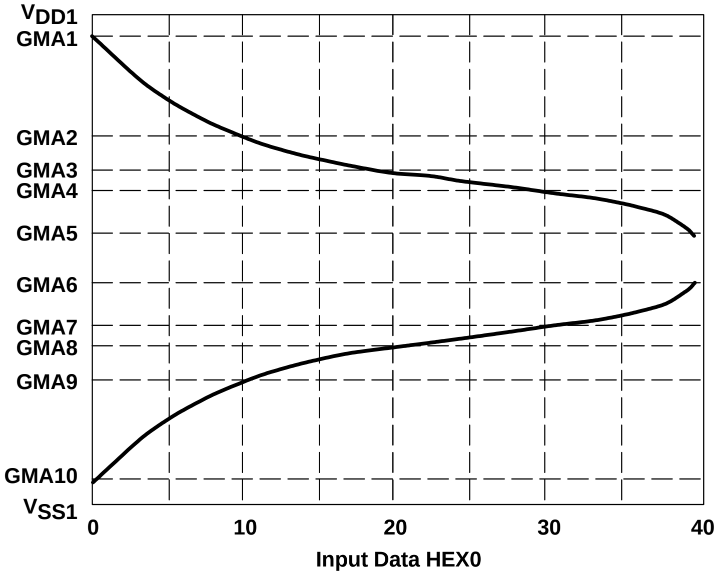


Figure 3. Gamma Correction Curve

The LCD source driver DAC uses the reference voltages and internal resistor ladder to produce individual voltages for each input code.

For gamma correction voltages GMA1 through GMA5, the voltage levels would be between $V_{DD1}/2$ and V_{DD1}, and for GMA6 through GMA10, the voltage levels would be between GND and $V_{DD1}/2$. That means that buffers 1 to 5 must have input stages that swing close to the positive rail, but will not have to swing very close to ground (or the negative rail). Therefore buffers 1 through 5 have only a single NMOS input pair. Buffers 6 to 10 have similar but opposite requirements in that they must have input ranges that go down to ground (or negative rail), enabling them to have only a PMOS input pair.

The output stages have been designed to match the characteristic of the input stage. That means that the output stage of buffer 1 swings very close to the positive range, whereas its ability to swing to GND (or negative rail) is limited. Buffers 2 to 5 have output stages with slightly larger output resistances, as they will not have to swing as close to the positive rail as buffer 1. The converse is true for buffers 6 to 10 in the sense that they have to swing closer to ground than the positive rail.

This approach significantly reduces the silicon area and cost of the whole solution. However due to this architecture the right buffer needs to be connected to the right gamma correction voltage. Connect buffer 1 to the gamma voltage closest to the positive rail, buffers 2 to 5 to the following voltages. Buffer 10 should be connected to the gamma correction voltage closest to GND (or the negative rail), buffers 9 through 6 to the following voltages.

When the LCD source driver has its gamma correction curves matched to the LCD panel, not all 10 reference inputs will be required; quite often only 4 might be used. The quad channel BUF4701 is an ideal device for these applications; it combines high drive with wide bandwidth in a 10-pin MSOP.

APPLICATION INFORMATION

driving LCD source drivers with >64 grey scale

When a greater number of gray scales are required, two or more BUF11702 devices can be used in parallel, see Figure 4. This might introduce some redundancy, but still provides a cost-effective way of producing more reference voltages over the use of quad op amps.

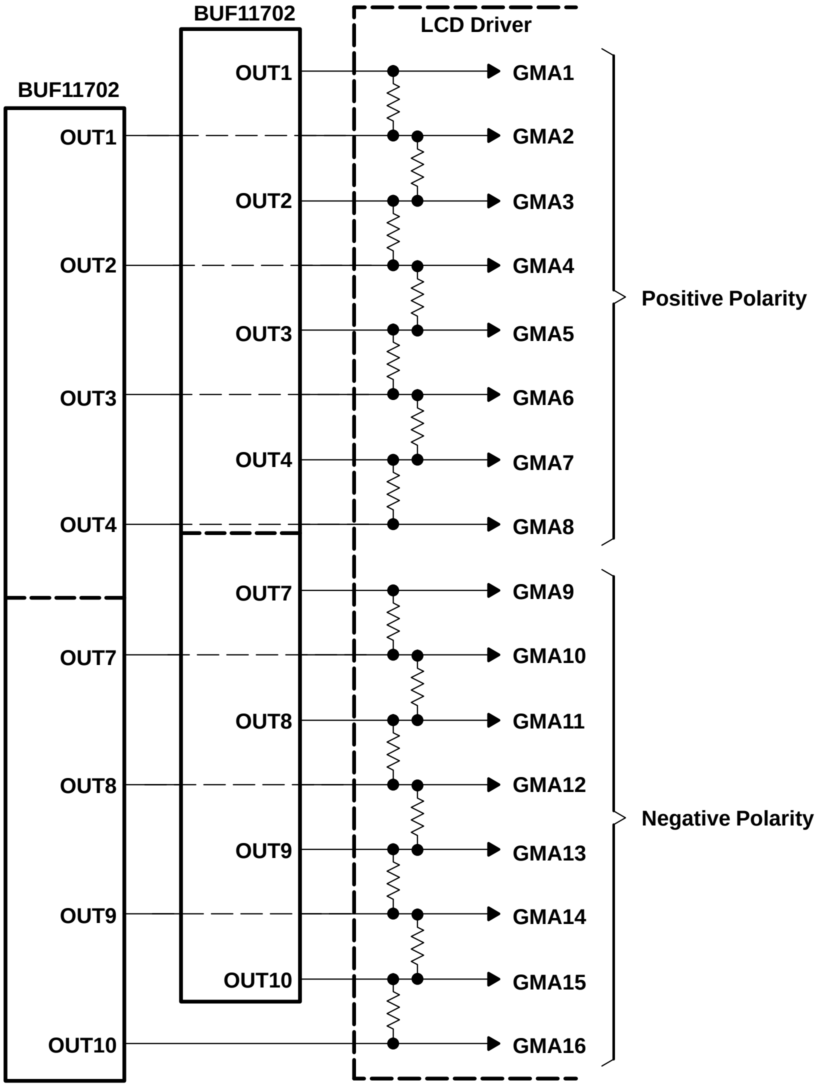


Figure 4. Two BUF11702 Driving a 16-Reference LCD Source Driver

An 8-bit source driver typically has 16 to 18 input pins for external gamma correction voltages. Using two BUF11702 ICs, a total of 20 gamma correction voltages can be provided to the respective LCD source driver. Despite the possible redundancy, the overall cost of two BUF11702s is very competitive.

APPLICATION INFORMATION

transient load regulation

The BUF11702 has been designed to be able to sink/source dc currents in excess of 10 mA. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However there are times when very fast current pulses are required. Therefore, in LCD source driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These are to improve the transient load regulation. These will typically vary from 100 pF and more. The BUF11702 buffers were designed to drive capacitances in excess of 100 pF and retain effective phase margins above 50°, see Figure 5.

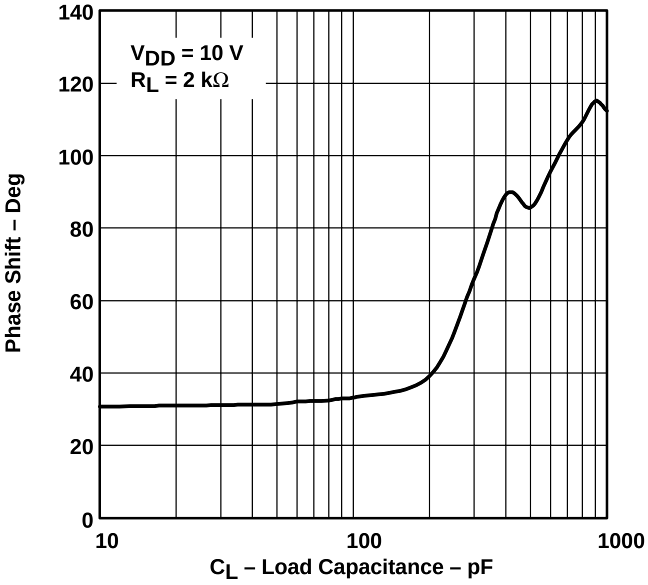


Figure 5. Phase Shift Between Output and Input vs Load Capacitance for Buffers 1–10

APPLICATION INFORMATION

transient load regulation (continued)

As with all closed-loop amplifiers, if the capacitive load becomes too large, then the phase margin will be reduced, introducing excessive ringing and overshoot. One way of overcoming this is to place series nulling resistors between the output and these load capacitors, see Figure 6.

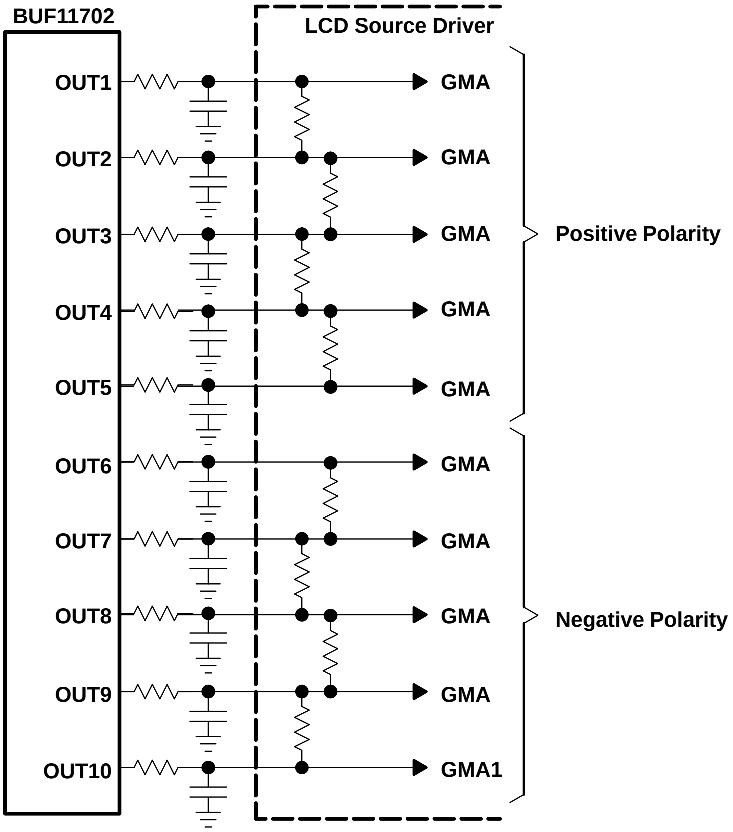


Figure 6. BUF11702 Driving a LCD Source Driver With Series Nulling Resistors

APPLICATION INFORMATION

common buffer

The common buffer output of the BUF11702 has a greater output drive capability than buffers 1–10, to meet the heavier current demands of driving the common node of the LCD panel. It was also designed to drive heavier capacitive loads and still remain stable, see Figure 7.

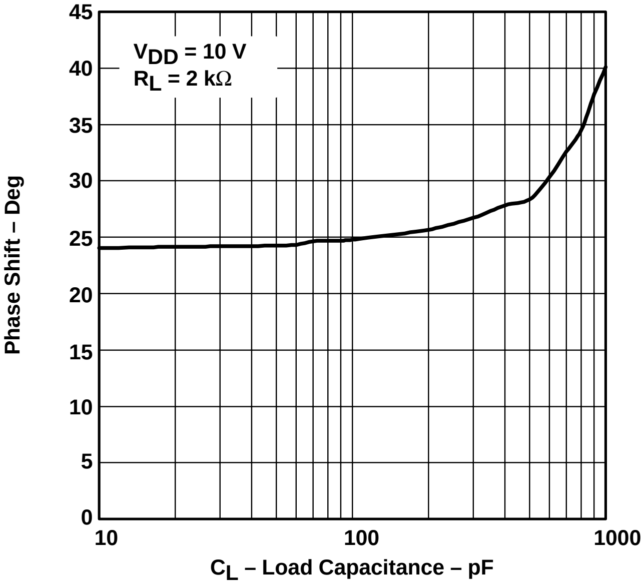


Figure 7. Phase Shift Between Output and Input vs Load Capacitance for Common Buffer

Because the common node of the panel acts like a large capacitor, the common output of the BUF11702 will have to supply very large pulses of current. In some applications the output drive capability of the BUF11702 might not be sufficient. Therefore discrete amplifiers with high output current drive capability and enough phase margin to drive large capacitive loads could be used.

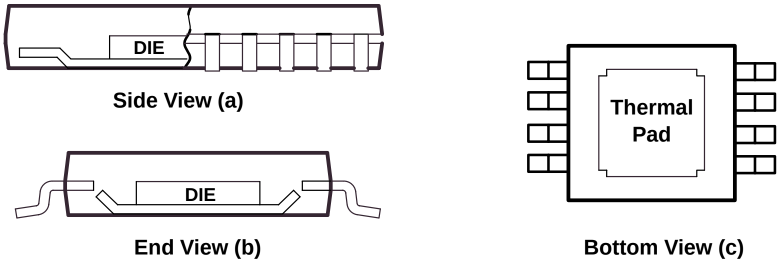
Possible alternatives include the OPA551, OPA350, BUF634, TLC081 or TLV4110/1. Because of their wide bandwidth and the low frequency pole created by the LCD panel common node capacitance, extra compensation may be required.

APPLICATION INFORMATION

general PowerPAD design considerations

The BUF11702 is available in the thermally enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 8(a) and Figure 8(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 8(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 8. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

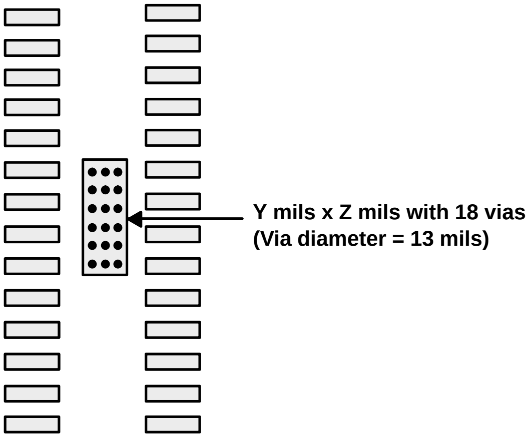


Figure 9. PowerPAD PCB Etch and Via Pattern

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 9. There should be etching for the leads as well as etch for the thermal pad.
2. Place eighteen holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF11702 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF11702 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The topside solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF11702 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

For a given θ_{JA}, the maximum power dissipation is shown in Figure 10 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of BUF11702 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (0.72°C/W)
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

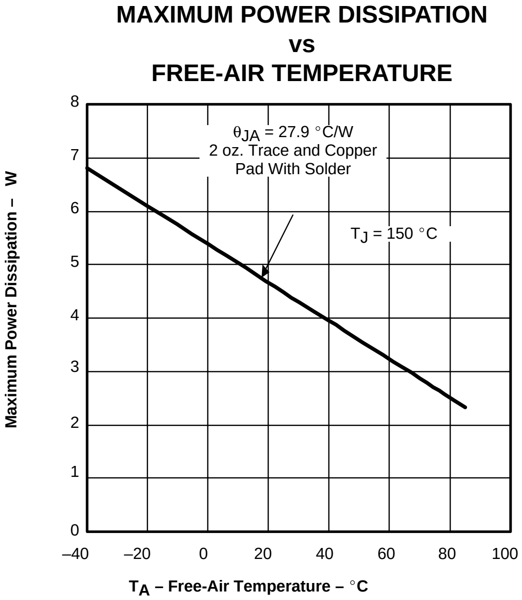


Figure 10. Maximum Power Dissipation vs Free-Air Temperature

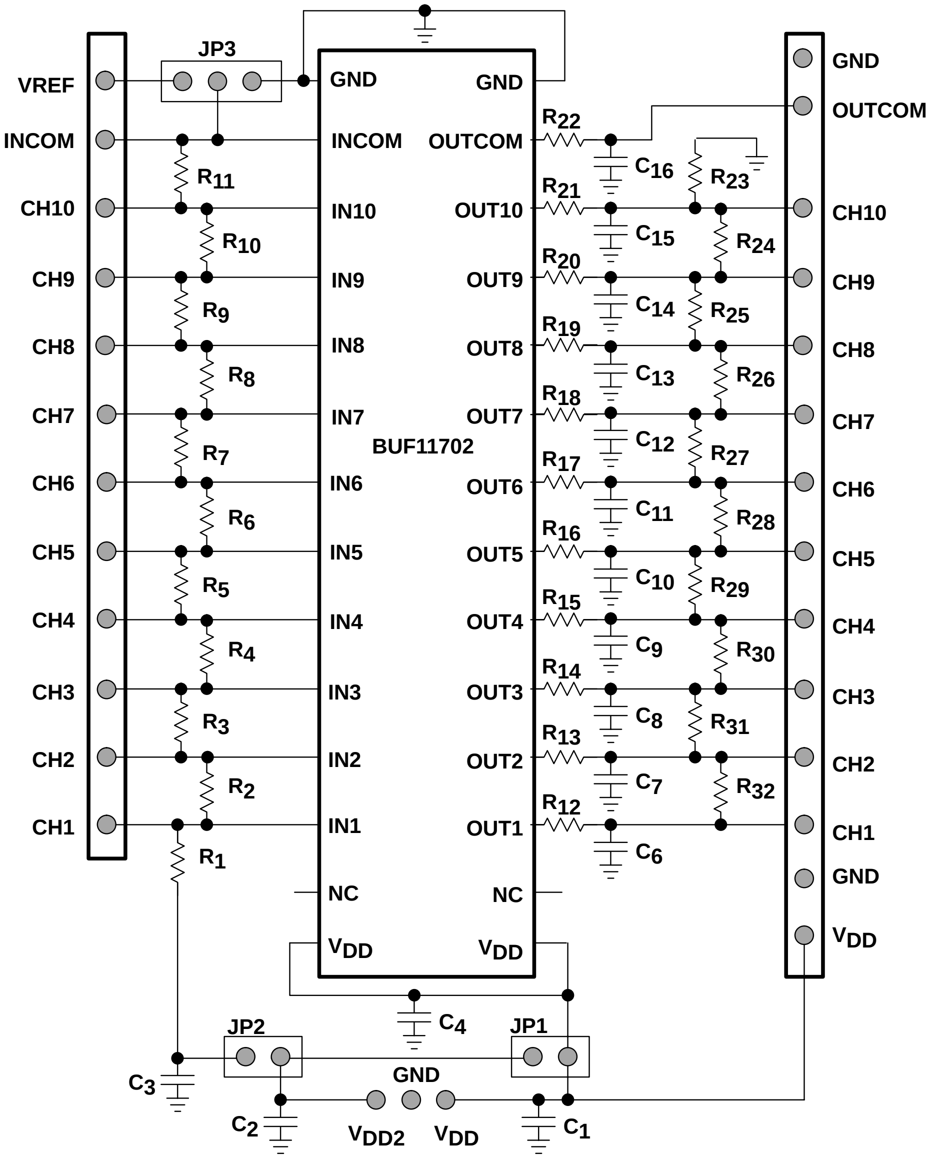
This lower thermal resistance enables the BUF11702 to deliver maximum output currents even at high ambient temperatures.

APPLICATION INFORMATION

BUF11702 evaluation module (SLOP356)

The BUF11702 has an evaluation module where it can be mounted along with reference resistors and load capacitors. This enables the BUF11702 to be used in its own daughterboard in existing designs for easy evaluation. The schematic of the BUF11702 EVM is shown below.

Note that the EVM has been configured for single supply use. As such, all decoupling capacitors are connected to the ground plane of the EVM, as are the ground terminals of the BUF11702.



In populated versions of the EVM capacitors C_1 to C_4 have been included. Capacitors C1 and C2 are bulk decoupling capacitors of 6.8 µF while capacitors C_3 and C_4 are 100 nF ceramic high frequency decoupling capacitors. Resistors R_1 to R_{32} and capacitors C_5 to C_{16} have not been included, as these are application specific.

APPLICATION INFORMATION

reference voltages

The reference voltages can be supplied externally via the connector J2 (not included) or generated onboard via resistors R_1 to R_{11}. Provision on the board for an external low side reference has been included so that the negative references can be referred to a voltage other than ground.

The reference ladder can be referred to either V_{DD} (master supply voltage) or a secondary voltage, V_{DD2}. This allows a low noise or absolute reference voltage to be used for the LCD source driver's DACs other than the system voltage. If the secondary voltage is used, then jumper JP1 should be left open and jumper JP2 shorted. If a ratiometric reference (proportional to the master supply voltage) is to be used, then jumper JP1 and JP2 should be shorted, feeding V_{DD} through to the reference ladder.

output

The outputs of the BUF11702 are fed to connector J3 (not mounted). This enables the output voltages to be monitored directly on the EVM or fed off-board for evaluation in a real system.

Onboard load resistors, R_{23} to R_{32}, connected to ground can also be mounted. These can be used to simulate resistive loading of the LCD source driver.

Transient improving capacitors are frequently used in LCD panel applications, and so pads to mount these transient improving capacitors, C_6 to C_{16}, have been included. Due to the possible magnitude of these capacitors, pads have been placed between the output of the BUF11702 and these capacitors to mount nulling resistors, R12 to R22. If the nulling resistors are not required, shorts could be placed instead of resistors.

The pads for R1 to R32 and capacitors C3 to C16 have been laid out to support 0805 or 1206 size components.

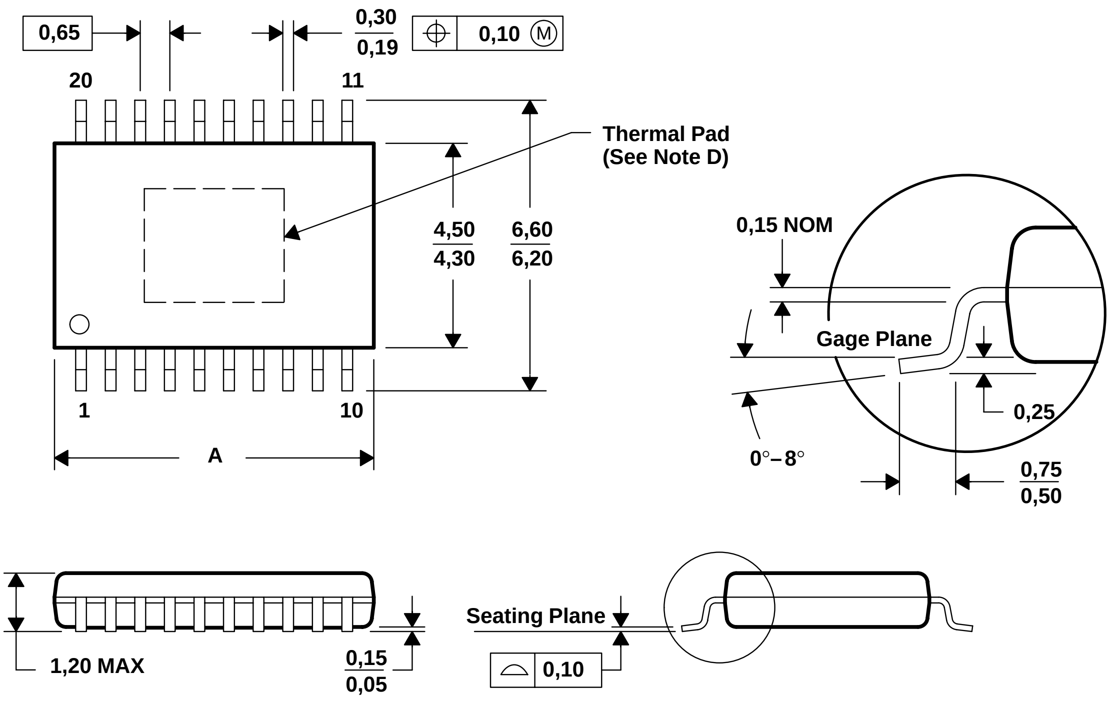
PowerPAD

The EVM has been laid out to support the PowerPAD feature of the BUF11702. An area is provided on the EVM, under the BUF11702, for the exposed leadframe to be connected to. Eighteen vias are connected to the ground plane of the EVM to reduce the thermal case to ambient resistance, θ_{CA}, significantly. See applications section on general PowerPAD design considerations.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2001, Texas Instruments Incorporated