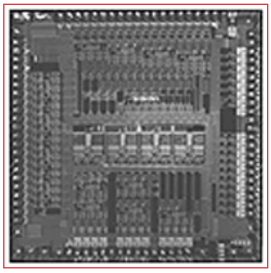
BROADCOM®

BCM4500 PRODUCT Brief



ADVANCED MODULATION SATELLITE RECEIVER

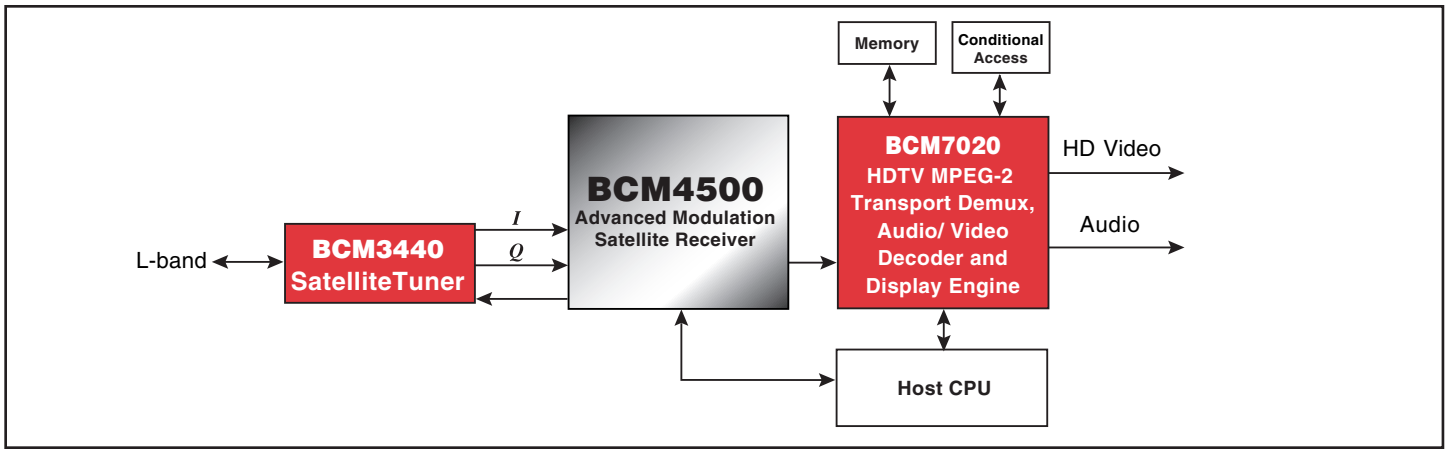
BCM4500 FEATURES

- **All-digital satellite receiver**
  - 1-30 MBaud variable rate receiver
  - Supports BPSK, QPSK, 8PSK, & 16QAM modulation
  - Dual integrated 7-bit A/D converters
  - Digital square-root Nyquist filters (α=0.2, 0.25, 0.35)
  - All-digital clock and carrier recovery
  - 12-tap adaptive equalizer
- **Advanced modulation turbo FEC decoder**
  - High performance code approaches constrained capacity theoretical limits
  - Supports QPSK rate 1/2
  - Supports 8PSK rates 1/2, 2/3, 3/4, 5/6, and 8/9
  - Supports 16QAM rate 3/4
  - Programmable convolutional deinterleaver with internal RAM
  - Reed-Solomon decoder; t=10
- **DVB/DIRECTV®/Digicipher II™-compliant FEC decoder**
- **MPEG-2 or DIRECTV output interface with output clock PLL**
- **On-chip microcontroller for acquisition and tracking**
- **On-chip BERT for BER testing**
- **Integrated DiSEqC™ (v2.0) transmitter and receiver**
- **128-pin PQFP**
- **3.3V I/O and analog operation**
- **1.8V digital operation**

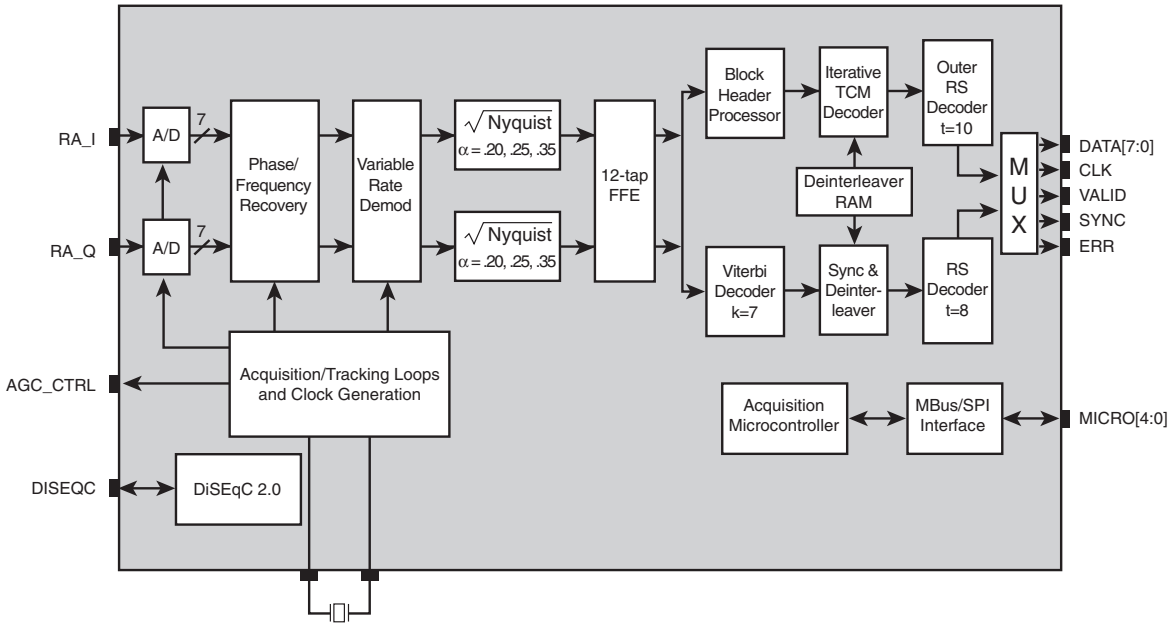
SUMMARY OF BENEFITS

- **Highly integrated solution provides universal front-end for advanced modulation satellite systems and legacy QPSK systems in a single package.**
- **High-performance turbo code FEC enables 50% throughput increase over existing satellite channels within current link budgets, enabling 2 HD channels within a single transponder.**
- **Advanced design architecture requires no external RAM for turbo FEC.**
- **Advanced modulation receiver provides robust performance for 8PSK operation at QPSK energy levels.**
- **Full variable rate operation from 1–30 Mbaud provides multiple operating point for optimal system deployment.**
- **Integrated microcontroller controls receiver operations including configuration, acquisition and performance monitoring.**
- **Host interface operates via high-level application programmers interface to reduce host software development time and to simplify system integration.**
- **MPEG-2 or DIRECTV output interface with PLL-generated data clock provides glueless integration with BCM7020 HD graphics and video subsystem.**
- **Highly integrated DiSEqC™ interface includes integrated analog components.**

Advanced Modulation Satellite Receiver Set-Top Box



Functional Block Diagram



The **BCM4500** brings a new level of performance to the satellite industry with the introduction of an integrated advanced modulation receiver and turbo decoder FEC. This breakthrough design provides 50% more throughput in the same satellite channel at standard QPSK operating points while simultaneously improving BER performance beyond existing levels. A high performance turbo code FEC is implemented with all required on-chip RAM to move system operating points near the theoretical capacity limits. A Reed-Solomon outer code is also used to drive BER beyond typical satellite 10E-11 limits.

The **BCM4500** is a single-chip digital satellite receiver supporting BPSK, QPSK, 8PSK and 16QAM modulations with iteratively (turbo) decoded error correction coding. It represents an industry milestone in terms of satellite system throughput and operating points. The **BCM4500** also receives DVB, DIRECTV and Digiciper II (DCII), QPSK signals to support legacy system operation.

The **BCM4500** contains dual 7-bit A/D converters, an all-digital variable rate BPSK/QPSK/8PSK/16QAM receiver, an advanced modulation turbo FEC decoder and a DVB/DIRECTV / DCII compliant FEC decoder. All required RAM is integrated and all required clocks are generated on-chip from a single reference crystal. Baseband I/Q analog waveforms are sampled by the integrated 7-bit A/D converters, resampled by integrated interpolative digital filter banks, and filtered by dual square-root Nyquist filters. Optimized soft decisions are then fed into either a DVB/DIRECTV/DCII-compliant FEC decoder, or an advanced modulation turbo decoder. The final error-corrected output is delivered in MPEG-2 or DIRECTV transport format. The output clock is generated by an on-chip PLL for low-jitter operation and glueless integration with Broadcom's BCM7020 HD graphics and video subsystem.

The **BCM4500** also features a simplified user interface employing an on-chip microcontroller for all system configuration, acquisition, control and monitoring functions. The host interface to the device is via a simplified, high-level application programmer interface (API). The chip also contains an integrated DiSEqC 2.0 controller with integrated voltage regulator for two-way communication with LNBs. An on-chip BERT is provided to simplify system test and manufacturing.

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