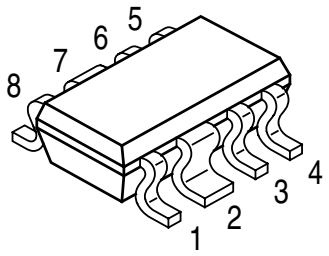
A 1.85 GHz Low Noise Self-Biased Transistor Amplifier using BGC420

Features



- **Gain=16dB / NF=1.65dB**
- **Small SCT598-Package**
- **Integrated Active Bias Circuit**
- **Control Pin for Power-Down Mode**
- **Current Easily Adjusted with an External Resistor**
- **Device Current Independent of Supply Voltage (2V – 5V)**

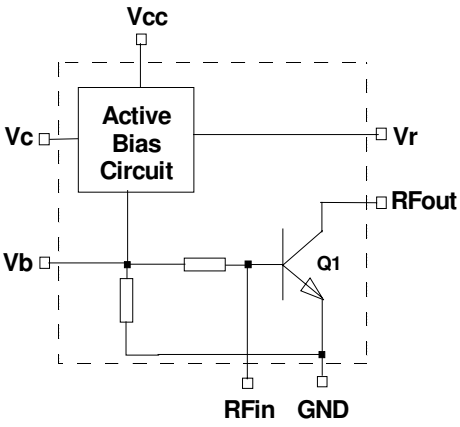
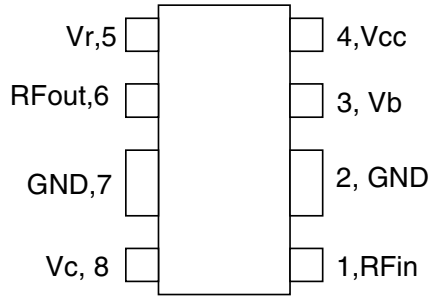


Figure 1. Simplified Equivalent Circuit



Note: Top View

Figure 2. Pin Connections, SCT598

Description

The Infineon BGC420 is a silicon self biased RF Transistor Amplifier that offers excellent gain and noise figure for applications up to 2.5 GHz. The BGC420 is a unique RFIC that combines the performance flexibility of a discrete transistor with the simplicity of using an integrated circuit. It offers an adjustable collector current nearly independent from device voltage in the range of 2.0V to 5.0V. In addition a control pin (Vc) for switching the device off is provided. The collector current can be adjusted by connecting a resistor between Vcc and Vr.

General Information

The BGC420 is developed for use in battery powered equipment demanding high performance with low supply voltages and minimal current drain. Typical applications for the device include low noise RF amplifiers, IF amplifiers, gain and buffer stages up to 2.5 GHz. The BGC420 is an excellent choice for use in cellular and cordless telephones, PCS, W/LAN's, RF modems and other commercial wireless equipment.

Infineon BGC420 is fabricated using SIEGET®25 Technology. SIEGET-25 stands for SIEMENS grounded emitter transistors with a transition frequency of 25 GHz and denotes a technology designed for high frequencies and low quiescent currents.

The Device combines the silicon RF transistor BFP420 and a bias regulation circuit. The active bias circuit solves three problems usually encountered with traditional techniques for biasing discrete transistors:

1. As an active bias circuit, the emitter of the RF transistor is dc grounded. This permits the collector current to be controlled without the need for resistors and bypass capacitors in the emitter that may degrade RF performance.

2. The internal bias circuit greatly simplifies the design tasks commonly associated with biasing transistors, such as accurately regulating the collector current, allowing for variation in h_{FE}, making a non-intrusive DC connection to the base of the transistor, and stabilising current over supply voltage.

3. The integrated circuit greatly reduce the parts count, cost and associated PCB area.

Design Steps

For an LNA design, first we need to choose the bias point of the RF transistor, and then match the device input and output for the desired frequency to source and load. The bias conditions are chosen at this step in the design sequence since many of the RF design characteristics e. g. S-parameters and noise parameters are dependent on current and/or voltage.

The bias voltage is often simple as it is normally limited by available system recourses, such as battery voltage or system power supply. The BGC420 will operate from 2 to 5 volts, with 3 volts considered to be the typical operating voltage. Although noise figure and gain are somewhat insensitive to device voltage as an independent variable, some increase in output power can be realised with higher device voltage .

The bias current has the greatest effect on RF performance and the following trade-offs should be considered:

- Noise Figure depends on the device current. The noise data in the S-parameter files of the BGC420 shows an increase in F_{min} of from 0.86dB at 4mA (900 MHz) of bias current to 1.16 dB at 10mA (900 MHz).

- Gain and output power increases significantly in proportion to device current.

Setting the Bias Current

The integrated bias control circuit is very easy to use. The collector current of the RF transistor (Q_1) can be set with a single resistor. Usually the collector of the RF transistor (Q_1)is connected to Vr by an inductor. The RF is

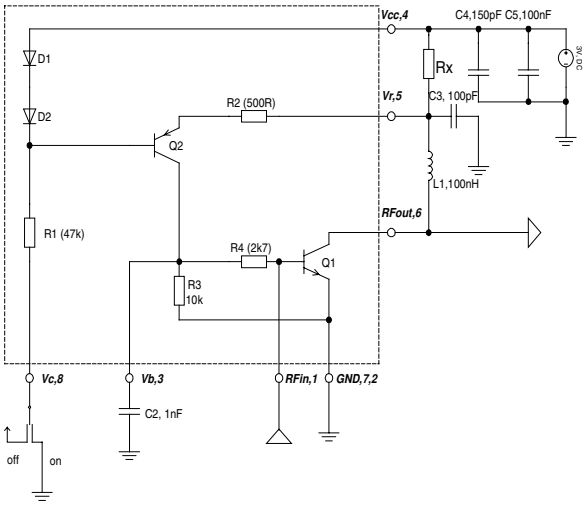


Figure 3. Typical Application and Internal Circuit

blocked by L_1 and decoupled with C_3 . The RF must be cancelled at the Vr pin. L_1 can also be used for output matching. The voltage drop between Vcc and Vr is regulated by the active bias circuit to approximately 0.6 V (nearly independent from voltage). Therefore the collector current can determined with the following equation:

$$R_X \cong \frac{0.6\,V}{I_C}$$

(The emitter current of Q2 is a fraction of the collector current and can be neglected). For example, for a desired collector current of 7 mA and a power supply of 3 volts, the value of R_x would be ≅ 86 Ω.

C_2 and C_3 help prevent the active bias circuit from oscillating at low frequency. C_3 should be at least 100 pF and C_2 ten times C_3. C_2 has to be placed as close as possible to the device.

Match the Device

The input impedance match is generally designed to achieve either of two goals, either lowest noise figure or maximum power transfer. The maximum power transfer match provides maximum gain and corresponds to minimum VWSR. In some cases, like LNA design, noise circles in combination with constant gain circles are used to design an intermediate match point to achieve a compromise in performance between low noise figure and low input VWSR.

To obtain lowest noise figure, the input of the BGC420 is matched to the Γ_{opt} . Γ_{opt} is the reflection coefficient of the source termination that results in F_{min}, the lowest possible device noise figure. Γ_{opt} design data are found at the end in the S-parameter files of the BGC420.

Otherwise if the design goal is to obtain maximum power transfer and minimum input VWSR, then the input of the BGC420 is matched to Γ_{MS} and the output to Γ_{ML}. Γ_{MS} and Γ_{ML} are the source and load impedance resulting from the simultaneous conjugate match of the input and output of the device. This is only possible if the device is unconditionally stable, if necessary the device has first to be stabilised. After the stabilisation of the device the required reflection coefficient (Γ_{MS} , Γ_{ML}) for maximum gain can be calculated.

There are several techniques to stabilise a unstable device. In keeping with the goals of low cost and circuit simplicity, the resistive loading method is the technique suggested for producing an unconditionally stable amplifier for most applications of the BGC420.

The resistive loading can be applied in either series or shunt and can be added to either the input or output of the amplifier. The choice of series or shunt resistive load may dictated by whether the real part of the output impedance of the amplifier device is greater or less than 50 Ω. The logical choice is to use a shunt resistor when the amplifier impedance is greater then 50 Ω and a series resistor for the case of less then 50 Ω impedance, thus simplifying the match.

In some cases, excessive voltage drop across the stabilising resistor due to the DC current into the device may preclude the use of the series configuration.
Shunt resistance is usually the straightforward solution to implement, since it can easily bypassed to ground with a capacitor without disturbing the bias.

For gain or buffer stages requiring maximum output power, the loading is applied to the amplifier input. If the performance goal is low noise figure, the resistive loading is implemented on the output side of the BGC420 Figure 4, 5 and 6 shows three possibilities for resistive loading with minimal part count.

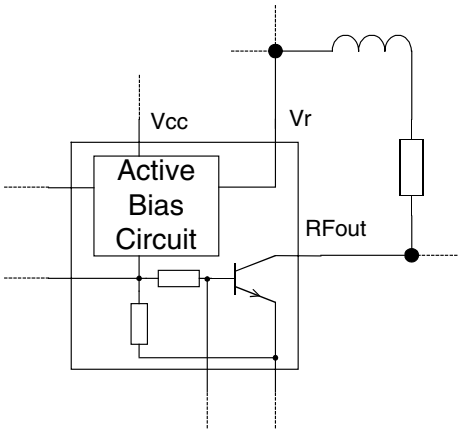


Figure 4. Shunt resistive loading I

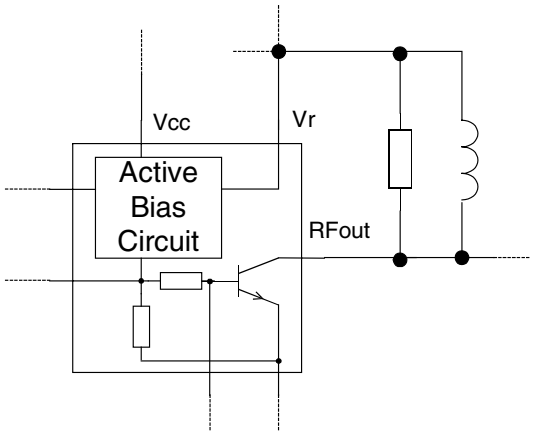


Figure 5. Shunt resistive loading II

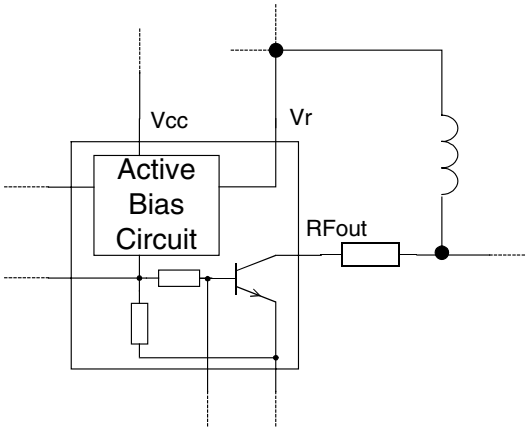


Figure 6. Series resistive loading

1850 MHz LNA Design Example

Figure 7 shows an example for a low noise amplifier stage for 1850 MHz using BGC420. The amplifier is designed for many low cost, battery powered receiver applications such as LNAs for cellular telephones like **GSM 1800**. The target was an amplifier with gain > 16 dB, NF < 1.8 dB, Rlin / Rlout > 10 dB, OIP3 > 10 dBm, unconditional stability and low board space.

In this example the device current is set to 7 mA, which yields a value of 82 Ω for R_2 (0.6 V / 7 mA ≅ 82 Ω). C_6 and R_3 are optional for measurement purpose. The device may be placed in and out of standby mode using J_2. C_1, L_1 are for the input and L_2 for the output matching. C_1 works also as DC-blocker. C_3 is a coupling capacitor. R_1 in combination with L_2 stabilise the device at lower frequencies. Table 1 shows the measured parameter values. These values includes the losses of the SMA connectors and microstrip lines of the FR4 epoxy board.

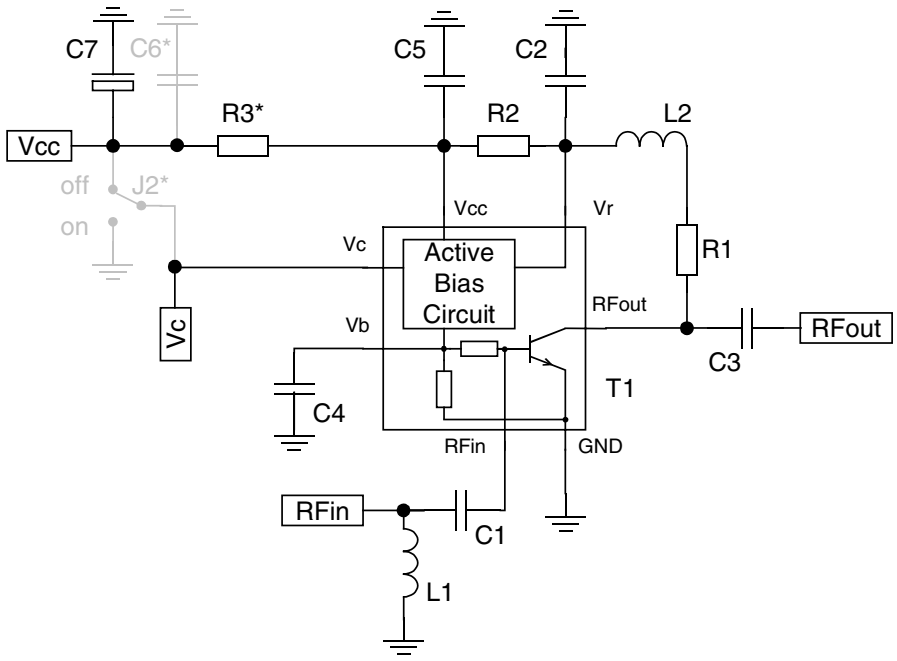


Figure 7. Schematic of 1850 MHz Amplifier

Symbol	Parameter	Unit	Measurement result
Gp	Power Gain ($\|S_{21}\|^2$)	dB	16
NF	Noise Figure	dB	≅ 1.65
RL_{in}	Input Return Loss	dB	>10
RL_{out}	Output Return Loss	dB	>10
OIP_3	Third-Order Intercept Point	dBm	10
P_{1dB}	Output Power at 1 dB Compression	dBm	1
A	Board Space (9 x 0402 + SCT598)	mm^2	20
n	Component Count	1	10

Table 1. Measured parameter values at 1850 MHz, 25˚ C and Vcc = 3V

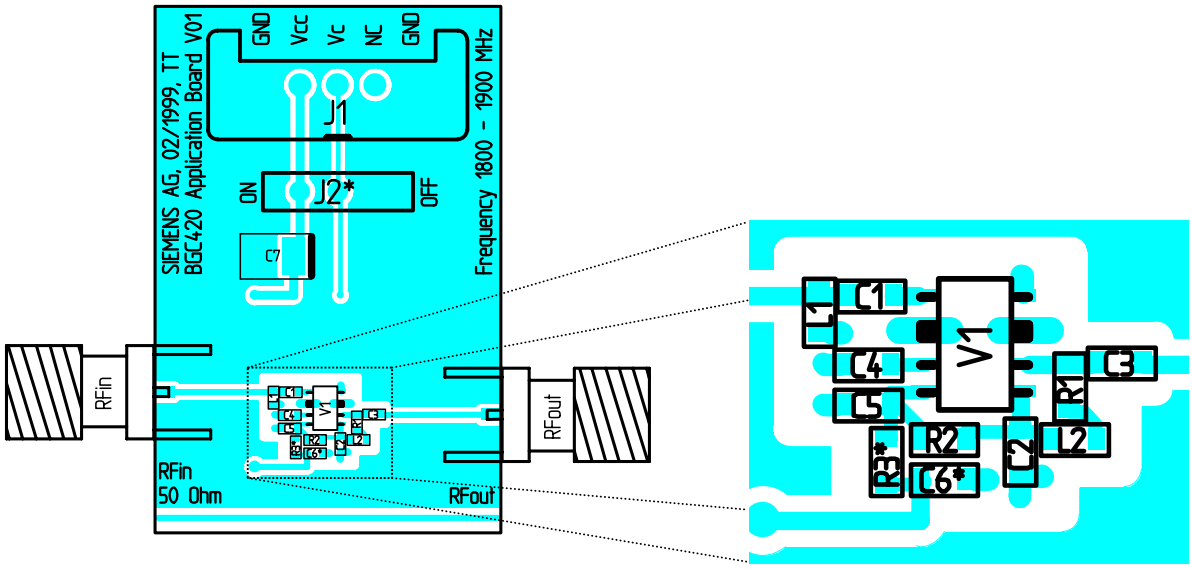


Figure 8. Application Board (scale 2:1, original size 23 x 35 mm)

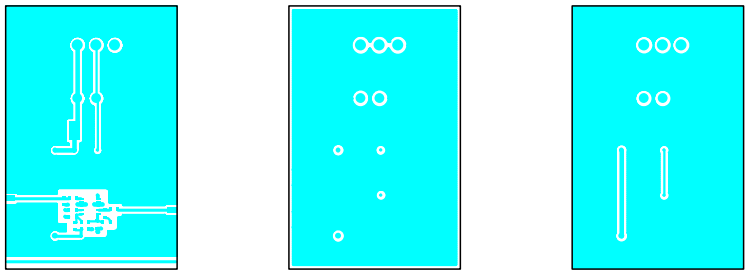


Figure 9. Top, Middle and Bottom layers of PCB-Board

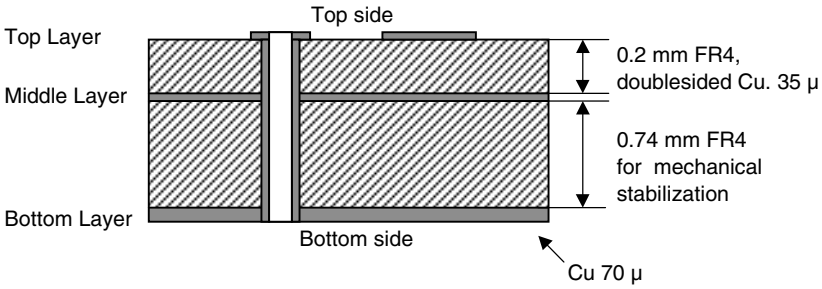


Figure 10. Cross-Section of PCB-Board

Name	Value	Package	Manufacturer	Function
C1	3.9 pF	0402	Murata (COG)	Input matching
C2	100 pF	0402	Murata (COG)	RF decoupling
C3	15 pF	0402	Murata (COG)	DC block
C4	1 nF	0402	Murata (X7R)	Low-frequency stabilisation
C5	100 pF	0402	Murata (COG)	Block capacitor
C6*	10 nF	0402	Murata (X7R)	Optional RF block capacitor
C7	6.8 µF	-	S+M (10V)	Block capacitor
J1	5 Pin	-	STOCKO / MKS1650	Pin connector
J2	3 Pin	-	APEM / NK 236	Switches LNA ON/OFF
L1	4.7 nH	0402	S+M	Input matching
L2	5.6 nH	0402	S+M	Output matching
R1	22 Ω	0402	S+M	Improves stability
R2	82 Ω	0402	S+M	Sets biasing to 7mA
R3*	0 Ω	0402	S+M	For measurement purpose
V1	BGC 420	SCT 598	Infineon (SIEMENS)	-
X1	SMA-Connector	SMA	Johnson	-
X2	SMA-Connector	SMA	Johnson	-

Table 2. Component Part list

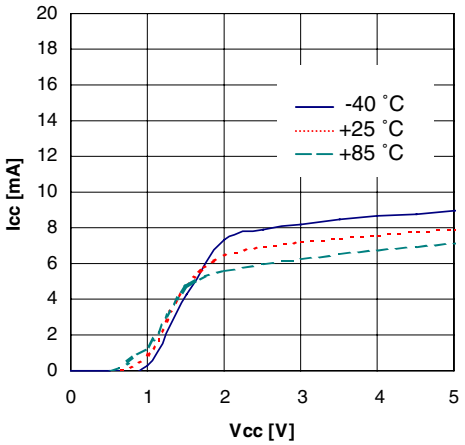


Figure 11. Icc vs. Vcc and Temperature

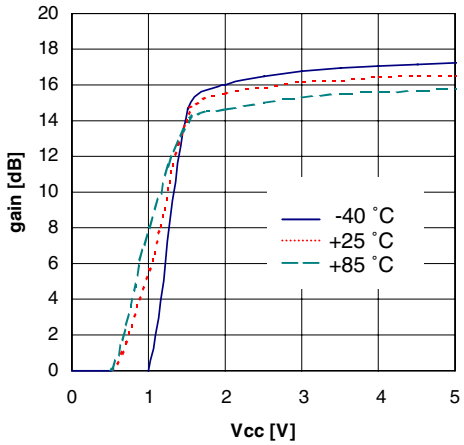


Figure 12. Gain vs. Vcc and Temperature at 1850 MHz

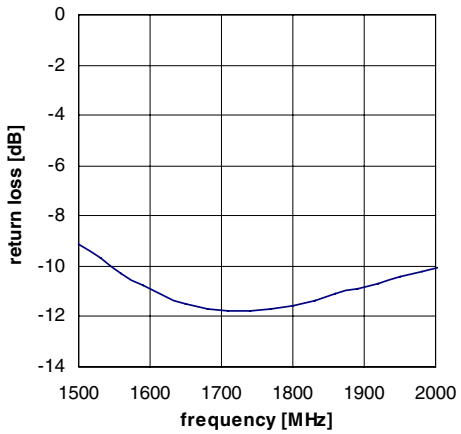


Figure 13. Input Return Loss vs. Frequency

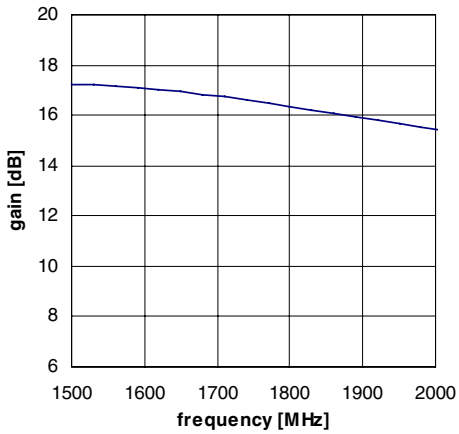


Figure 14. Gain vs. Frequency at 1850 MHz

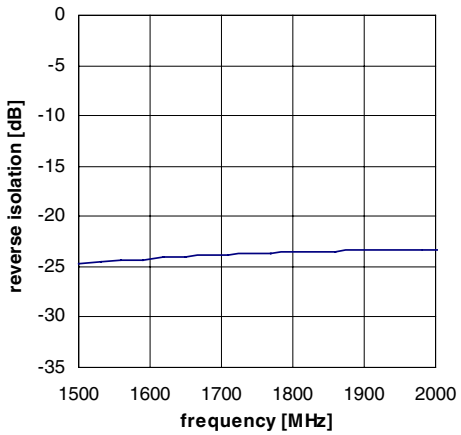


Figure 15. Return Isolation vs. Frequency

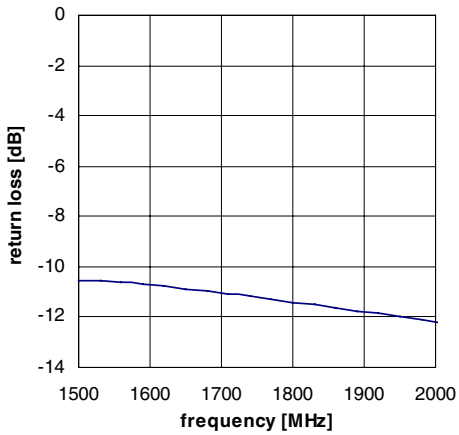


Figure 16. Output Return Loss vs.Frequency

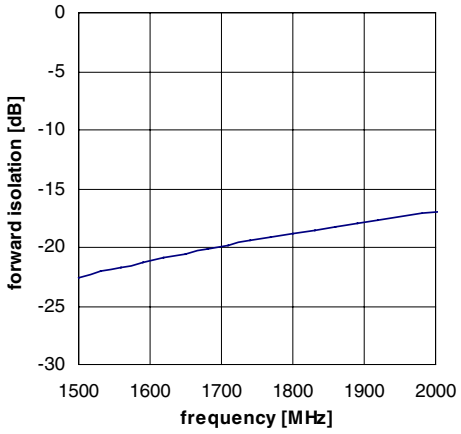


Figure 17. Forward Isolation vs. Frequency, LNA OFF (Vc = Vcc = 3V)

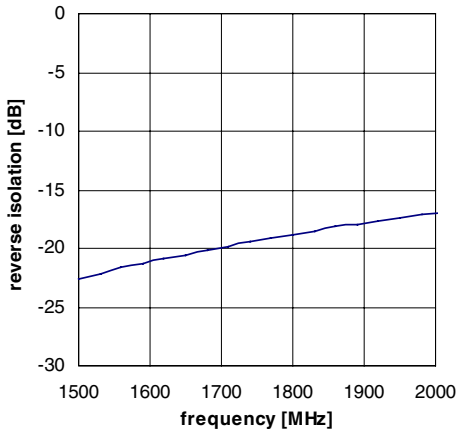


Figure 18. Reverse Isolation vs. Frequency, LNA OFF (Vc = Vcc = 3V)

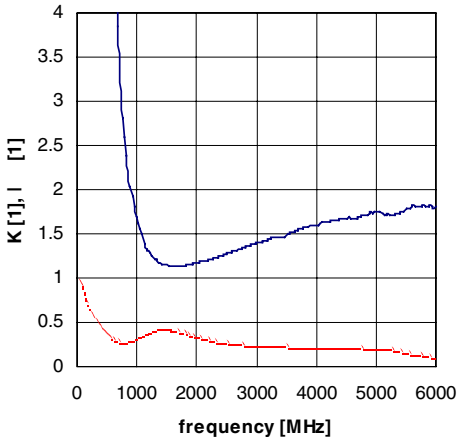


Figure 19. Stability Factor K, the magnitude of the S-matrix determinant vs. Frequency

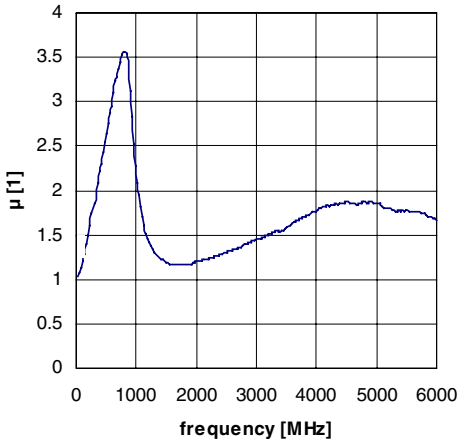


Figure 20. Stability Factor μ vs. Frequency

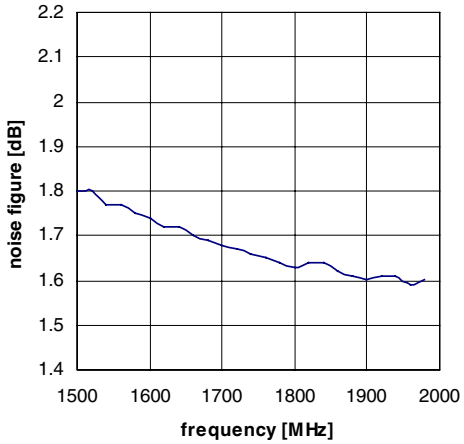


Figure 21. NF vs. Frequency (25 ˚C)

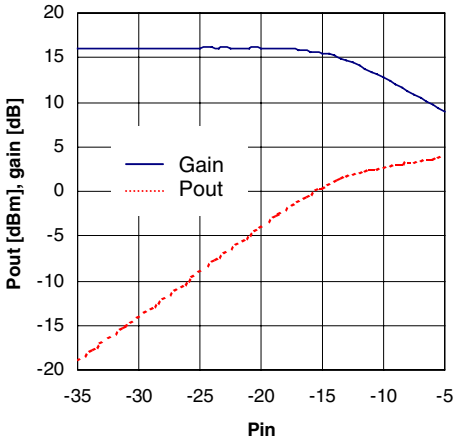


Figure 22. Gain, Pout vs. Frequency at 1850 MHz (P_{1dB} = 1 dBm)

Measured parameter values

Figures 11 to 22 show the measured parameter values at 25˚ C, Vcc = 3 V and 1850 MHz unless otherwise noted. These values include the losses of the SMA connectors and microstrip lines of the 0,2 mm FR4 epoxy board. Figure 11 shows the supply current versus supply voltage and temperatures. Gain over Vcc and temperature is represented in Figure 12. Figure 13 to 16 shows the S-parameter as measured when the LNA is switched on. Figure 17 and 18 present forward and reverse isolation when the LNA is off. The stability versus frequency is shown in figure 19 and 20. The stability factors are calculated from the S-parameters measured at the SMA-connectors. Finally the noise figure, output power and gain are presented in Figure 21 and 22. The noise figure can be reduced by 0.1 dB using L_1 = 4.7nH instead of 5.6nH. This also reduces gain.

In order to optimise the design for a particular application, observe following points:

- The stability can be increased by reducing L_2 = 5.6nH to 4.7nH or increasing the value of R_1.
- To avoid low frequency oscillation of the bias circuit, the blocking capacitor C_4 should be at least ten times the value of C_2. For further information refer to the BGC420 data sheet.
- The BGC 420 provides a control pin labelled Vc for switching off the device. Keep in mind that also the coupling capacitors at RFin / RFout determine the switching times. To determine the switching time, remove switch J_2 and use the Vc-pin from connector J_1 for switching the device.
- Place C_4 as close to the device as possible.

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