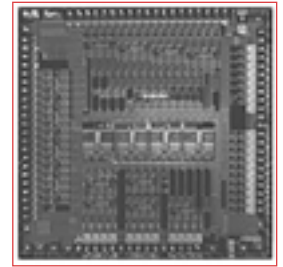




BCM8150 PRODUCT Brief



SONET TRANSCEIVER WITH INTERNAL LOOP TIMING AND PHASE DETECTOR

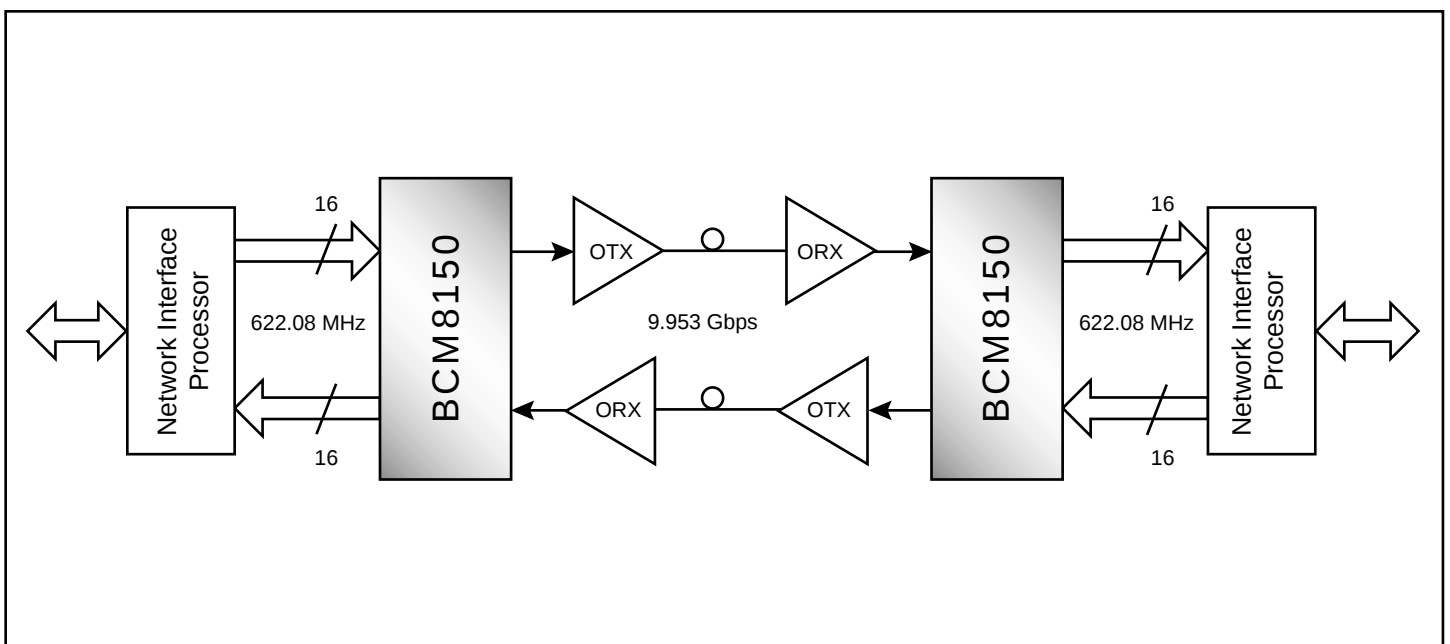
BCM8150 FEATURES

- Fully integrated CDR, MUX, DEMUX, and CMU
- OIF-compliant, 16-bit, 622.08 MHz LVDS interface
- On-chip PLL-based clock generator
- Line and system loopback modes
- Loss of Signal (LOS) Output and (LOSIB) Input
- Tx and Rx Lock Detect
- Elastic buffering with FIFO overflow alarm
- 155.52 or 622.08 MHz reference clock
- Selectable Rx Clock and Rx Data Squelch on LOS
- Selectable Loop Timing mode
- Dual REFCLK inputs
- Internal phase detector and charge pump for cleanup PLL. External VCXO required.
- Power supplies: Core, CML, and LVDS at 1.8V, CMOS at 1.8 or 3.3V, LVPECL at 3.3V
- Standard CMOS fabrication process
- Power dissipation: 1.3W maximum at 1.8V

SUMMARY OF BENEFITS

- Compliant with industry standards such as: Optical Internetworking Forum (OIF), Telcordia, and ITU-T standards.
- Reduces design cycle and time to market.
- High level of integration allows for higher port density solutions.
- CMOS-based device uses the most effective silicon economy of scale.
- Exceeds SONET jitter requirements
- Target Applications:
 - STS-192/STM-64 Transmission Equipment
 - SONET/SDH Optical Modules
 - ADD/DROP Multiplexers
 - Digital Cross-Connects
 - ATM Switch Backbone
 - SONET Test Equipment
 - Terabit and Edge Routers

Application Block Diagram



BCM 8150 OVERVIEW



Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. An on-chip phase detector and charge pump plus external VCXO implements a cleanup PLL. The cleanup PLL may be used to clean up the recovered CDR clock for loop timing applications or to clean up a noisy system clock.

The OIF-compliant, low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia (formerly Bellcore), ANSI, and ITU-T standards. The **BCM8150** is packaged in a 21 x 21 x 1.71 mm BGA.

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