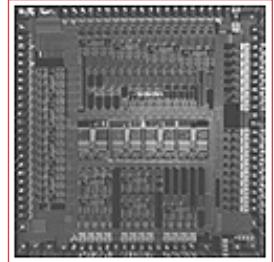




BCM8010 PRODUCT Brief



10 GIGABIT ETHERNET CMOS TRANSCEIVER OVER FIBER

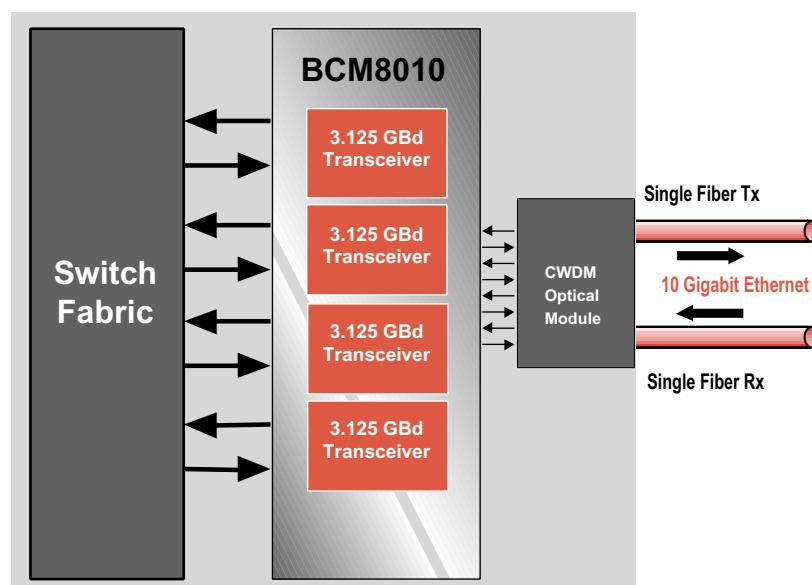
BCM8010 FEATURES

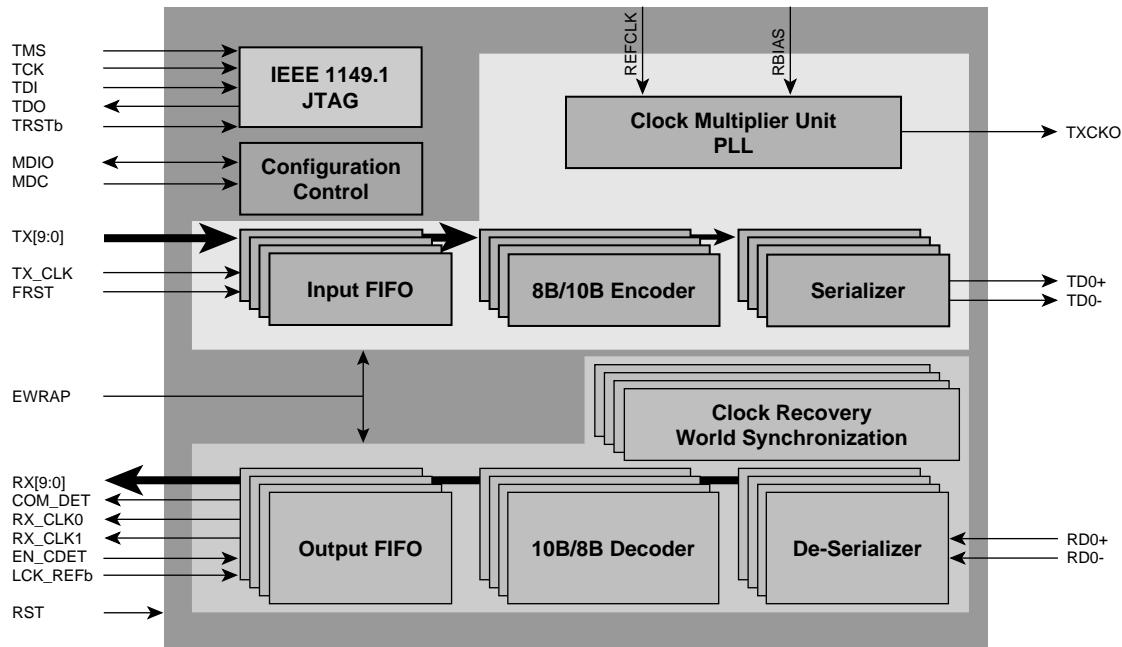
- 10-Gigabit Ethernet 4-Channel CMOS Transceiver
- Supporting 1.25 to 3.125 Gigabit per Second (Gbps) Full Duplex Operation
- Less than 3 ps RMS Transmit Jitter using Broadcom's LC VCO Technology
- Adaptive Equalizer at each Receiver
- 10-bit Parallel SSTL_2/HSTL Compatible Interface
- On-chip Phase-Locked Loop (PLL) Providing Clock Synthesis from 62.5, 125, or 156 MHz Reference Clock
- Optional 8B/10B Encoder and 10B/8B Decoder (with bypass mode)
- Parallel or Serial Loop-back Mode
- Built-In Self-Test (BIST) Capability
- MDC/MDIO Management Interface
- Termination Resistors on Chip
- Low Power 0.25 micron CMOS Process Technology (2.5 V Supply)
- 256-pin TBGA (27 mm X 27 mm)

SUMMARY OF BENEFITS

- Enables data transfer rate of 10 Gbps over metropolitan network when used with a four wavelength CWDM laser module
- Low jitter and integrated equalizer on every channel result in longer cable reach (over 50km) and superior transceiver performance
- Supports the proposed XAUI and XMII IEEE transceiver standards
- 10 Gbps channel aggregation capability by synchronizing all 4 channels
- Bypassing 8B/10B encoding and 10B/8B decoding enables full utilization of the 12.5 Gbps data transfer rate
- Global Configuration Registers enable/disable functions such as: PLL lock, channel synchronization, VCO bypass, speed selection from 1.25 to 3.125 GBd, serial and loopback modes for self diagnostics, single and double data rate selections
- Each transceiver can be independently reset/powered down
- Receiver FIFO is provided for de-skew of the four data streams

10 Gigabit Ethernet over long haul Single Mode Fiber





The **BCM8010** integrates four channels of the new Broadcom FusionCore™ - a programmable, high performance mixed-signal transceiver core, capable of transmitting and receiving at data rates ranging from 1.25 to 3.125 gigabits per second (Gbps).

The chip provides aggregate bandwidth of 10 Gbps full duplex extending Ethernet capabilities into the Wide Area Network (WAN). It enables establishing a cost-effective 10 Gbps Ethernet link over local, regional and metropolitan fiber optic networks.

It is the first transceiver to incorporate receiver adaptive equalizers at these speeds, which improve overall cable reach and transceiver performance. The unique equalizer design removes inter-symbol interference from the incoming data stream, enhancing noise immunity and providing optimum transceiver performance.

Fully integrated PLL and Clock & Data Recovery (CDR) enables individual channels to lock to the incoming data. The unique

design of the LC VCO and CDR blocks have resulted in superior jitter performance (<3pSec) implemented in CMOS. All receivers can be synchronized using a robust design of buffers. Similarly, the chip offers the option of synchronizing the transmitters for simultaneous transmission.

The transmitter section accepts Ten Bit Interface (TBI) parallel SSTL_2/HSTL data at 125 MHz byte clock and serializes into a CML high speed serial data for each channel.

The receiver section enables individual channels to lock to the incoming data. The recovered data is presented at the SSTL_2/HSTL parallel outputs. The 8B/10B encoding and 10B/8B decoding of the PCS layer, speed selection, channel alignment schemes, VCO and Synchronization bypass capabilities are addressed through configuration registers.

The BCM8010 is manufactured in a standard single-poly low-cost CMOS process and is offered in a 256-pin TBGA package.

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