■ FEATURES

- Ultra low operation voltage : 1.8V ~ 3.6V
- Ultra low power consumption :
  - Vcc = 2.0V C-grade : 10mA (Max.) operating current
    - I- grade : 15mA (Max.) operating current
    - 0.005uA (Typ.) CMOS standby current
  - Vcc = 3.0V C-grade : 20mA (Max.) operating current
    - I-grade : 25mA (Max.) operating current
    - 0.01uA (Typ.) CMOS standby current
- High speed access time :
  - -15 150ns (Max.) at Vcc = 2.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options

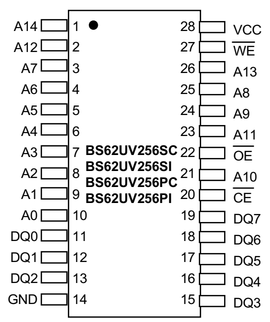
■ DESCRIPTION

The BS62UV256 is a high performance, ultra low power CMOS Static Random Access Memory organized as 32,768 words by 8 bits and operates from a wide range of 1.8V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.005uA and maximum access time of 150ns in 2V operation.
Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The BS62UV256 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS62UV256 is available in the JEDEC standard 28 pin 330mil Plastic SOP, 8mmx13.4mm TSOP (normal type), 300mil Plastic SOJ and 600mil Plastic DIP.

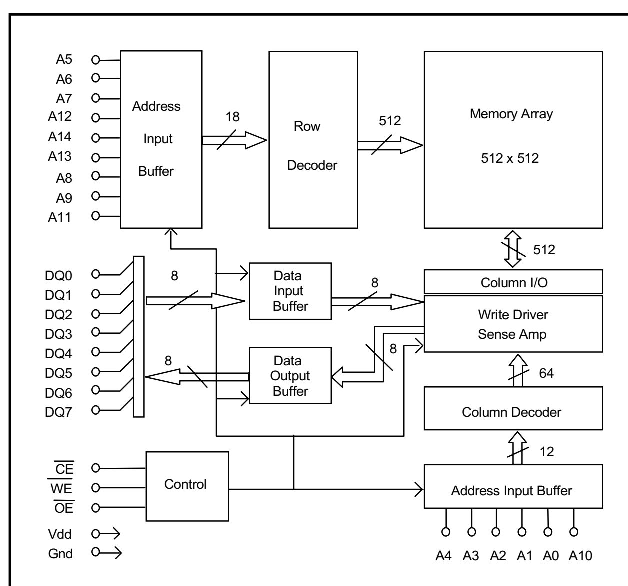
■ PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				STANDBY (I_{CCSB1}, Max)		Operating (I_{CC}, Max)		
			Vcc= 2.0V	Vcc= 3.0V	Vcc= 2.0V	Vcc= 3.0V	Vcc= 2.0V	
BS62UV256SC	+0 °C to +70 °C	1.8V ~ 3.6V	150	0.2uA	0.1uA	20mA	10mA	SOP-28
BS62UV256TC								TSOP-28
BS62UV256PC								PDIP-28
BS62UV256JC								SOJ-28
BS62UV256DC								DICE
BS62UV256SI	-40 °C to +85 °C	1.8V ~ 3.6V	150	0.4uA	0.3uA	25mA	15mA	SOP-28
BS62UV256TI								TSOP-28
BS62UV256PI								PDIP-28
BS62UV256JI								SOJ-28
BS62UV256DI								DICE

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A14 Address Input	These 15 address inputs select one of the 32768 x 8-bit words in the RAM
$\overline{CE}$ Chip Enable Input	$\overline{CE}$ is active LOW. Chip enables must be active to read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
DQ0 – DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	DOUT	I_{CC}
Write	L	L	X	DIN	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{o}C
T_{STG}	Storage Temperature	-60 to +150	^{o}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 ^{O}C to +70 ^{O}C	1.8V ~ 3.6V
Industrial	-40 ^{O}C to +85 ^{O}C	1.8V ~ 3.6V

■ CAPACITANCE (1) (TA = 25^{o}C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=2.0V	-0.5	--	0.6	V
			Vcc=3.0V			0.8	
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=2.0V	1.4	--	Vcc+0.2	V
			Vcc=3.0V	2.0			
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc		--	--	1	uA
I_{OL}	Output Leakage Current	Vcc = Max, $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc		--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 1mA	Vcc=2.0V	--	--	0.4	V
			Vcc=3.0V				
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -0.5mA	Vcc=2.0V	1.6	--	--	V
			Vcc=3.0V	2.4			
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, F = Fmax(3)	Vcc=2.0V	--	--	10	mA
			Vcc=3.0V	--	--	20	
I_{CCSB}	Standby Current-TTL	$\overline{CE}$ = V_{IH}, I_{DQ} = 0mA	Vcc=2.0V	--	--	0.5	mA
			Vcc=3.0V	--	--	1.0	
I_{CCSB1}	Standby Current-CMOS	$\overline{CE}$ ≧ Vcc-0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	Vcc=2.0V	--	0.005	0.1	uA
			Vcc=3.0V	--	0.01	0.2	

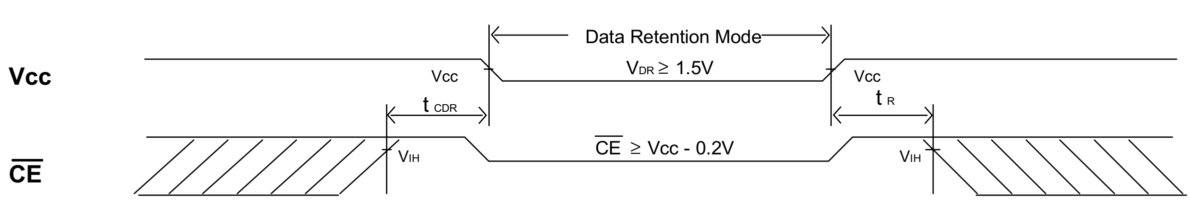
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ DATA RETENTION CHARACTERISTICS (TA = 0°C to + 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE}$ ≧ Vcc - 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≧ Vcc -0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.005	0.1	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE}$ Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ AC TEST LOADS AND WAVEFORMS

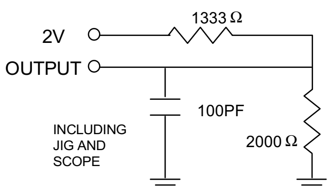


FIGURE 1A

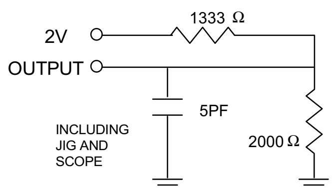
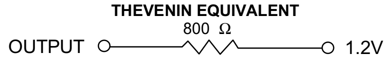


FIGURE 1B

THEVENIN EQUIVALENT



ALL INPUT PULSES

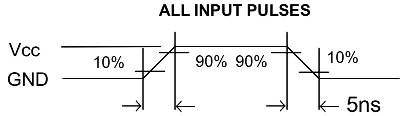
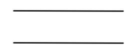
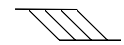
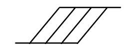
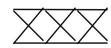
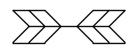


FIGURE 2

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

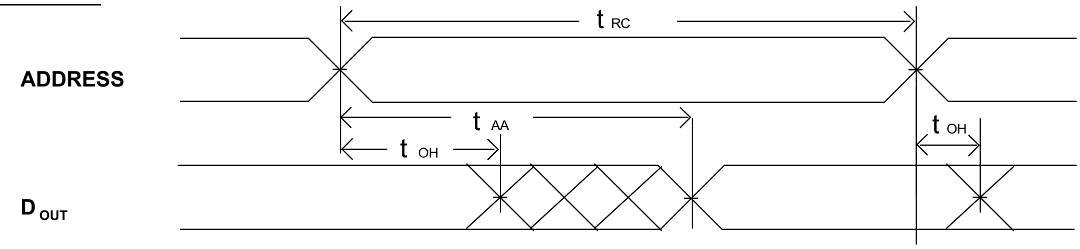
■ AC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C, Vcc = 2.0V)

READ CYCLE

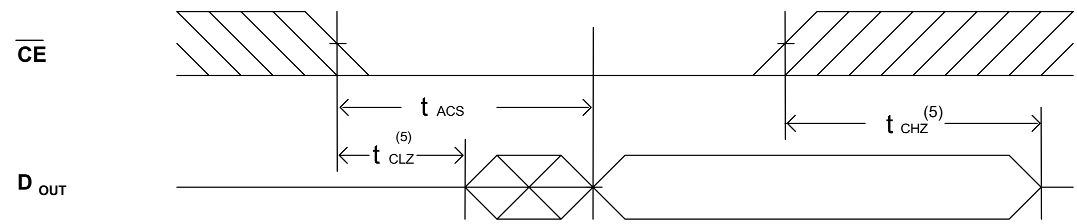
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS62UV256-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	150	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	150	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time	--	--	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	100	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	ns
t_{AXOX}	t_{OH}	Output Disable to Output Address Change	10	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

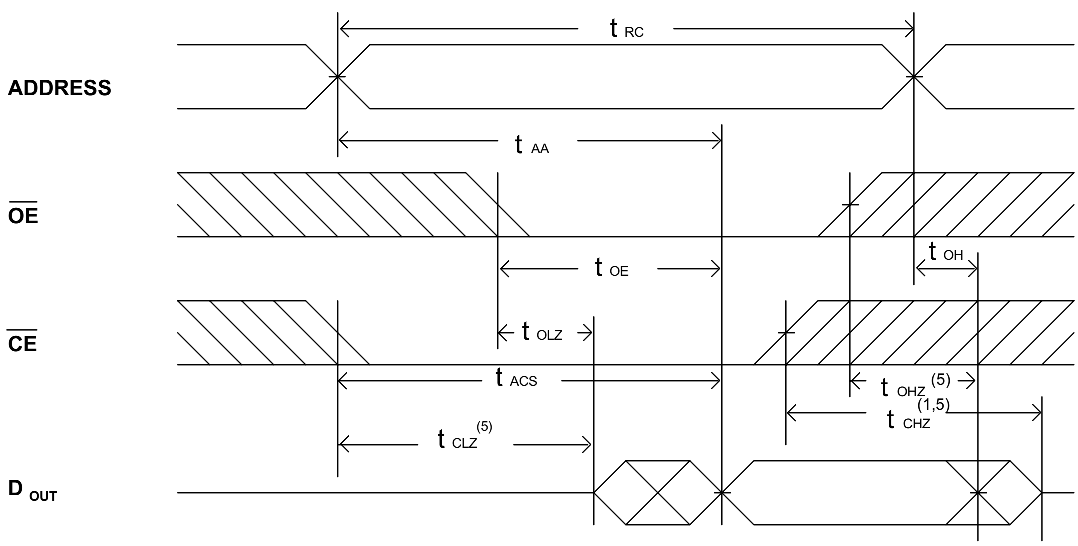
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL} .
5. Transition is measured $\pm$500mV from steady state with C_L = 5pF as shown in Figure 1B.
   The parameter is guaranteed but not 100% tested.

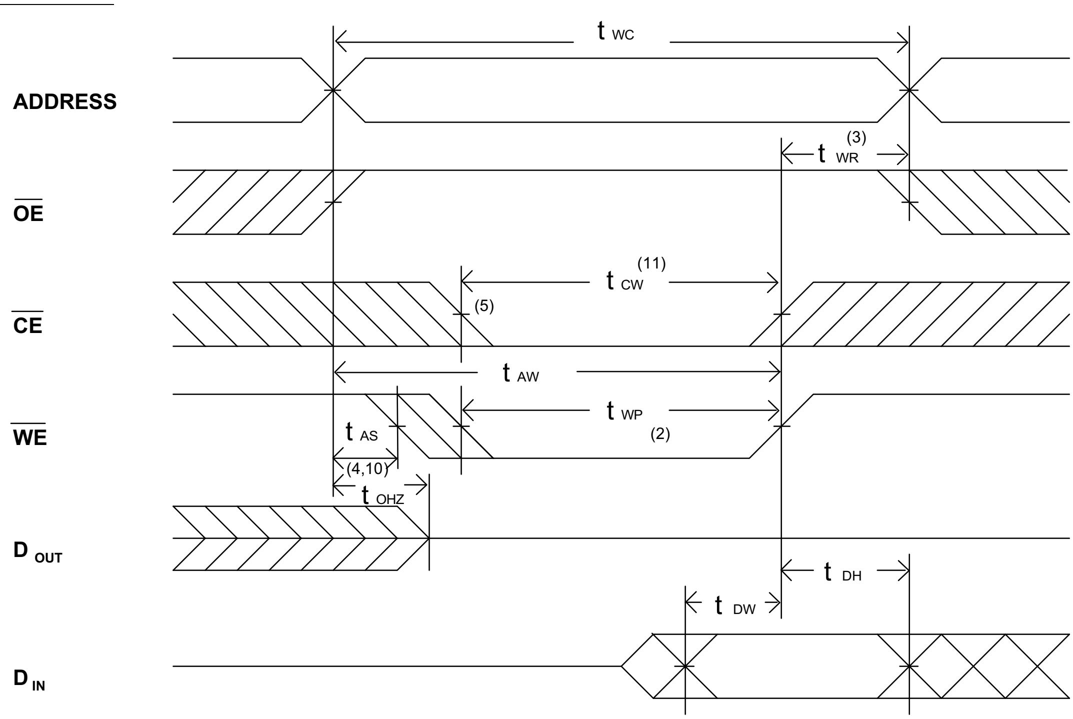
■ AC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C, Vcc = 2.0V)

WRITE CYCLE

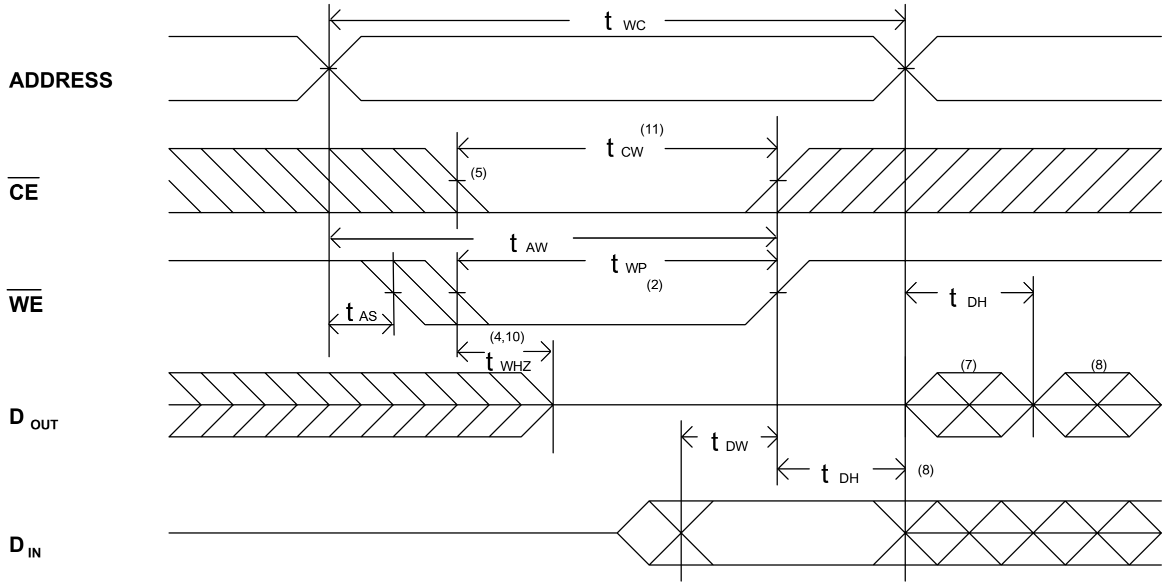
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS62UV256-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	150	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	150	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	150	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	80	--	--	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	--	--	ns
t_{WLOZ}	t_{WHZ}	Write to Output in High Z	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	ns
t_{WHQX}	t_{OW}	End ot Write to Output Active	5	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



WRITE CYCLE2 (1,6)



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm$500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

■ ORDERING INFORMATION

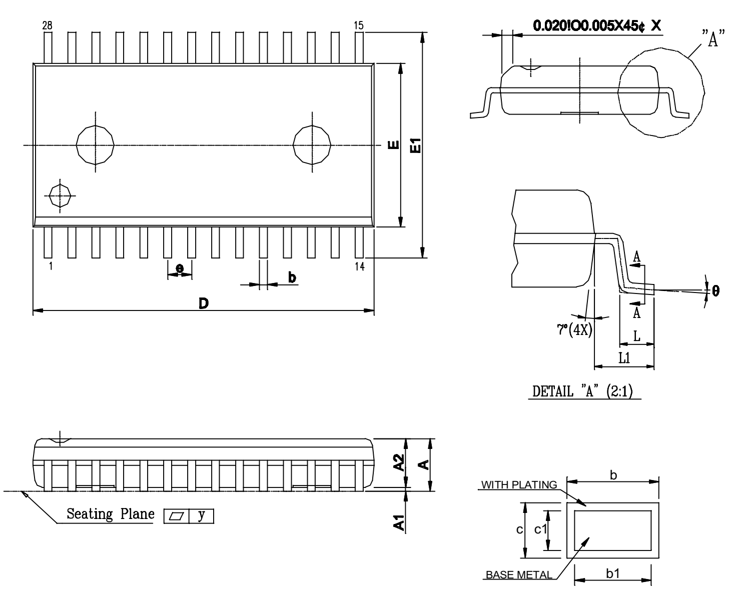
BS62UV256 X X -- Y Y

SPEED
15: 150ns

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

PACKAGE
S: SOP
P: PDIP
J : SOJ
T: TSOP (8mm x 13.4mm)
D : DICE

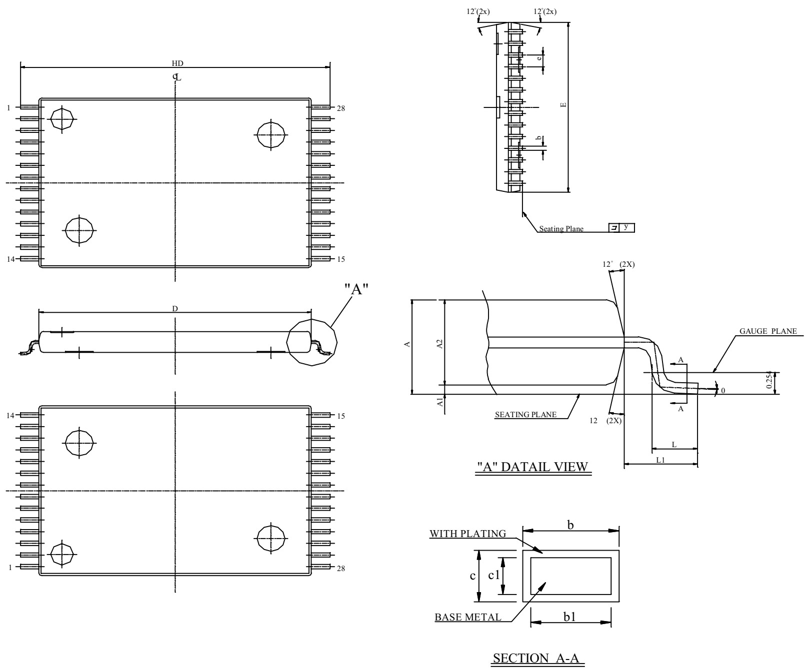
■ PACKAGE DIMENSIONS



SYMBOL \ UNIT	INCH	MM
A	0.106±0.006	2.692±0.152
A1	0.009±0.005	0.226±0.124
A2	0.098±0.005	2.489±0.127
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.45
c	0.008 ~ 0.012	0.20 ~ 0.32
c1	0.008 ~ 0.011	0.20 ~ 0.28
D	0.713±0.005	18.110±0.127
E	0.331±0.005	8.407±0.127
E1	0.465±0.012	11.811±0.305
e	0.050±0.006	1.270±0.152
L	0.0380±0.0104	0.964±0.264
L1	0.0677±0.0079	1.72±0.2
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

SOP - 28

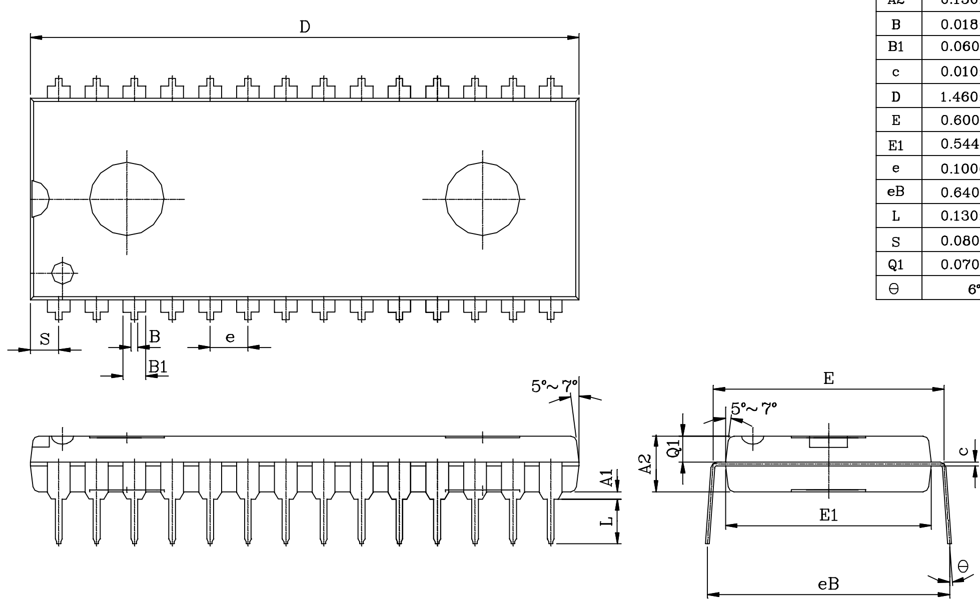
■ PACKAGE DIMENSIONS (continued)



UNIT / SYMBOL	INCH	MM
A	0.0433±0.004	1.10±0.10
A1	0.0045±0.0026	0.115±0.065
A2	0.039±0.002	1.00±0.05
b	0.009±0.002	0.22±0.05
b1	0.008±0.001	0.20±0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022±0.004	0.55±0.10
HD	0.528±0.008	13.40±0.20
L	$0.0197\ ^{+0.008}_{-0.004}$	$0.50\ ^{+0.20}_{-0.10}$
L1	0.0315±0.004	0.80±0.10
y	0.004 Max.	0.1 Max.
θ	0°~ 8°	0°~ 8°

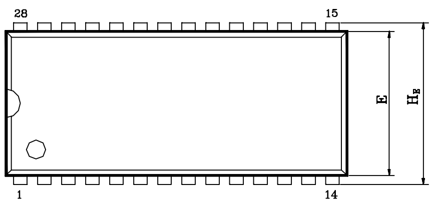
TSOP - 28

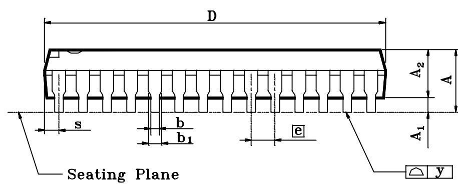
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150±0.005	3.810±0.127
B	0.018±0.005	0.457±0.127
B1	0.060±0.010	1.524±0.254
c	0.010±0.004	0.254±0.102
D	1.460±0.005	37.084±0.127
E	0.600±0.010	15.240±0.254
E1	0.544±0.004	13.818±0.102
e	0.100(TYP)	2.540(TYP)
eB	0.640±0.020	16.256±0.508
L	0.130±0.010	3.302±0.254
S	0.080±0.010	2.032±0.254
Q1	0.070±0.005	1.778±0.127
Θ	6°±3°	6°±3°

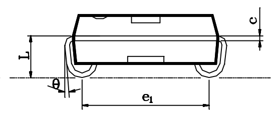


PDIP - 28

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.140	—	—	3.56
A_1	0.027	—	—	0.69	—	—
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.710	0.730	—	18.03	18.54
E	0.295	0.300	0.305	7.49	7.62	7.75
$\boxed{e}$	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.245	0.265	0.285	6.22	6.73	7.24
H_E	0.327	0.337	0.347	8.31	8.56	8.81
L	0.077	0.087	0.097	1.96	2.21	2.46
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°







Note:
1. Dimension D Max & s include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inch
5. General appearance spec. should be based on final visual inspection spec.

SOJ - 28