B9949

3.3V, 160MHz, 1:15 Clock Distribution Buffer

Approved Product

Product Features

- 160MHz Clock Support
- LVPECL or LVCMOS/LVTTL Clock Input
- LVCMOS/LVTTL Compatible Inputs
- 15 Clock Outputs: Drive up to 30 Clock Lines
- 1X and 1/2X Configurable Outputs
- Output Tri-state Control
- 350ps Maximum Output-to-Output Skew
- Pin Compatible with MPC949
- 52-Pin TQFP Package

Description

The B9949 is a low voltage clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9949 has an effective fan-out of 1:30.

The B9949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The B9949 outputs can also be tri-stated via MR/OE# input. When MR/OE# is set high, it resets the internal flip-flops and tri-states the outputs.

Block Diagram

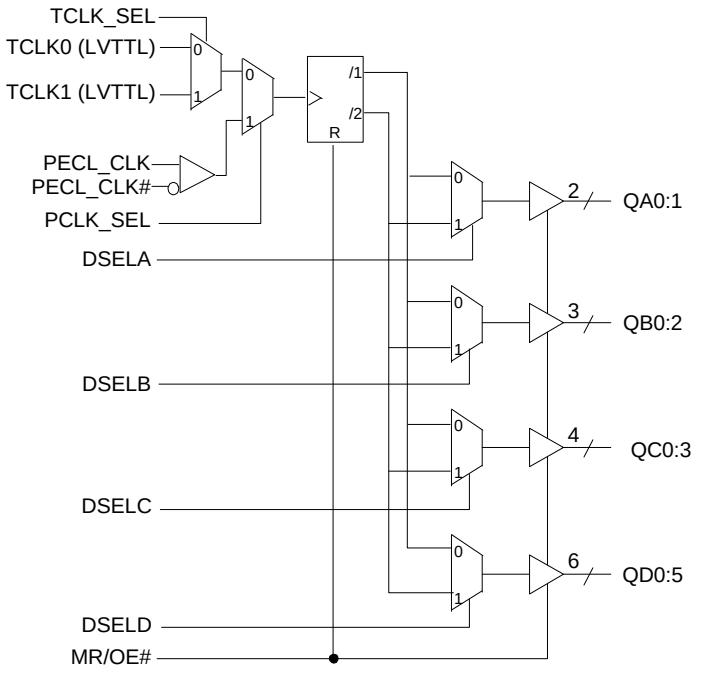
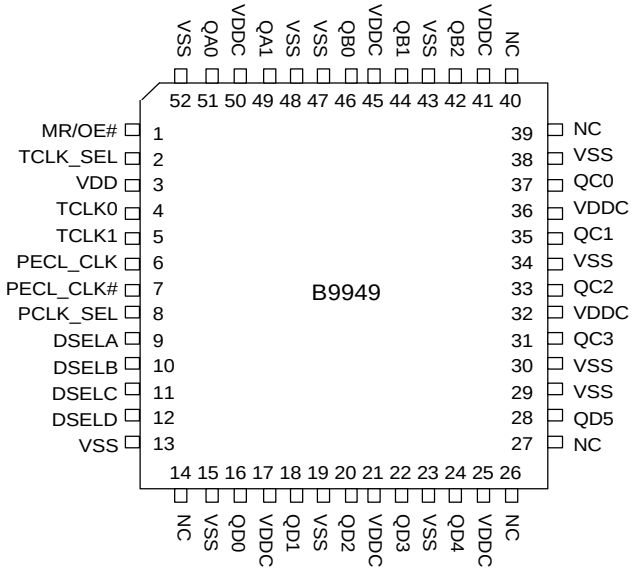


Figure 1

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	Description
6	**PECL_CLK**		I, PD	PECL Input Clock.
7	**PECL_CLK#**		I, PU	PECL Input Clock.
4, 5	**TCLK(0,1)**		I, PU	External Reference/Test Clock Input.
49, 51	**QA(1,0)**	VDDC	O	Clock Outputs.
42, 44, 46	**QB(2:0)**	VDDC	O	Clock Outputs.
31, 33, 35, 37	**QC(3:0)**	VDDC	O	Clock Outputs.
16, 18, 20, 22, 24, 28	**QD(5:0)**	VDDC	O	Clock Outputs.
9, 10, 11, 12	**DSEL(A:D)**		I, PD	Divider Select Inputs. When high, selects ÷2 input divider. When low, selects ÷1 input divider.
2	**TCLK_SEL**		I, PD	TCLK Select Input. When low, TCLK0 clock is selected and when high TCLK1 is selected.
8	**PCLK_SEL**		I, PD	PECL Select Input. When high, PECL clock is selected and when low TCLK(0,1) is selected
1	**MR_OE#**		I, PD	Output Enable Input. When asserted low, the outputs are enabled and when asserted high, internal flip-flops are reset and the outputs are tri-stated.
17, 21, 25, 32, 36, 41, 45, 50	**VDDC**			3.3V Power Supply for Output Clock Buffers.
3	**VDD**			3.3V Power Supply
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	**VSS**			Common Ground
14, 26, 27, 39, 40,	**NC**			Not Connected

PD = Internal Pull-Down, PU = Internal Pull-Up.