B9947

3.3V, 160MHz, 1:9 Clock Distribution Buffer

Approved Product

Product Features

- 160MHz Clock Support
- LVCMOS/LVTTL Compatible Inputs
- 9 Clock Outputs: Drive up to 18 Clock Lines
- Synchronous Output Enable
- Output Tri-state Control
- 350ps Maximum Output-to-Output Skew
- Pin Compatible with MPC947
- 32-Pin TQFP Package

Description

The B9947 is a low voltage clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The nine outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9947 has an effective fan-out of 1:18. The outputs can also be tri-stated via the tri-state input TS#. Low output-to-output skews make the B9947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The B9947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram

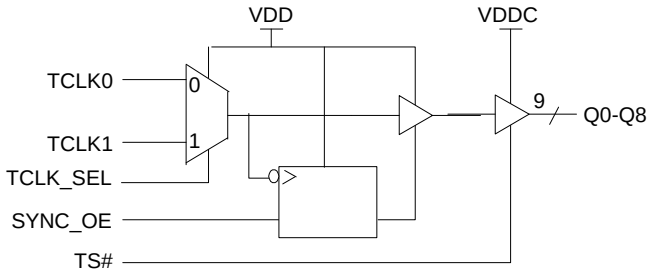
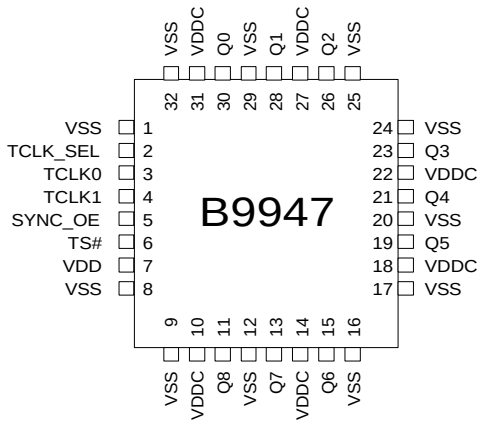


Figure 1

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	Description
3	**TCLK0**		I, PU	Test Clock Input.
4	**TCLK1**		I, PU	Test Clock Input.
2	**TCLK_SEL**		I, PU	Test Clock Select Input. When low, TCLK0 is selected. When asserted high, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	**Q(8:0)**	VDDC	O	Clock Outputs.
5	**SYNC_OE**		I, PU	Output Enable Input. When asserted high, the outputs are enabled and when set low the outputs are disabled in a low state.
6	**TS#**		I, PU	Tri-state Control Input. When asserted low, the output buffers are tri-stated. When set high, the output buffers are enabled.
10, 14, 18, 22, 27, 31	**VDDC**			3.3V Power Supply for Output Clock Buffers.
7	**VDD**			3.3V Power Supply
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	**VSS**			Common Ground

PU = Internal Pull-Up.