



B9946

3.3V, 160MHz, 1:10 Clock Distribution Buffer

Approved Product

Product Features

- 160MHz Clock Support
- LVC MOS/LVTTL Compatible Inputs
- 10 Clock Outputs: Drive up to 20 Clock Lines
- 1X or 1/2X Configurable Outputs
- Output Tri-state Control
- 250ps Maximum Output-to-Output Skew
- Pin Compatible with MPC946
- 32-Pin TQFP Package

Block Diagram

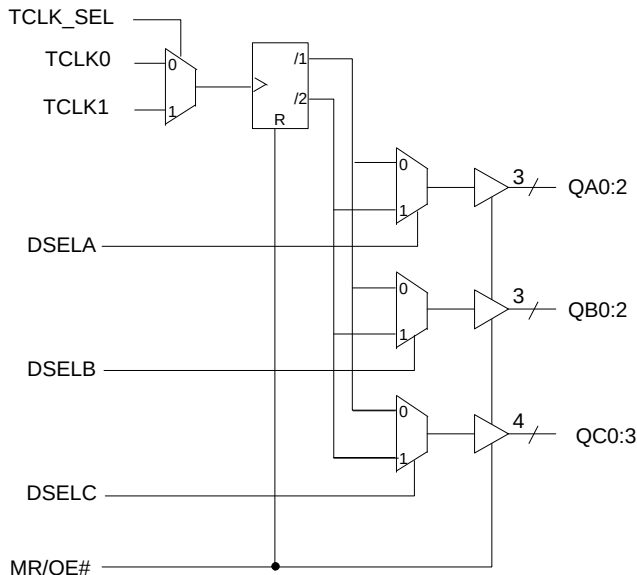


Figure 1

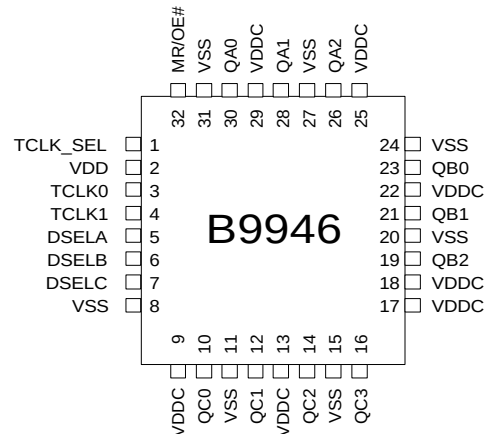
Description

The B9946 is a low voltage clock distribution buffer with the capability to select one of two LVC MOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVC MOS/LVTTL compatible. The 10 outputs are 3.3V LVC MOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9946 has an effective fan-out of 1:20.

The B9946 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1X to 1/2X outputs.

The B9946 outputs can also be tri-stated via MR/OE# input. When MR/OE# is set high, it resets the internal flip-flops and tri-states the outputs.

Pin Configuration





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Pin Description

PIN	NAME	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input.
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs.
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs.
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs.
5, 6, 7	DSEL(A:C)		I, PD	Divider Select Inputs. When high, selects ÷2 input divider. When low, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When low, TCLK0 clock is selected and when high TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted low, the outputs are enabled and when asserted high, internal flip-flops are reset and the outputs are tri-stated.
9, 13, 17, 18, 22, 25, 29	VDDC			3.3V Power Supply for Output Clock Buffers.
2	VDD			3.3V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.