

Preliminary

Product Features

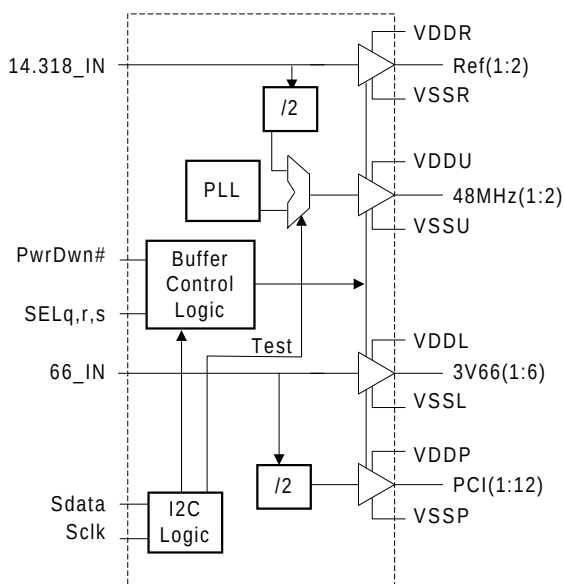
- Six 3V66 clocks
- Twelve 3V, 33 MHz PCI clocks
- Two 48 MHz clocks
- Two 14.318 MHz reference clocks
- Select logic, Hi-Z, and output disable modes
- Power Savings Clock OFF Mode
- 66 MHz reference input for PCI and 3V66 clocks
- 14.318 reference input for REF and 48M clocks
- 56 Pin SSOP and TSSOP Package

Frequency Selection Table

SELq	SELr	SELs	Description
0	0	0	All outputs on
0	0	1	PCI(1:8) off in low state
0	1	0	PCI(1:6) off in low state
0	1	1	All PCI off
1	0	0	All outputs Hi-Z
1	0	1	3V66_1 off in low state
1	1	0	Ref(1:2) off in low state
1	1	1	48MHz1 off in low state

NOTE: all SEL changes cause glitch free output clock transitions to occur.

Block Diagram



Pin Configuration

VSSN	1	56	VDDR
14.318_In	2	55	Ref1
VDDN	3	54	Ref2
66_In	4	53	VSSR
VSSP	5	52	VDDL
PCI1	6	51	3V66_1
PCI2	7	50	3V66_2
VDDP	8	49	VSSL
VSSP	9	48	VSSL
PCI3	10	47	3V66_3
PCI4	11	46	3V66_4
VDDP	12	45	VDDL
VSSP	13	44	VDDL
PCI5	14	43	3V66_5
PCI6	15	42	3V66_6
VDDP	16	41	VSSL
PCI7	17	40	VDD
PCI8	18	39	VSS
VSSP	19	38	VDDU
VDDP	20	37	48 MHz1
PCI9	21	36	48 MHz2
PCI10	22	35	VSSU
VSSP	23	34	Sels
PCI11	24	33	PwrDwn#
PCI12	25	32	VDD
VDDP	26	31	VSS
Selq	27	30	Sclock
Selr	28	29	Sdata